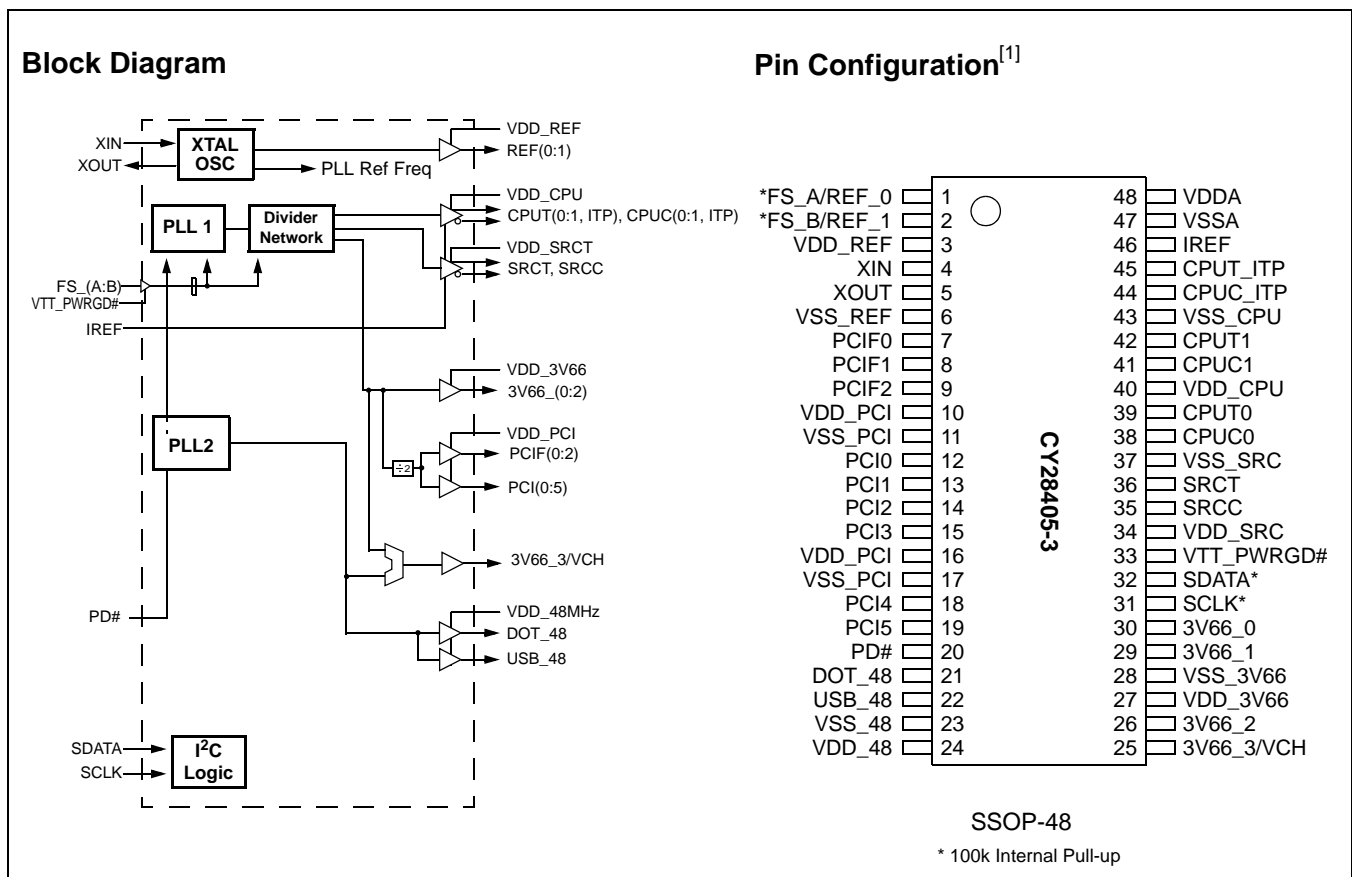# SPECTRALINEAR

# CY28405-3

# Clock Synthesizer with Differential SRC and CPU Outputs

## Features

- **Supports Intel® Pentium® 4-type CPUs**
- **Selectable CPU frequencies**
- **3.3V power supply**
- **Nine copies of PCI clocks**
- **Four copies of 3V66 with one optional VCH**
- **Two copies 48 MHz clock**
- **Two copies of REF**

- **Three differential CPU clock pairs**
- **One differential SRC clock**
- **Support SMBus/I²C Byte, Word and Block Read/ Write**
- **Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction**
- **48-pin SSOP package**

| CPU | SRC | 3V66 | PCI | REF | 48M |
|-----|-----|------|-----|-----|-----|
| x 3 | x 1 | x 4  | x 9 | x 2 | x 2 |

## Block Diagram

## Pin Configuration[1]



SSOP-48

* 100k Internal Pull-up

**Note:**
1. Signals marked with [*] and [**] have internal pull-up and pull-down resistors, respectively.

## Pin Description

| Pin No. | Name | Type | Description |
|---------|------|------|-------------|
| 1 | FS_A/REF_0 | I/O, SE | **This pin is the FS_A at power-up and VTT_PWRGD# = 0**, then it becomes REF_0 output. (3.3V 14.318-MHz clock output.) |
| 2 | FS_B/REF_1 | I/O, SE | **This pin is the FS_B at power up and VTT_PWRGD# = 0**, then it becomes REF_1 output. (3.3V 14.318-MHz clock output.) |
| 4 | XIN | I | **Crystal connection or external reference frequency input**. This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input. |
| 5 | XOUT | O, SE | **Crystal connection**. Connection for an external 14.318-MHz crystal output. |
| 39, 42, 38, 41, 45, 44 | CPUT(0:1), CPUC(0:1), CPUT_ITP, CPUC_ITP | O, DIF | **CPU clock output**. Differential CPU clock outputs. See *Table 1* for frequency configuration. |
| 36, 35 | SRCT, SRCC | O, DIF | Differential serial reference clock. |
| 26, 29, 30 | 3V66(2:0) | O, SE | **66 MHz clock output**. 3.3V 66 MHz clock from internal VCO. |
| 25 | 3V66_3/VCH | O, SE | **48 or 66 MHz clock output**. 3.3V selectable through SMBUS to be 66 MHz or 48 MHz. Default is 66 MHz. |
| 7, 8, 9 | PCI_F(0:2) | O, SE | **Free-running PCI Output**. 33 MHz clocks divided down from 3V66. |
| 12, 13, 14, 15, 18, 19 | PCI(0:5) | O, SE | **PCI Clock Output**. 33 MHz clocks divided down from 3V66. |
| 22 | USB_48 | O, SE | Fixed 48 MHz clock output. |
| 21 | DOT_48 | O, SE | Fixed 48MHz clock output. |
| 46 | IREF | I | **Current Reference**. A precision resistor is attached to this pin which is connected to the internal current reference. |
| 20 | PD# | I, PU | **3.3V LVTTL input for PowerDown# active low**. |
| 33 | VTT_PWRGD# | I | **3.3V LVTTL input is a level sensitive strobe used to latch the FS[A:E] input (active low)**. |
| 32 | SDATA | I/O, PU | SMBus-compatible SDATA. |
| 31 | SCLK | I, PU | SMBus-compatible SCLOCK. |
| 48 | VDDA | PWR | 3.3V power supply for PLL. |
| 47 | VSSA | GND | Ground for PLL. |
| 3, 10, 16, 24, 27, 34, 40 | VDD | PWR | 3.3V power supply for outputs. |
| 6, 11, 17, 23, 28, 37, 43 | VSS | GND | Ground for outputs. |

## Frequency Select Pins (FS_A, FS_B)

Host clock frequency selection is achieved by applying the appropriate logic levels to FS_A and FS_B inputs prior to VTT_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT_PWRGD# being sampled low by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS_A & FS_B input values. For all logic levels of FS_A and FS_B VTT_PWRGD# employs a one-shot functionality in that once a valid low on VTT_PWRGD# has been sampled low, all further VTT_PWRGD#, FS_A, and FS_B transitions will be ignored. Once "Test Clock Mode" has been invoked, all further FS_B transitions will be ignored and FS_A will asynchronously select between the Hi-Z and REF/N mode. Exiting test mode is accomplished by cycling power with FS_B in a high or low state.

**Table 1. Frequency Select Table (FS_A FS_B)**

| FS_A | FS_B | CPU | SRC | 3V66 | PCIF/PCI | REF0 | REF1 | USB/DOT |
|------|------|-----|-----|------|----------|------|------|---------|
| 0 | 0 | 100 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 0 | B6b7 | REF/N | REF/N | REF/N | REF/N | REF/N | REF/N | REF/N |
| 0 | 1 | 200 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 1 | 0 | 133 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 1 | B6b7 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |

**Table 2. Frequency Select Table (FS_A FS_B) SMBus Bit 5 of Byte 6 = 1**

| FS_A | FS_B | CPU | SRC | 3V66 | PCIF/PCI | REF0 | REF1 | USB/DOT |
|------|------|-----|-----|------|----------|------|------|---------|
| 0 | 0 | 200 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 0 | 1 | 400 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 1 | 0 | 266 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |

## Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

## Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 3*.

The block write and block read protocol is outlined in *Table 4* while *Table 5* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 3. Command Code Definition**

| Bit | Description |
|-----|-------------|
| 7 | 0 = Block read or block write operation, 1 = Byte read or byte write operation |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000' |

**Table 4. Block Read and Block Write Protocol**

| Block Write Protocol | | Block Read Protocol | |
|------|-------------|------|-------------|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 2:8 | Slave address – 7 bits | 2:8 | Slave address – 7 bits |
| 9 | Write = 0 | 9 | Write = 0 |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code – 8 bits '00000000' stands for block operation | 11:18 | Command Code – 8 bits '00000000' stands for block operation |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Byte Count – 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address – 7 bits |
| 29:36 | Data byte 1 – 8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 38:45 | Data byte 2 – 8 bits | 30:37 | Byte count from slave – 8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge from master |

**Table 4. Block Read and Block Write Protocol** (continued)

| | Block Write Protocol | | | Block Read Protocol |
|---|---|---|---|---|
| **Bit** | **Description** | | **Bit** | **Description** |
| .... | ...................... | | 39:46 | Data byte from slave – 8 bits |
| .... | Data Byte (N–1) –8 bits | | 47 | Acknowledge from master |
| .... | Acknowledge from slave | | 48:55 | Data byte from slave – 8 bits |
| .... | Data Byte N –8 bits | | 56 | Acknowledge from master |
| .... | Acknowledge from slave | | .... | Data byte N from slave – 8 bits |
| .... | Stop | | .... | Acknowledge from master |
| | | | .... | Stop |

**Table 5. Byte Read and Byte Write protocol**

| | Byte Write Protocol | | | Byte Read Protocol |
|---|---|---|---|---|
| **Bit** | **Description** | | **Bit** | **Description** |
| 1 | Start | | 1 | Start |
| 2:8 | Slave address – 7 bits | | 2:8 | Slave address – 7 bits |
| 9 | Write = 0 | | 9 | Write = 0 |
| 10 | Acknowledge from slave | | 10 | Acknowledge from slave |
| 11:18 | Command Code – 8 bits '100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed | | 11:18 | Command Code – 8 bits '100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed |
| 19 | Acknowledge from slave | | 19 | Acknowledge from slave |
| 20:27 | Data byte from master – 8 bits | | 20 | Repeat start |
| 28 | Acknowledge from slave | | 21:27 | Slave address – 7 bits |
| 29 | Stop | | 28 | Read = 1 |
| | | | 29 | Acknowledge from slave |
| | | | 30:37 | Data byte from slave – 8 bits |
| | | | 38 | Acknowledge from master |
| | | | 39 | Stop |

## Byte Configuration Map

**Byte 0: Control Register**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | Reserved | Reserved, set = 0 |
| 6 | 1 | PCIF PCI | PCI Drive Strength Override 0 = Force All PCI and PCIF Outputs to Low Drive Strength 1 = Force All PCI and PCIF Outputs to High Drive Strength |
| 5 | 0 | Reserved | Reserved, set = 0 |
| 4 | 0 | Reserved | Reserved, set = 0 |
| 3 | 1 | Reserved | Reserved, set = 1 |
| 2 | 1 | Reserved | Reserved, set = 1 |
| 1 | HW | FS_B | Power up latched value of FS_B pin |
| 0 | HW | FS_A | Power up latched value of FS_A pin |

**Byte 1: Control Register**

| Bit | @Pup | Name | Description |
|-----|------|------|-------------|
| 7 | 0 | SRCT<br>SRCC | Allow control of SRC during SW PCI_STP assertion<br>0 = Free Running, 1 = Stopped with SW PCI_STP |
| 6 | 1 | SRCT<br>SRCC | SRC Output Enable<br>0 = Disabled (three-state), 1 = Enabled |
| 5 | 1 | Reserved | Reserved, set = 1 |
| 4 | 1 | Reserved | Reserved, set = 1 |
| 3 | 1 | Reserved | Reserved, set = 1 |
| 2 | 1 | CPUT_ITP, CPUC_ITP | CPU_ITP Output Enable<br>0 = Disabled (three-state), 1 = Enabled |
| 1 | 1 | CPUT1, CPUC1 | CPU(T/C)1 Output Enable,<br>0 = Disabled (three-state), 1 = Enabled |
| 0 | 1 | CPUT0, CPUC0 | CPUT/C)0 Output Enable<br>0 = Disabled (three-state), 1 = Enabled |

**Byte 2: Control Register**

| Bit | @Pup | Name | Description |
|-----|------|------|-------------|
| 7 | 0 | SRCT, SRCC | SRCT/C Pwrdwn drive mode<br>0 = Driven in power down, 1 = three-state in power down |
| 6 | 0 | SRCT, SRCC | SRC Stop drive mode<br>0 = Driven in PCI_STP, 1 = three-state in power down |
| 5 | 0 | CPUT_ITP, CPUC_ITP | CPU(T/C)_ITP Pwrdwn drive mode<br>0 = Driven in power down, 1 = three-state in power down |
| 4 | 0 | CPUT1, CPUC1 | CPU(T/C)1 Pwrdwn drive mode<br>0 = Driven in power down, 1 = three-state in power down |
| 3 | 0 | CPUT0, CPUC0 | CPU(T/C)0 Pwrdwn drive mode<br>0 = Driven in power down, 1 = three-state in power down |
| 2 | 0 | Reserved | Reserved, set = 0 |
| 1 | 0 | Reserved | Reserved, set = 0 |
| 0 | 0 | Reserved | Reserved, set = 0 |

**Byte 3: Control Register**

| Bit | @Pup | Name | Description |
|-----|------|------|-------------|
| 7 | 1 | SW PCI STOP | SW PCI_STP Function<br>0= PCI_STP assert, 1= PCI_STP deassert<br>When this bit is set to 0, all STOPPABLE PCI, PCIF and SRC outputs will be stopped in a synchronous manner with no short pulses.<br>When this bit is set to 1, all STOPPED PCI,PCIF and SRC outputs will resume in a synchronous manner with no short pulses. |
| 6 | 1 | Reserved | Reserved |
| 5 | 1 | PCI5 | PCI5 Output Enable<br>0 = Disabled, 1 = Enabled |
| 4 | 1 | PCI4 | PCI4 Output Enable<br>0 = Disabled, 1 = Enabled |
| 3 | 1 | PCI3 | PCI3 Output Enable<br>0 = Disabled, 1 = Enabled |
| 2 | 1 | PCI2 | PCI2 Output Enable<br>0 = Disabled, 1 = Enabled |
| 1 | 1 | PCI1 | PCI1 Output Enable<br>0 = Disabled, 1 = Enabled |
| 0 | 1 | PCI0 | PCI0 Output Enable<br>0 = Disabled, 1 = Enabled |

**Byte 4: Control Register**

| Bit | @Pup | Name | Description |
|-----|------|------|-------------|
| 7 | 0 | USB_48 | USB_48MHz Drive Strength Control<br>0 = Low Drive Strength, 1 = High Drive Strength |
| 6 | 1 | USB_48 | USB_48MHz Output Enable<br>0 = Disabled, 1 = Enabled |
| 5 | 0 | PCIF2 | Allow control of PCIF2 with assertion of SW PCI_STP<br>0 = Free Running, 1 = Stopped with SW PCI_STP |
| 4 | 0 | PCIF1 | Allow control of PCIF1 with assertion of SW PCI_STP<br>0 = Free Running, 1 = Stopped with SW PCI_STP |
| 3 | 0 | PCIF0 | Allow control of PCIF0 with assertion of SW PCI_STP<br>0 = Free Running, 1 = Stopped with SW PCI_STP |
| 2 | 1 | PCIF2 | PCIF2 Output Enable<br>0 = Disabled, 1 = Enabled |
| 1 | 1 | PCIF1 | PCIF1 Output Enable<br>0 = Disabled, 1 = Enabled |
| 0 | 1 | PCIF0 | PCIF0 Output Enable<br>0 = Disabled, 1 = Enabled |

**Byte 5: Control Register**

| Bit | @Pup | Name | Description |
|-----|------|------|-------------|
| 7 | 1 | DOT_48 | DOT_48MHz Output Enable<br>0 = Disabled, 1 = Enabled |
| 6 | 1 | Reserved | Reserved |
| 5 | 0 | 3V66_3/VCH | 3V66_3/VCH Frequency Select<br>0 = 3V66 mode, 1 = VCH (48MHz) mode |
| 4 | 1 | 3V66_3/VCH | 3V66_3/VCH Output Enable<br>0 = Disabled, 1 = Enabled |
| 3 | 1 | Reserved | Reserved, set = 1 |
| 2 | 1 | 3V66_2 | 3V66_2 Output Enable<br>0 = Disabled, 1 = Enabled |
| 1 | 1 | 3V66_1 | 3V66_1 Output Enable<br>0 = Disabled, 1 = Enabled |
| 0 | 1 | 3V66_0 | 3V66_0 Output Enable<br>0 = Disabled, 1 = Enabled |

**Byte 6: Control Register**

| Bit | @Pup | Name | Description |
|-----|------|------|-------------|
| 7 | 0 | Reserved | Reserved, set = 0 |
| 6 | 0 | Reserved | Reserved, set = 0 |
| 5 | 0 | CPUC0, CPUT0<br>CPUC1, CPUT1<br>CPUT_ITP,CPUC_ITP | FS_A & FS_B Operation<br>0 = Normal, 1 = Test mode |
| 4 | 0 | SRCT, SRCC | SRCT/C Frequency Select<br>0 = 100Mhz, 1 = 200MHz |
| 3 | 0 | PCIF<br>PCI<br>3V66<br>SRCT,SRCC<br>CPUT_ITP,CPUC_ITP | Spread Spectrum Mode<br>0 = down (default), 1 = center |

**Byte 6: Control Register** (continued)

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 2 | 0 | PCIF<br>PCI<br>3V66<br>SRCT,SRCC<br>CPUT_ITP,CPUC_ITP | Spread Spectrum Enable<br>0 = Spread Off, 1 = Spread On |
| 1 | 1 | REF_1 | REF_1 Output Enable<br>0 = Disabled, 1 = Enabled |
| 0 | 1 | REF_0 | REF_0 Output Enable<br>0 = Disabled, 1 = Enabled |

**Byte 7: Control Register**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | Revision ID Bit 3 | Revision ID Bit 3 |
| 6 | 1 | Revision ID Bit 2 | Revision ID Bit 2 |
| 5 | 0 | Revision ID Bit 1 | Revision ID Bit 1 |
| 4 | 0 | Revision ID Bit 0 | Revision ID Bit 0 |
| 3 | 1 | Vendor ID Bit 3 | Vendor ID Bit 3 |
| 2 | 0 | Vendor ID Bit 2 | Vendor ID Bit 2 |
| 1 | 0 | Vendor ID Bit 1 | Vendor ID Bit 1 |
| 0 | 0 | Vendor ID Bit 0 | Vendor ID Bit 0 |

## Crystal Recommendations

The CY28405-3 requires a **Parallel Resonance Crystal**. Substituting a series resonance crystal will cause the CY28405-3 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

**Table 6. Crystal Recommendations**

| Frequency (Fund) | Cut | Loading | Load Cap | Drive (max.) | Shunt Cap (max.) | Motional (max.) | Tolerance (max.) | Stability (max.) | Aging (max.) |
|---|---|---|---|---|---|---|---|---|---|
| 14.31818 MHz | AT | Parallel | 20 pF | 0.1 mW | 5 pF | 0.016 pF | 50 ppm | 50 ppm | 5 ppm |

## Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

The following diagram shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is **not true**.
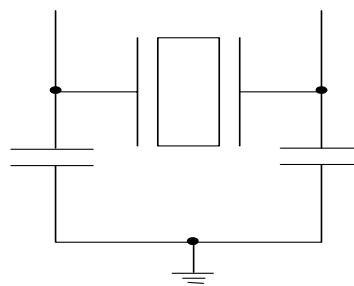


**Figure 1. Crystal Capacitive Clarification**

## Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.
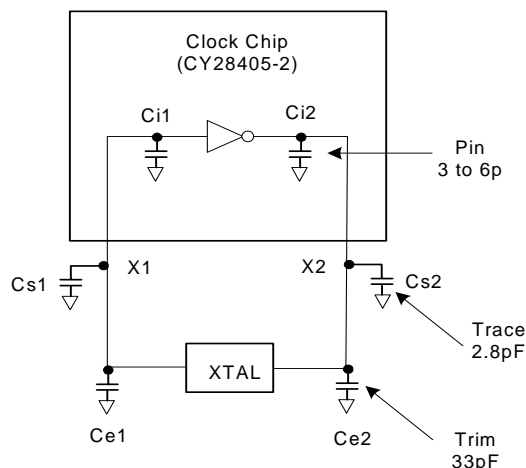


**Figure 2. Crystal Loading Example**

Use the following formulas to calculate the trim capacitor values from Ce1 and Ce2.

**Load Capacitance (each side)**

$$Ce = 2 * CL - (Cs + Ci)$$

**Total Capacitance (as seen by the crystal)**

$$CLe = \frac{1}{\left(\dfrac{1}{Ce1 + Cs1 + Ci1} + \dfrac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL .................................................. Crystal load capacitance

CLe ........................................Actual loading seen by crystal

.....................................using standard value trim capacitors

Ce ....................................................External trim capacitors

Cs ...........................................Stray capacitance (trace,etc)

Ci ............Internal capacitance (lead frame, bond wires etc)

## PD# (Power-down) Clarification

The PD# (Power Down) pin is used to shut off ALL clocks prior to shutting off power to the device. PD# is an asynchronous active LOW input. This signal is synchronized internally to the device powering down the clock synthesizer. PD# is an asynchronous function for powering up the system. When PD#

is low, all clocks are driven to a LOW value and held there and the VCO and PLLs are also powered down. All clocks are shut down in a synchronous manner so has not to cause glitches while transitioning to the low 'stopped' state.

**PD# – Assertion**

When PD# is sampled low by two consecutive rising edges of CPUC clock then all clock outputs (except CPU) clocks must be held low on their next high to low transition. CPU clocks must be hold with CPU clock pin driven high with a value of 2x Iref and CPUC undriven.

Due to the state of itnernal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete
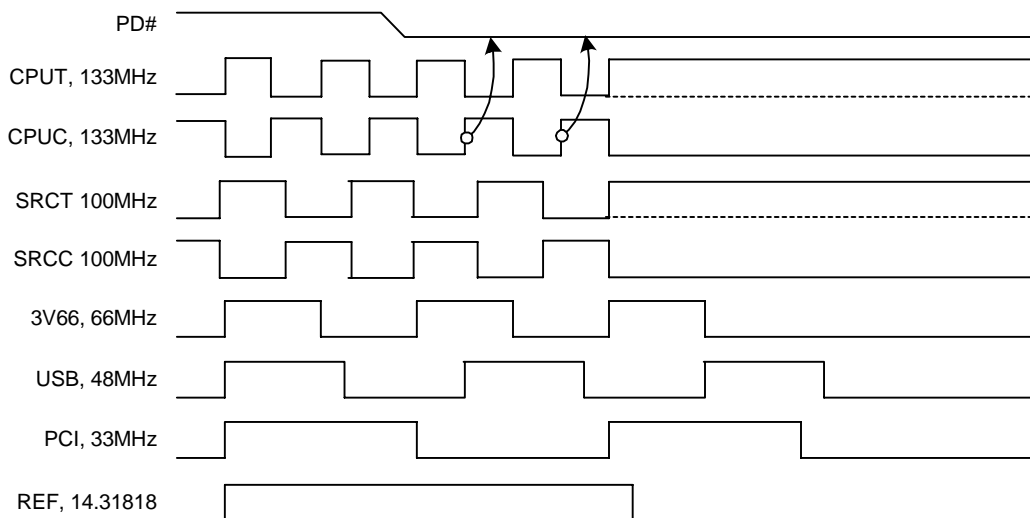
**Figure 3. Power-down Assertion Timing Waveforms**

**PD# Deassertion**

The power-up latency between PD# rising to a valid logic '1'
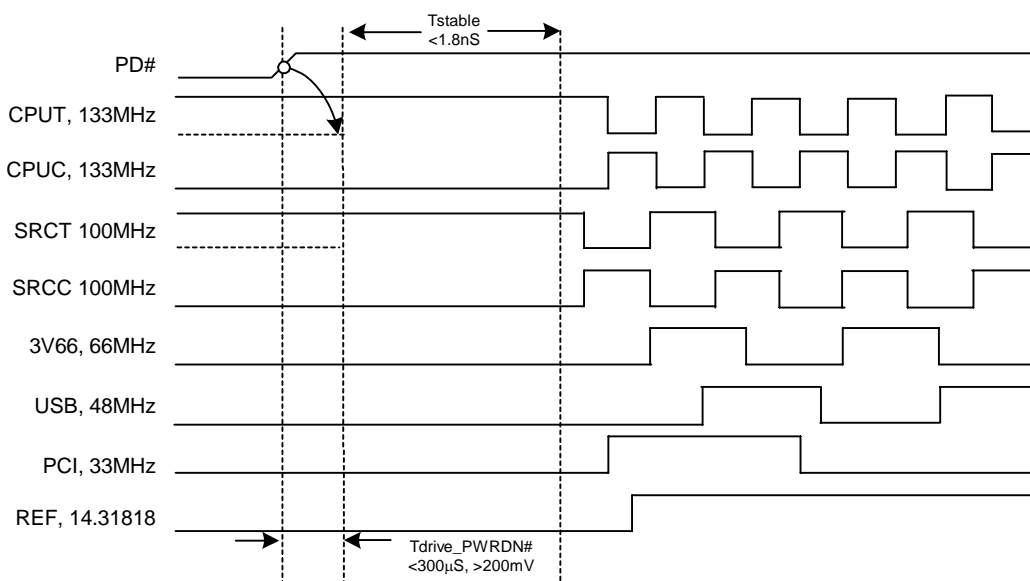level and the starting of all clocks is less than 3.0 ms.



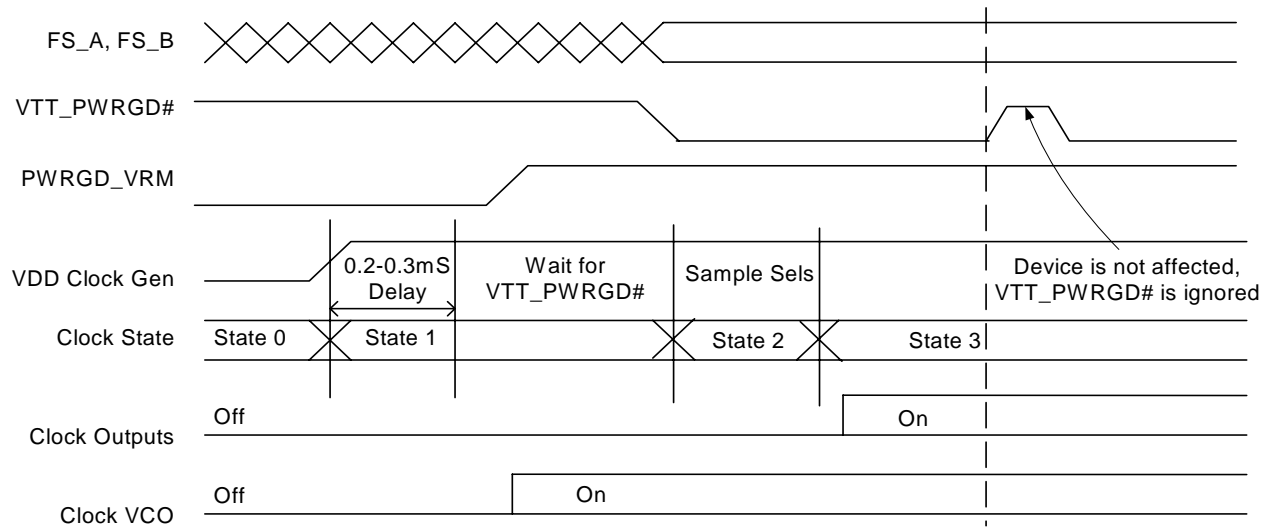**Figure 4. Power-down Deassertion Timing Waveforms**
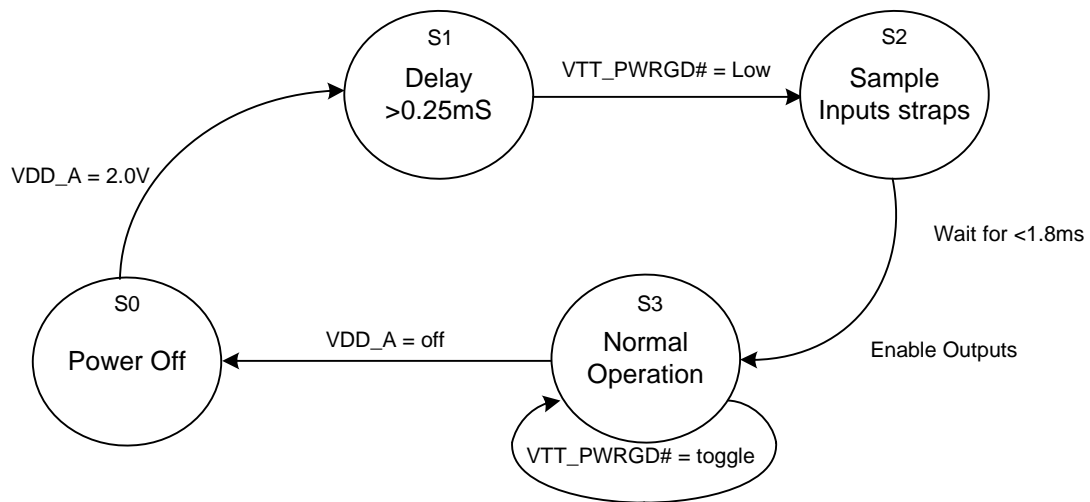
**Figure 5. VTT_PWRGD# Timing Diagram**



**Figure 6. Clock Generator Power-up/Run State Diagram**

## Absolute Maximum Conditions

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | −0.5 | 4.6 | V |
| $V_{DDA}$ | Analog Supply Voltage | | −0.5 | 4.6 | V |
| $V_{IN}$ | Input Voltage | Relative to $V_{SS}$ | −0.5 | $V_{DD}$ + 0.5 | VDC |
| $T_S$ | Temperature, Storage | Non-functional | −65 | +150 | °C |
| $T_A$ | Temperature, Operating Ambient | Functional | 0 | 70 | °C |
| $T_J$ | Temperature, Junction | Functional | – | 150 | °C |
| $ESD_{HBM}$ | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | – | V |
| $Ø_{JC}$ | Dissipation, Junction to Case | Mil-Spec 883E Method 1012.1 | 36.9 | | °C/W |
| $Ø_{JA}$ | Dissipation, Junction to Ambient | JEDEC (JESD 51) | 83.5 | | °C/W |
| UL–94 | Flammability Rating | At 1/8 in. | V–0 | | |
| MSL | Moisture Sensitivity Level | | 1 | | |

**Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

## DC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$, $V_{DDA}$ | 3.3 Operating Voltage | 3.3V ± 5% | 3.135 | 3.465 | V |
| $V_{ILI2C}$ | Input Low Voltage | SDATA, SCLK | – | 1.0 | V |
| $V_{IHI2C}$ | Input High Voltage | SDATA, SCLK | 2.2 | – | V |
| $V_{IL}$ | Input Low Voltage | | $V_{SS}$−0.5 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | Except SDATA and SCLK | 2.0 | $V_{DD}$+0.5 | V |
| $I_{IL}$ | Input Leakage Current | except Pull ups or Pull downs $0 < V_{IN} < V_{DD}$ | −5 | 5 | µA |
| $I_{ILI2C}$ | Forward Bias Current | $V_{DD}$ = OFF, SCLK and SDATA at 0V or 3.3V | −5 | 5 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 1 mA | – | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −1 mA | 2.4 | – | V |
| $I_{OZ}$ | High-Impedance Output Current | | −10 | 10 | µA |
| $C_{IN}$ | Input Pin Capacitance | | 2 | 5 | pF |
| $C_{OUT}$ | Output Pin Capacitance | | 3 | 6 | pF |
| $L_{IN}$ | Pin Inductance | | – | 7 | nH |
| $V_{XIH}$ | Xin High Voltage | | $0.7V_{DD}$ | $V_{DD}$ | V |
| $V_{XIL}$ | Xin Low Voltage | | 0 | $0.3V_{DD}$ | V |
| $I_{DD}$ | Dynamic Supply Current | At 200 MHz and all outputs loaded per *Table 9* and *Figure 7* | – | 350 | mA |
| $I_{PD}$ | Power-down Supply Current | PD# asserted, all differential outputs three-stated. | – | 2 | mA |

## AC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| **Crystal** | | | | | |
| $T_{DC}$ | XIN Duty Cycle | The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification | 47.5 | 52.5 | % |
| $T_{PERIOD}$ | XIN period | When Xin is driven from an external clock source | 69.841 | 71.0 | ns |
| $T_R / T_F$ | XIN Rise and Fall Times | Measured between $0.3V_{DD}$ and $0.7V_{DD}$ | – | 10.0 | ns |
| $T_{CCJ}$ | XIN Cycle to Cycle Jitter | As an average over 1-µs duration | – | 500 | ps |
| $L_{ACC}$ | Long-term Accuracy | Over 150 ms | | 300 | ppm |
| **CPU at 0.7V** | | | | | |
| $T_{DC}$ | CPUT and CPUC Duty Cycle | Measured at crossing point $V_{OX}$ | 45 | 55 | % |
| $T_{PERIOD}$ | 100-MHz CPUT and CPUC Period | Measured at crossing point $V_{OX}$ | 9.9970 | 10.003 | ns |
| $T_{PERIOD}$ | 133-MHz CPUT and CPUC Period | Measured at crossing point $V_{OX}$ | 7.4978 | 7.5023 | ns |
| $T_{PERIOD}$ | 200-MHz CPUT and CPUC Period | Measured at crossing point $V_{OX}$ | 4.9985 | 5.0015 | ns |
| $T_{SKEW}$ | Any CPUT/C to CPUT/C Clock Skew | Measured at crossing point $V_{OX}$ | – | 100 | ps |
| $T_{CCJ}$ | CPUT/C Cycle to Cycle Jitter | Measured at crossing point $V_{OX}$ | – | 125 | ps |
| $T_R / T_F$ | CPUT and CPUC Rise and Fall Times | Measured from Vol = 0.175 to Voh = 0.525V | 175 | 700 | ps |
| $T_{RFM}$ | Rise/Fall Matching | Determined as a fraction of $2^*(T_R - T_F)/(T_R + T_F)$ | – | 20 | % |
| $\Delta T_R$ | Rise Time Variation | | – | 125 | ps |
| $\Delta T_F$ | Fall Time Variation | | – | 125 | ps |
| $V_{HIGH}$ | Voltage High | Math averages *Figure 7* | 660 | 850 | mV |
| $V_{LOW}$ | Voltage Low | Math averages *Figure 7* | –150 | – | mV |
| $V_{OX}$ | Crossing Point Voltage at 0.7V Swing | | 250 | 550 | mV |
| $V_{OVS}$ | Maximum Overshoot Voltage | | – | $V_{HIGH} + 0.3$ | V |
| $V_{UDS}$ | Minimum Undershoot Voltage | | –0.3 | – | V |
| $V_{RB}$ | Ring Back Voltage | See *Figure 7*. Measure SE | – | 0.2 | V |
| **SRC** | | | | | |
| $T_{DC}$ | SRCT and SRCC Duty Cycle | Measured at crossing point $V_{OX}$ | 45 | 55 | % |
| $T_{PERIOD}$ | 100 MHz SRCT and SRCC Period | Measured at crossing point $V_{OX}$ | 9.9970 | 10.003 | ns |
| $T_{PERIOD}$ | 200 MHz SRCT and SRCC Period | Measured at crossing point $V_{OX}$ | 4.9985 | 5.0015 | ns |
| $L_{ACC}$ | Long Term Accuracy | Measured at crossing point $V_{OX}$ | – | 300 | ppm |
| $T_{CCJ}$ | SRCT/C Cycle to Cycle Jitter | Measured at crossing point $V_{OX}$ | – | 125 | ps |
| $T_R / T_F$ | SRCT and SRCC Rise and Fall Times | Measured from Vol= 0.175 to Voh = 0.525V | 175 | 700 | ps |
| $T_{RFM}$ | Rise/Fall Matching | Determined as a fraction of $2^*(T_R - T_F)/(T_R + T_F)$ | – | 20 | % |
| $\Delta T_R$ | Rise Time Variation | | – | 125 | ps |
| $\Delta T_F$ | Fall Time Variation | | – | 125 | ps |
| $V_{HIGH}$ | Voltage High | Math averages *Figure 7* | 660 | 850 | mv |
| $V_{LOW}$ | Voltage Low | Math averages *Figure 7* | –150 | – | mv |
| $V_{OX}$ | Crossing Point Voltage at 0.7V Swing | | 250 | 550 | mV |

## AC Electrical Specifications (continued)

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OVS}$ | Maximum Overshoot Voltage | | – | $V_{HIGH}$ + 0.3 | V |
| $V_{UDS}$ | Minimum Undershoot Voltage | | –0.3 | – | V |
| $V_{RB}$ | Ring Back Voltage | See *Figure 7.* Measure SE | – | 0.2 | V |
| **3V66** | | | | | |
| $T_{DC}$ | 3V66 Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| $T_{PERIOD}$ | Spread Disabled 3V66 Period | Measurement at 1.5V | 14.9955 | 15.0045 | ns |
| $T_{PERIOD}$ | Spread Enabled 3V66 Period | Measurement at 1.5V | 14.9955 | 15.0799 | ns |
| $T_{HIGH}$ | 3V66 High Time | Measurement at 2.0V | 4.9500 | – | ns |
| $T_{LOW}$ | 3V66 Low Time | Measurement at 0.8V | 4.5500 | – | ns |
| $T_R$ / $T_F$ | 3V66 Rise and Fall Times | Measured between 0.8V and 2.0V | 0.5 | 2.0 | ns |
| $T_{SKEW}$ | Any 3V66 to Any 3V66 Clock Skew | Measurement at 1.5V | – | 250 | ps |
| $T_{CCJ}$ | 3V66 Cycle-to-Cycle Jitter | Measurement at 1.5V | – | 250 | ps |
| **PCI/PCIF** | | | | | |
| $T_{DC}$ | PCI Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| $T_{PERIOD}$ | Spread Disabled PCIF/PCI Period | Measurement at 1.5V | 29.9910 | 30.0009 | ns |
| $T_{PERIOD}$ | Spread Enabled PCIF/PCI Period | Measurement at 1.5V | 29.9910 | 30.1598 | ns |
| $T_{HIGH}$ | PCIF and PCI High Time | Measurement at 2.0V | 12.0 | – | ns |
| $T_{LOW}$ | PCIF and PCI Low Time | Measurement at 0.8V | 12.0 | – | ns |
| $T_R$ / $T_F$ | PCIF and PCI Rise and Fall Times | Measured between 0.8V and 2.0V | 0.5 | 2.0 | ns |
| $T_{SKEW}$ | Any PCI clock to Any PCI Clock Skew | Measurement at 1.5V | – | 500 | ps |
| $T_{CCJ}$ | PCIF and PCI Cycle to Cycle Jitter | Measurement at 1.5V | – | 250 | ps |
| **DOT** | | | | | |
| $T_{DC}$ | Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| $T_{PERIOD}$ | Period | Measurement at 1.5V | 20.8271 | 20.8396 | ns |
| $T_{HIGH}$ | USB High Time | Measurement at 2.0V | 8.094 | 10.036 | ns |
| $T_{LOW}$ | USB Low Time | Measurement at 0.8V | 7.694 | 9.836 | ns |
| $T_R$ / $T_F$ | Rise and Fall Times | Measured between 0.8V and 2.0V | 1.0 | 2.0 | ns |
| $T_{CCJ}$ | Cycle to Cycle Jitter | Measurement at 1.5V | – | 350 | ps |
| $T_{SKEW}$ | Any 48 MHz to 48 MHz clock skew | Measurement @1.5V | – | 500 | ps |
| **USB** | | | | | |
| $T_{DC}$ | Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| $T_{PERIOD}$ | Period | Measurement at 1.5V | 20.8271 | 20.8396 | ns |
| $T_{HIGH}$ | USB High Time | Measurement at 2.0V | 8.094 | 10.036 | ns |
| $T_{LOW}$ | USB Low Time | Measurement at 0.8V | 7.694 | 9.836 | ns |
| $T_R$ / $T_F$ | Rise and Fall Times | Measured between 0.8V and 2.0V | 1.0 | 2.0 | ns |
| $T_{CCJ}$ | Cycle to Cycle Jitter | Measurement at 1.5V | – | 350 | ps |
| $T_{SKEW}$ | Any 48 MHz to 48 MHz Clock Skew | Measurement @1.5V | – | 500 | ps |
| **REF** | | | | | |
| $T_{DC}$ | REF Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| $T_{PERIOD}$ | REF Period | Measurement at 1.5V | 69.827 | 69.855 | ns |
| $T_R$ / $T_F$ | REF Rise and Fall Times | Measured between 0.8V and 2.0V | 1.0 | 4.0 | V/ns |

## AC Electrical Specifications (continued)

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{CCJ}$ | REF Cycle to Cycle Jitter | Measurement at 1.5V | – | 1000 | ps |
| $T_{SKEW}$ | Any REF to REF clock skew | Measurement @1.5V | – | 500 | ps |
| **ENABLE/DISABLE and SET-UP** | | | | | |
| $T_{STABLE}$ | Clock Stabilization from Power-up | | – | 1.8 | ms |
| $T_{SS}$ | Stopclock Set-up Time | | 10.0 | – | ns |
| $T_{SH}$ | Stopclock Hold Time | | 0 | – | ns |

**Table 7. Group Timing Relationship and Tolerances**

| Group | Conditions | Offset Min. | Offset Max. |
|---|---|---|---|
| 3V66 to PCI | 3V66 Leads PCI | 1.5ns | 3.5ns |

**Table 8. USB to DOT Phase Offset**

| Parameter | Typical | Value | Tolerance |
|---|---|---|---|
| DOT Skew | 0° | 0.0ns | 1000 ps |
| USB Skew | 180° | 0.0ns | 1000 ps |
| VCH SKew | 0° | 0.0ns | 1000 ps |

## Test and Measurement Set-up

**Table 9. Maximum Lumped Capacitive Output Loads**

| Clock | Max Load | Units |
|---|---|---|
| PCI Clocks | 30 | pF |
| 3V66 Clocks | 30 | pF |
| USB Clock | 20 | pF |
| DOT Clock | 10 | pF |
| REF Clock | 30 | pF |

### For Differential CPU and SRC Output Signals

The following diagram shows lumped test load configurations for the differential Host Clock Outputs.
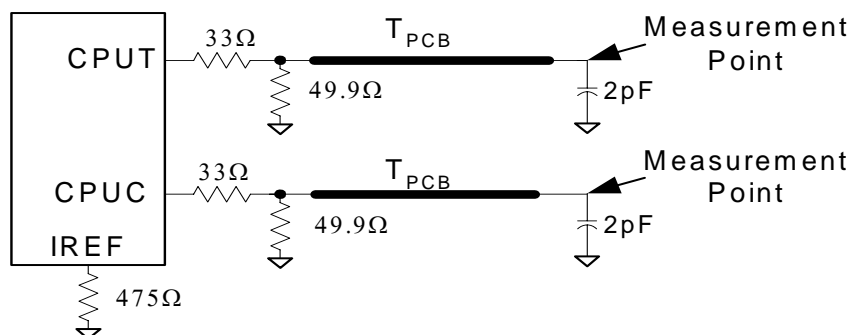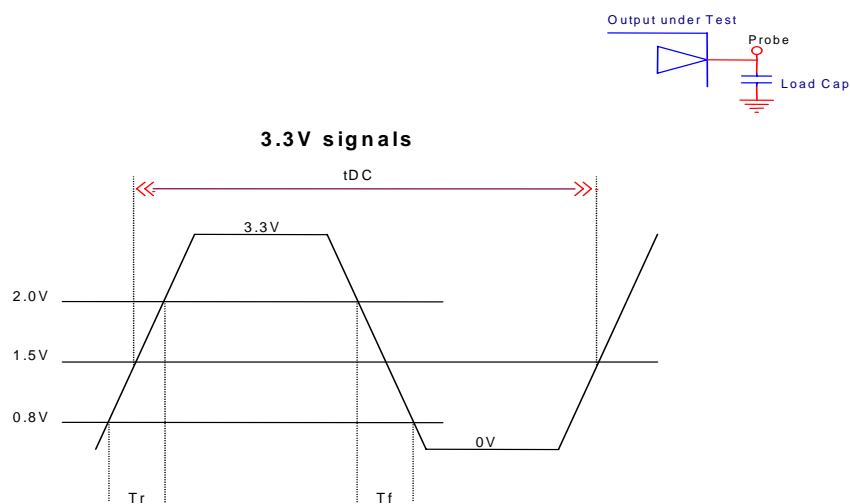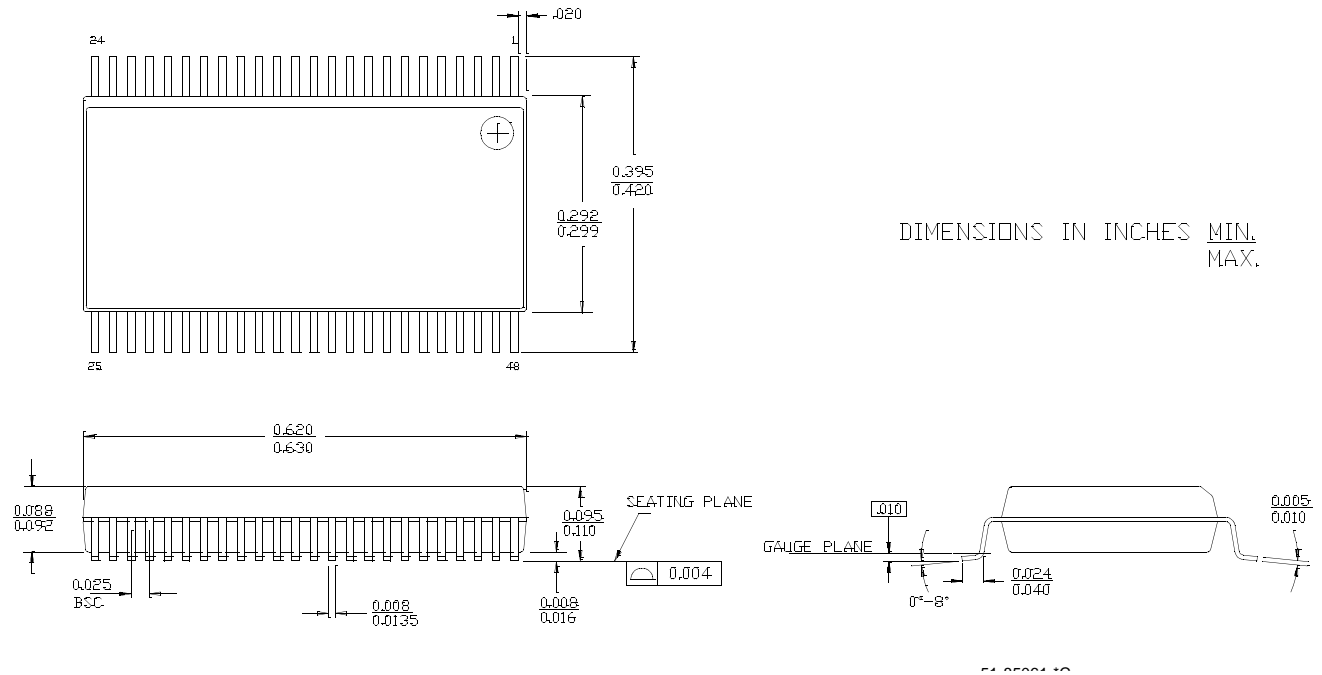


**Figure 7. 0.7V Load Configuration**

Output under Test
Probe
Load Cap

3.3V signals

tDC

3.3V

2.0V

1.5V

0.8V

0V

Tr                Tf

**Figure 8. Lumped Load For Single-ended Output Signals (for AC Parameters Measurement)**

**Table 10. CPU Clock Current Select Function**

| Board Target Trace/Term Z | Reference R, $I_{REF}$ – $V_{DD}$ (3*$R_{REF}$) | Output Current | $V_{OH}$ @ Z |
|---|---|---|---|
| 50 Ohms | $R_{REF}$ = 475 1%, $I_{REF}$ = 2.32mA | $I_{OH}$ = 6*$I_{REF}$ | 0.7V @ 50 |

## Ordering Information

| Part Number | Package Type | Product Flow |
|---|---|---|
| CY28405OC-3 | 48-pin SSOP | Commercial, 0° to 70°C |
| CY28405OC-3T | 48-pin SSOP – Tape and Reel | Commercial, 0° to 70°C |

## Package Drawing and Dimensions

**48-lead Shrunk Small Outline Package O48**



DIMENSIONS IN INCHES MIN.
MAX.