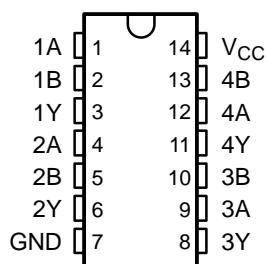


FEATURES

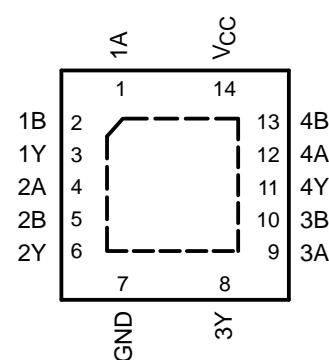
- Operates From 1.65 V to 3.6 V
- Max t_{pd} of 3 ns at 3.3 V
- ± 24 -mA Output Drive at 3.3 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17

- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

D, DGV, NS, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This quadruple 2-input positive-NAND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVC00 performs the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN - RGY	Tape and reel	SN74ALVC00RGYR	VA00
	SOIC - D	Tube	SN74ALVC00D	
		Tape and reel	SN74ALVC00DR	ALVC00
	SOP - NS	Tape and reel	SN74ALVC00NSR	ALVC00
	TSSOP - PW	Tape and reel	SN74ALVC00PWR	VA00
	TVSOP - DGV	Tape and reel	SN74ALVC00DGVR	VA00

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H

LOGIC DIAGRAM, EACH GATE (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74ALVC00

QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCES115G–JULY 1997–REVISED AUGUST 2004



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	4.6	V
V_O	Output voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current $V_I < 0$		-50	mA
I_{OK}	Output clamp current $V_O < 0$		-50	mA
I_o	Continuous output current		± 50	mA
	Continuous current through V_{CC} or GND		± 100	mA
θ_{JA}	Package thermal impedance	D package ⁽⁴⁾	86	°C/W
		DGV package ⁽⁴⁾	127	
		NS package ⁽⁴⁾	76	
		PW package ⁽⁴⁾	113	
		RGY package ⁽⁵⁾	47	
T_{stg}	Storage temperature range	-65	150	°C

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- This value is limited to 4.6 V maximum.
- The package thermal impedance is calculated in accordance with JESD 51-7.
- The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.65	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	
V_{IL}	Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0.8	
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65 \text{ V}$	-4	mA
		$V_{CC} = 2.3 \text{ V}$	-12	
		$V_{CC} = 2.7 \text{ V}$	-12	
		$V_{CC} = 3 \text{ V}$	-24	
I_{OL}	Low-level output current	$V_{CC} = 1.65 \text{ V}$	4	mA
		$V_{CC} = 2.3 \text{ V}$	12	
		$V_{CC} = 2.7 \text{ V}$	12	
		$V_{CC} = 3 \text{ V}$	24	
$\Delta t/\Delta V$	Input transition rise or fall rate		5	ns/V
T_A	Operating free-air temperature	-40	85	°C

- All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = -100 µA	1.65 V to 3.6 V	V _{CC}	- 0.2		V
	I _{OH} = -4 mA	1.65 V		1.2		
	I _{OH} = -6 mA	2.3 V		2		
		2.3 V		1.7		
	I _{OH} = -12 mA	2.7 V		2.2		
		3 V		2.4		
	I _{OH} = -24 mA	3 V		2		
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V		0.2		V
	I _{OL} = 4 mA	1.65 V		0.45		
	I _{OL} = 6 mA	2.3 V		0.4		
	I _{OL} = 12 mA	2.3 V		0.7		
	I _{OL} = 24 mA	2.7 V		0.4		
I _I	V _I = V _{CC} or GND	3.6 V		±5	µA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V		10	µA	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		750	µA	
C _i	V _I = V _{CC} or GND	3.3 V		4.5	pF	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

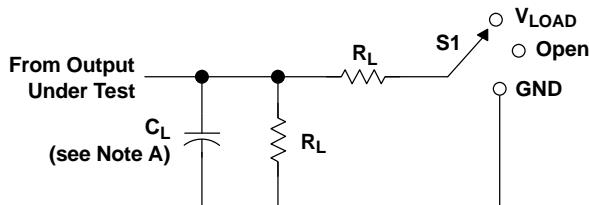
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V	UNIT			
			MIN	MAX	MIN	MAX				
t _{pd}	A or B	Y	1	4.4	1	2.8	3.2	1	3	ns

OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
		TYP	TYP	TYP		
C _{pd}	Power dissipation capacitance per gate	C _L = 0 pF, f = 10 MHz	20	21	23	pF

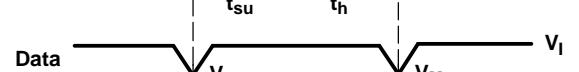
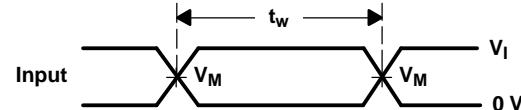
PARAMETER MEASUREMENT INFORMATION



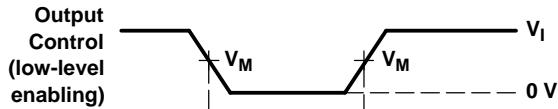
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

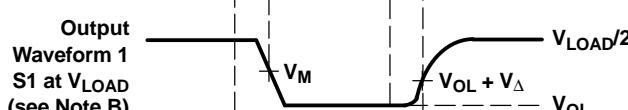
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



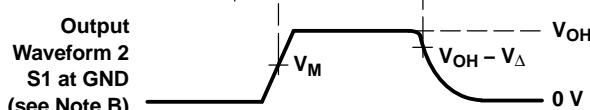
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ALVC00D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00DGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00DGVR4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00DGVRG4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC00RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74ALVC00RGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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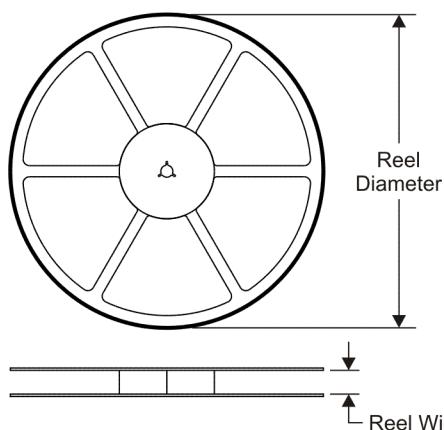
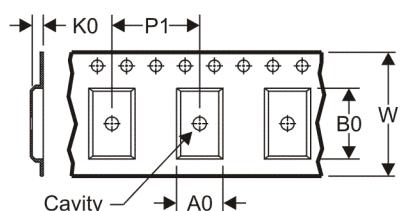
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OTHER QUALIFIED VERSIONS OF SN74ALVC00 :

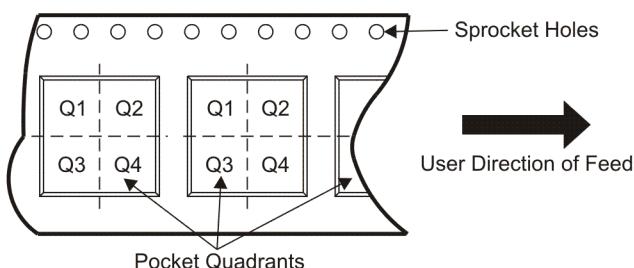
- Automotive: [SN74ALVC00-Q1](#)
- Enhanced Product: [SN74ALVC00-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A_0	Dimension designed to accommodate the component width
B_0	Dimension designed to accommodate the component length
K_0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P_1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A_0 (mm)	B_0 (mm)	K_0 (mm)	P_1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVC00DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74ALVC00DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ALVC00NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74ALVC00PWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74ALVC00RGYR	VQFN	RGY	14	3000	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

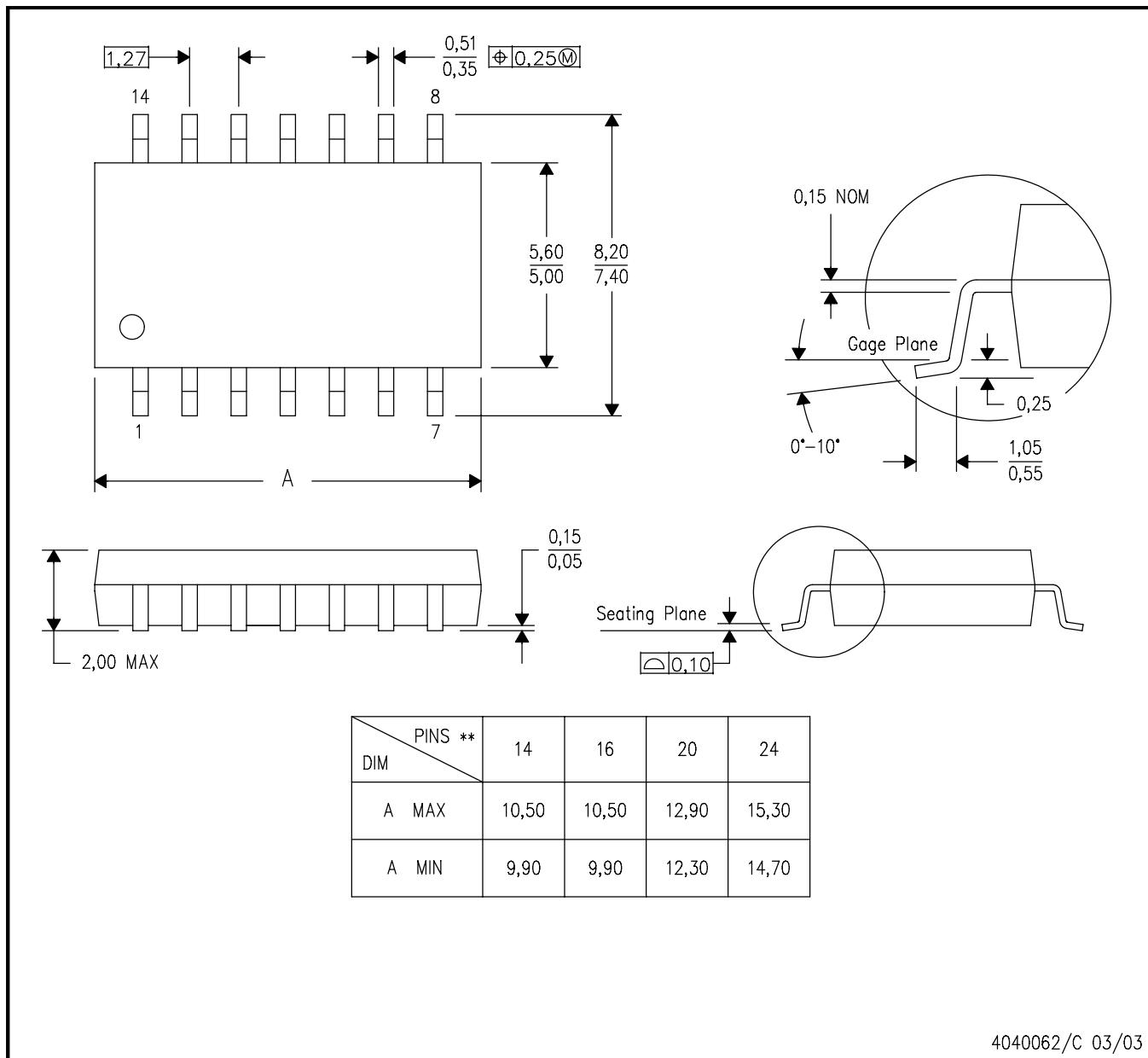
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVC00DGVR	TVSOP	DGV	14	2000	346.0	346.0	29.0
SN74ALVC00DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74ALVC00NSR	SO	NS	14	2000	346.0	346.0	33.0
SN74ALVC00PWR	TSSOP	PW	14	2000	346.0	346.0	29.0
SN74ALVC00RGYR	VQFN	RGY	14	3000	190.5	212.7	31.8

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



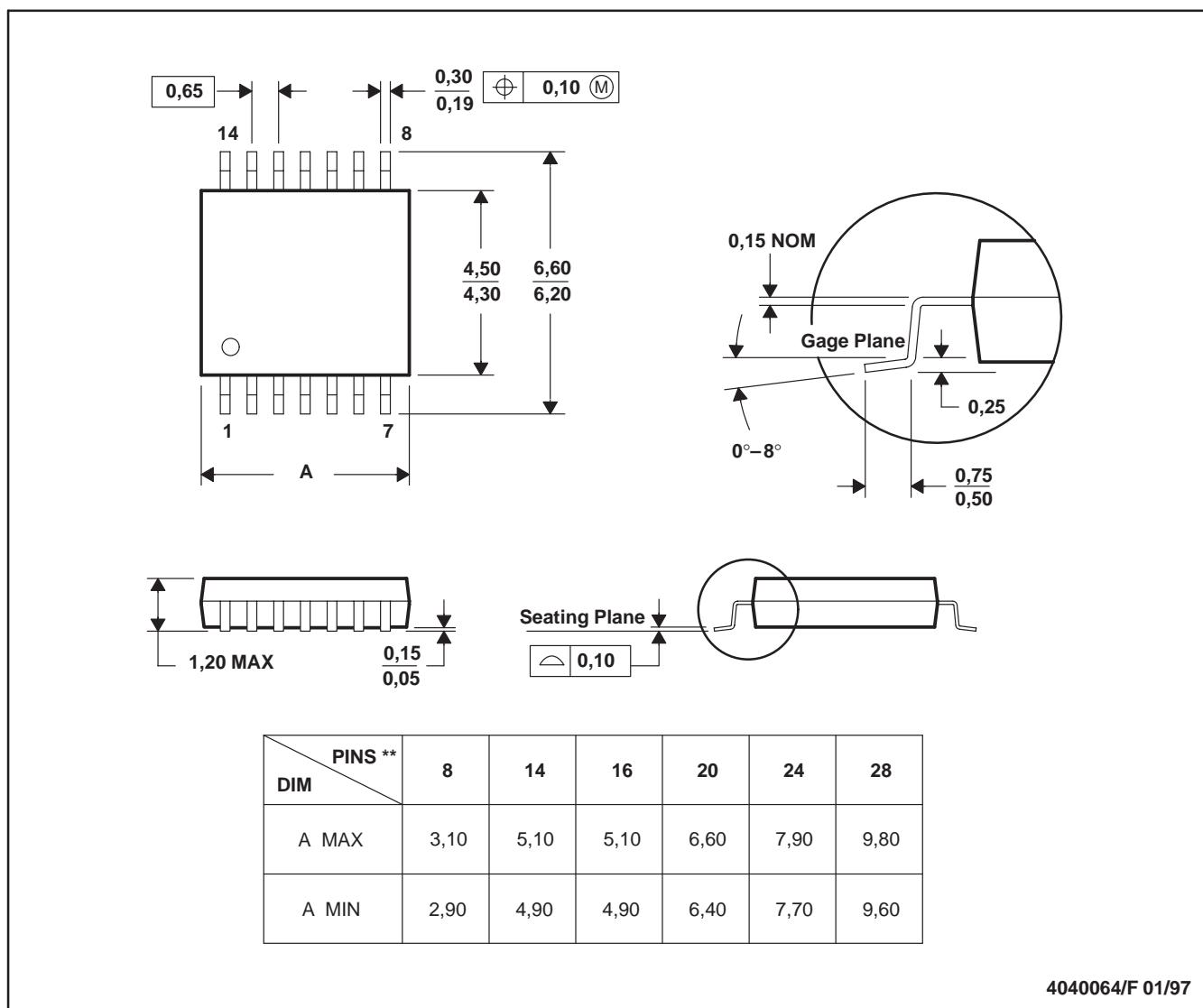
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

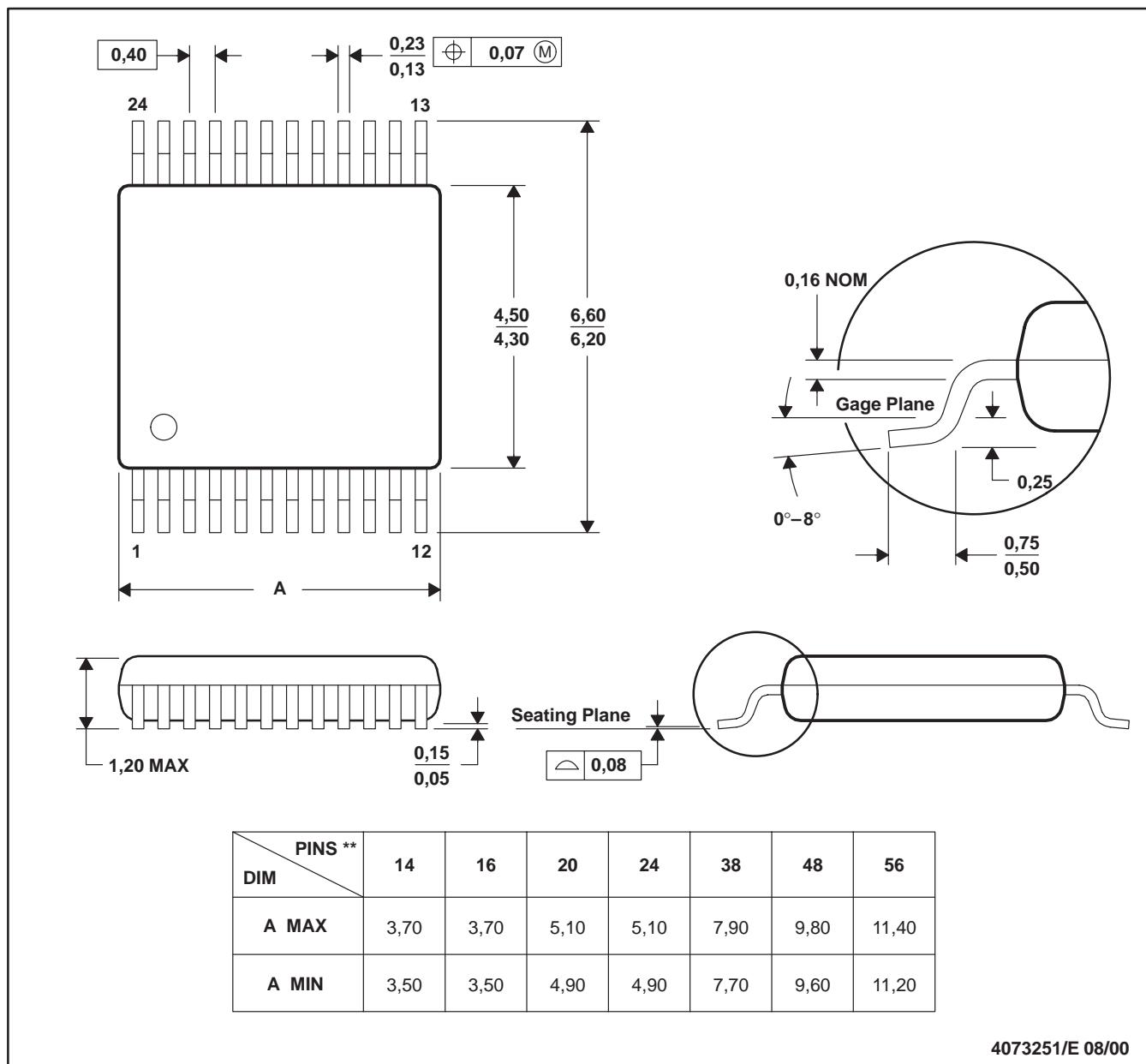


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-153

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

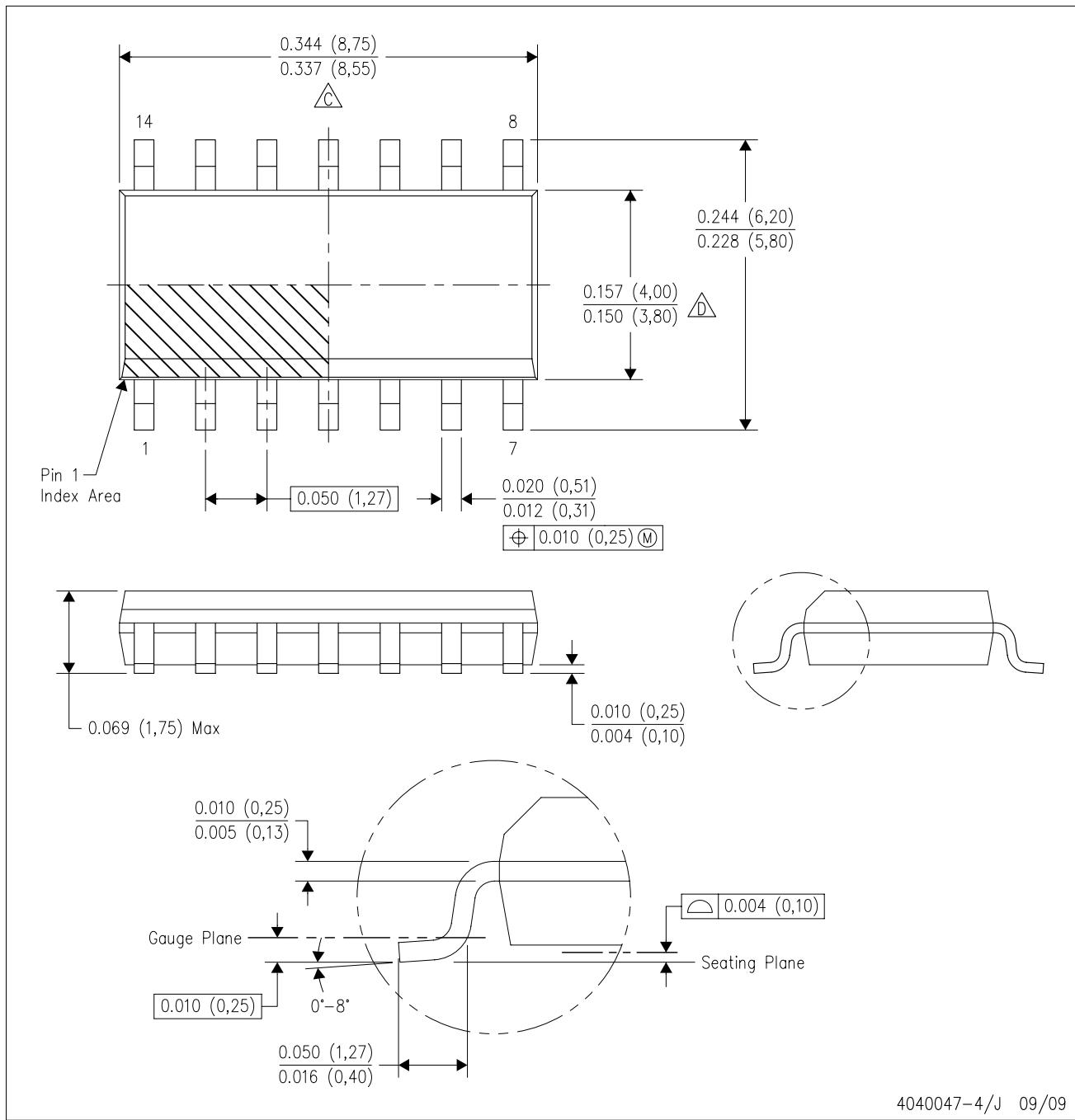
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

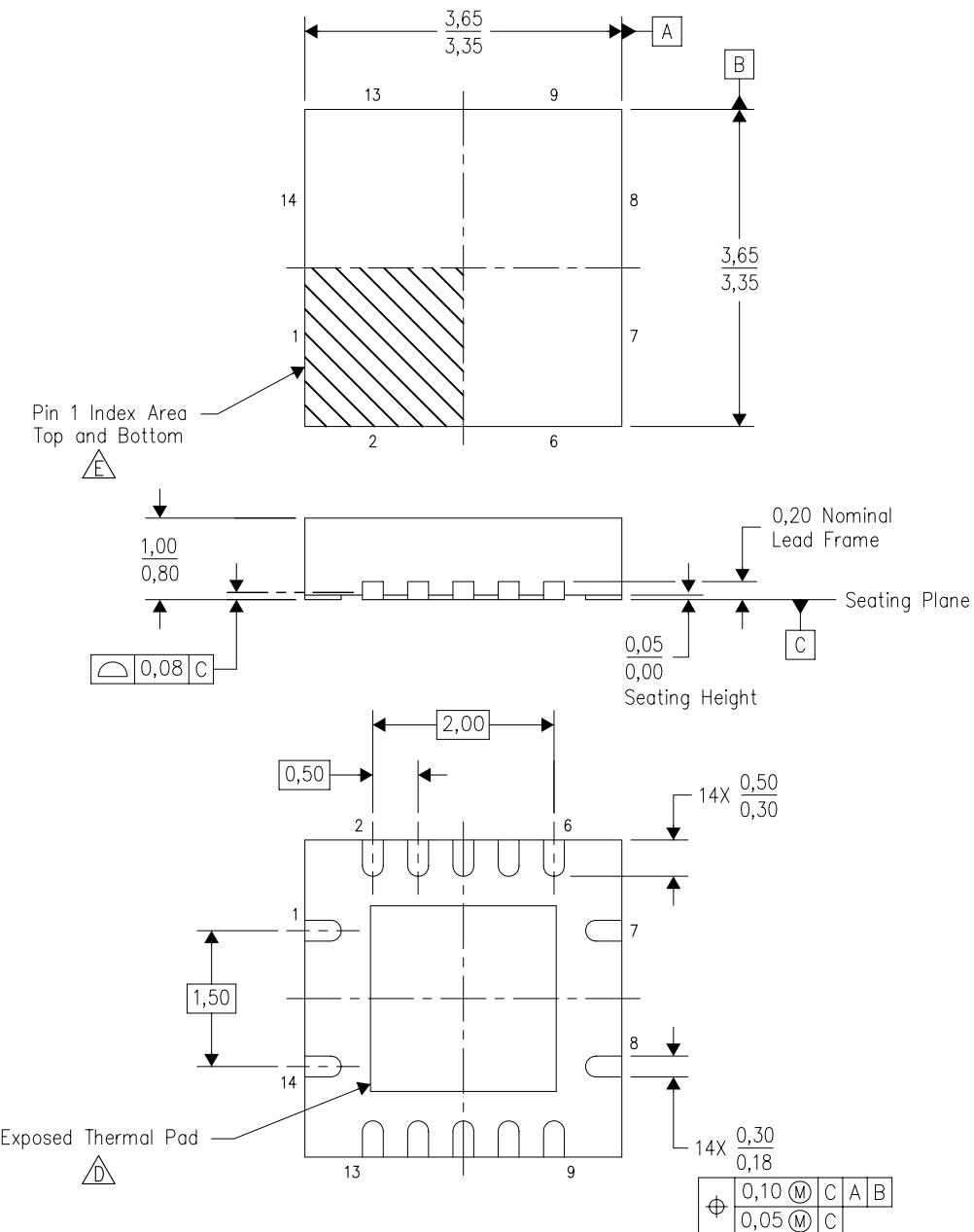
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AB.

MECHANICAL DATA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-2/H 06/2009

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice

C. QFN (Quad Flatpack No-Lead) package configuration

QIN (Quad Flatpack No-Lead) package configuration.

The package thermal pad must be soldered to the board for thermal and mechanical performance. See the [Pad Layout Rule Sheet](#) for detailed information on the pad layout dimensions.

See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

 Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.

The Pin 1 identifiers are either a molded, marked, or metal feature.

F. Package complies to JEDEC MO-241 variation BA.

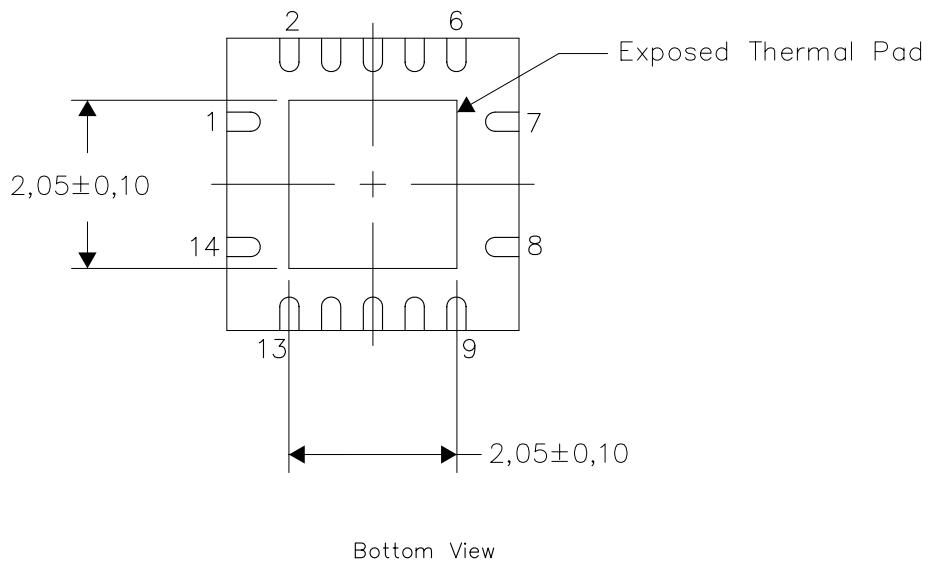


THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

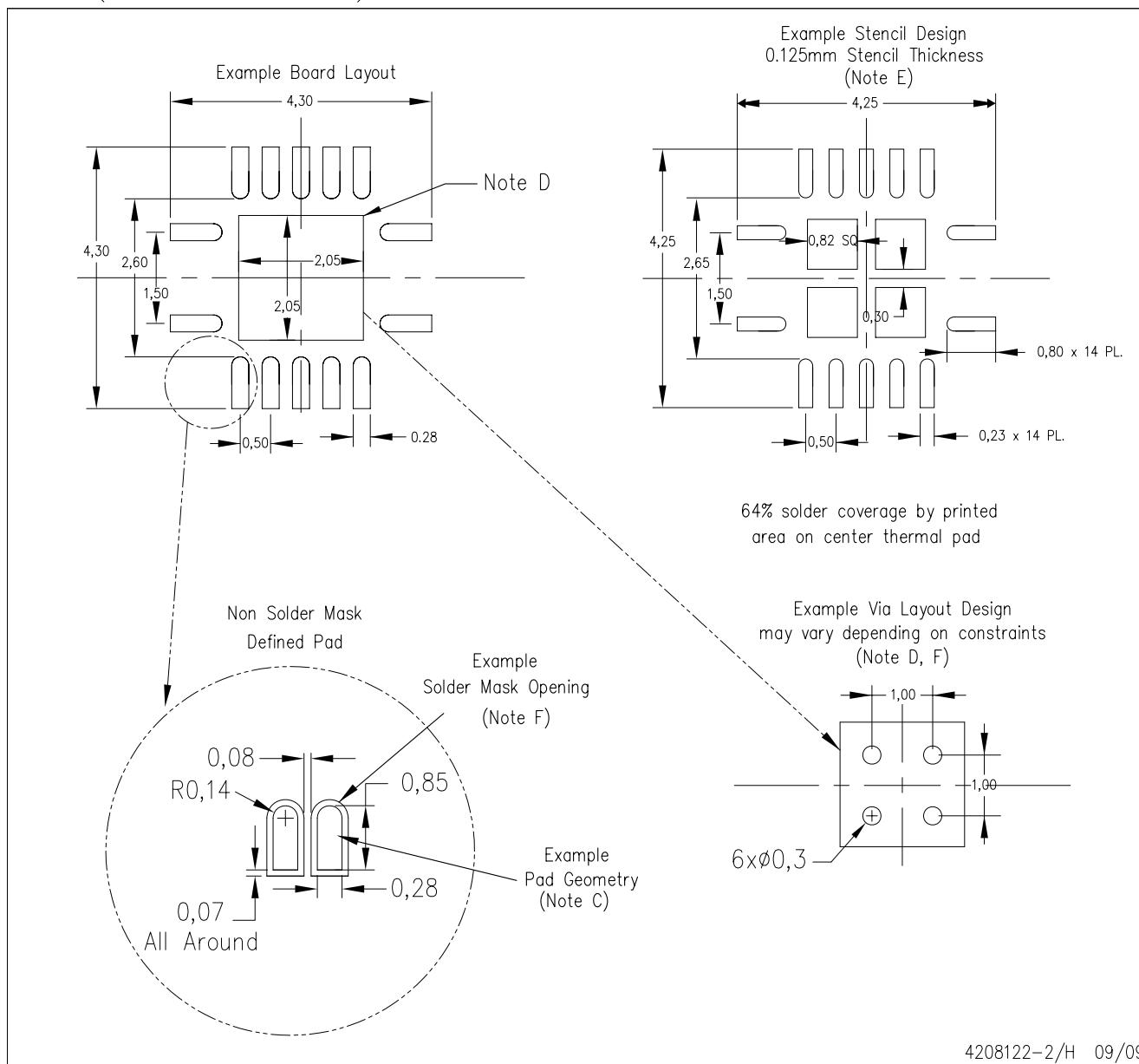


Bottom View

NOTES: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (S-PVQFN-N14)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.