True Single Chip Multi-Mode Wireless Power Receiver IC

IDTP9020

Preliminary Datasheet Short Form

Features

- Single Chip Solution for Wireless Power Consortium (WPC) "Qi" compliant wireless power receiver designs
- Designed to meet WPC specifications, with up to 7.5W power delivery in proprietary mode
- Integrated Synchronous Full-Bridge Rectifier
- Integrated Synchronous Buck Converter
- Embedded MCU, ROM, RAM, & ADC
- Integrated USB Adaptor Switches for USB charging
- Supports proprietary power transmission protocols in addition to Qi with dynamic switching capability
- Closed Loop Power Transfer control between Base Station and Mobile Device
- Proprietary Base to Mobile Communication for Authentication
- Programmable option for added security and encryption up to 64 bit for 2-way authentication
- Multi-layer advanced Foreign Object Detection (FOD) for safety
- Over Temperature, Voltage, Current Protection
- Thermal Loop Control
- Compatible with all WPC receiver coils including proprietary and PCB based coils
- Power Good Status Pin
- Open Drain Coupling LED indicator Outputs
- I²C Interface
- Packages 7x7-56 TQFN, 4.6 x 4.9 WLCSP

	WPC Mode	Proprietary Modes
Output Power	5W	7.5W
Authentication	OFF	ON
Foreign Object Detection	1,2	1,2,3,4
Channel Communication	RX→TX	RX→TX & TX→RX

Description

The IDTP9020 is a highly-integrated single-chip, multi-mode wireless power receiver IC. The device enables conversion of AC power provided via an inductively coupled coil (from a compatible wireless transmitter) into a regulated 5V output voltage, which can be used to power devices or supply the charger input in mobile applications. The IDTP9020 integrates a high-efficiency synchronous full bridge rectifier, high efficiency synchronous buck converter, and control circuits used to modulate the load to transmit WPC compliant message packets to the transmitter station to optimize power delivery. In WPC mode, power delivery is limited to 5W in accordance with the Qi specification, while up 7.5W power may be delivered in proprietary modes.

The IDTP9020 may be operated in proprietary modes where additional enhanced functions such as multi layered Foreign Object Detection (FOD), 2-way secure authentication, and higher-efficiency control algorithms may be employed.

The device includes over temperature/voltage/current protection and up to four levels of advanced Foreign Object Detection (FOD) (when used with IDT's IDTP9030 transmitter) to ensure safety of the base station and mobile device from over-heating in the presence of a metallic foreign objects. Power transfer fault conditions are managed by the embedded MCU and controls status LEDs indicate operating and fault modes.

Applications

- WPC Compliant or Non-WPC Wireless Receiver Solutions for Mobile Applications
- Mobile and Smart Phones
- Tablets, MIDs
- Digital Camera, MP3 Player
- Remote controls
- GPS, and more….

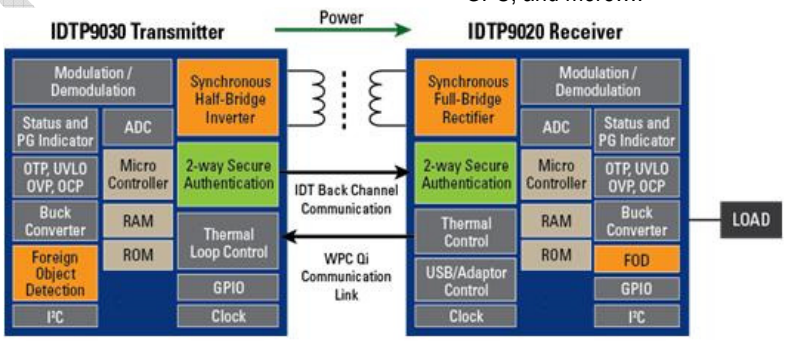

Figure 1 - IDT Power Transfer/Data Communication System Block Diagram

ABSOLUTE MAXIMUM RATINGS

Table 1: Absolute Maximum Ratings Summary

Symbol	Description	Value	Units
INP, INM, Z_{REFP}, Z_{REFM}, A_{CMP}, A_{CMM}	Input voltage	-1 to 24V	V
T_J	Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at Leads)	300	°C
ESD	ESD rating, Human Body Model	+/- 2000	V

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)}-T_A)/\theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

Table 2: Package Thermal Resistivity

Symbol	Description	Value	Units
Θ_{JA}	Maximum Thermal Resistance (TQFN 7 x 7)	TBD	°C/W
Θ_{JA}	Maximum Thermal Resistance (WLCSP-TBD)	TBD	°C/W

This thermal rating was calculated based on a JEDEC standard 4-layer board with dimensions 4in x 4.5in in still air conditions. Actual thermal resistance will be affected by PCB size, solder joint quality, PCB layer count, copper thickness, air flow, altitude, and other unlisted variables.

IDTP9020

SPECIFICATION TABLE

T_J = -40 to +125°C, unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
Synchronous Full Bridge Rectifier (SFBR)						
$V_{IN,AC}$	Input voltage to SFBR	f_{PWM} = 110-205kHz			+24	V
I_{RECT}	Current from rectified voltage pin				1.5	A
V_{DSMAX}	Maximum drain to source voltage on SFBR switch	f_{PWM} = 110-205kHz			24	V
$R_{LOAD,MIN}$	Minimum on-chip load	f_{PWM} = 110-205kHz	1		5	kΩ
Modulation						
RX Coil A						
C_{MOD_AC}	AC modulation capacitor			47		nF
$R_{DS-ON,CMOD\_AC}$	Mosfet on resistance driving C_{MOD}		0.5	2	4	Ω
RX Coil B						
C_{MOD_AC}	AC modulation capacitor			47		nF
$R_{DS-ON,CMOD\_AC}$	Mosfet on resistance driving C_{MOD}		0.5	2	4	Ω
RX Coil C						
C_{MOD}	AC modulation capacitor			47		nF
$R_{DS-ON,CMOD}$	Mosfet on resistance driving C_{MOD}		0.5	2	4	Ω
RX Coil D						
C_{MOD}	AC modulation capacitor			22		nF
$R_{DS-ON,CMOD}$	Mosfet on resistance driving C_{MOD}		0.5	2	4	Ω
Analog to Digital Converter						
N	Resolution			12		Bit
f_{SAMPLE}	Sampling Rate				125	kSPS
Channel	# of Channel		8			
ADC_{CLK}	Sampling Rate				2	MHz
INL	Integral Non Linearity				±2	LSB
DNL	Differential Non Linearity				±2	LSB
$V_{IN,FS}$	Full scale Input voltage		0		TBD	V
$I_{QUIESENT}$	Quiesent current				600	µA
V_{REF}	Reference voltage			TBD		V
PSRR	Power Supply Rejection		TBD			dB

SPECIFICATION TABLE (CONTINUED)

T_J = -40 to +125°C, unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
OVP/OCP/UVLO						
$V_{RECT,OVP}$	Over voltage protection for rectified voltage	I_{RECT}=0 to 1.5A			20	V
$V_{RECT,UVLO}$						V
	Rising				6.5	V
	Falling		6			V
DCDC Converter						
V_{IN}	Input voltage				20	V
V_{OUT}	Output voltage			5		V
ΔV_{OUT} /V_{OUT}	Output voltage accuracy		-5		5	%
I_{OUT}	Output current				1.5	A
Fsw	Switching frequency			3		MHz
Low Drop Out Regulator						
LDO2P5V						
V_{IN}	Input voltage			5		V
V_{OUT}	Output voltage			2.5		V
I_{OUT}	Output current				200	mA
ΔV_{OUT} /V_{OUT}	Output voltage accuracy		-5		+5	%
LDO5V						
V_{IN}	Input voltage				20	V
V_{OUT}	Output voltage			5		V
ΔV_{OUT} /V_{OUT}	Output voltage accuracy		-5		+5	%
I_{OUT}	Output current			30	90	mA
Thermal Shutdown						
T_{SD}	Thermal shutdown		Threshold Rising	140		^{O}C
			Threshold Falling	110		^{O}C
Microcontroller						
F_{CLOCK}	Clock frequency				40	MHz
F_{CLOCK} Accuracy	Clock accuracy		TBD			%
V_{IN}	Input voltage			2.5		V

SPECIFICATION TABLE (CONTINUED)

T_J = -40 to +125°C, unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
SCL, SDA (I^2C Interface)						
f_{SCL}	Clock Frequency		0		400	kHz
t_{LOW}	Clock Low Period		1.3			µS
t_{HIGH}	Clock High Period		0.6			µS
$t_{HD,STA}$	Hold Time (Repeated) for START Condition		0.6			µS
$t_{SU:STA}$	Set-up Time for Repeated START Condition		0.6			µs
$t_{SU:DAT}$	Data Setup Time		100			ns
$t_{HD:DAT}$	Data Hold Time				0.9	µs
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3			µs
t_R	Rise Time of Both SDA and SCL Signals		20 + 0.1 C_B		300	ns
t_F	Fall Time of Both SDA and SCL Signals		20 + 0.1 C_B		300	ns
T_{SP}	Spike Pulse Widths Suppressed by Input Filter		0		50	ns
C_B	Capacitive Load for Each Bus Line				400	pF
C_{BIN}	SCL, SDA Input Capacitance				60	pF
V_{IL}	Input Threshold Low	(Note 1)			0.4	V
V_{IH}	Input Threshold High	(Note 1)	1.4			V
I_I	Input Leakage Current		-1.0		1.0	µA
V_{OL}	Output Logic Low (SDA)	I_{PD}= 4mA (Note 1)			0.4	V
I_{PD}	SCL, SDA Pull-down Current	V_{BAT}=4.2V V_{PIN}=0.4V		0.2		uA
t_{SLEEP}	Bus Low Timeout	(Note 3)	1.5		2.2	S

IDTP9020

PIN CONFIGURATION & DESCRIPTION

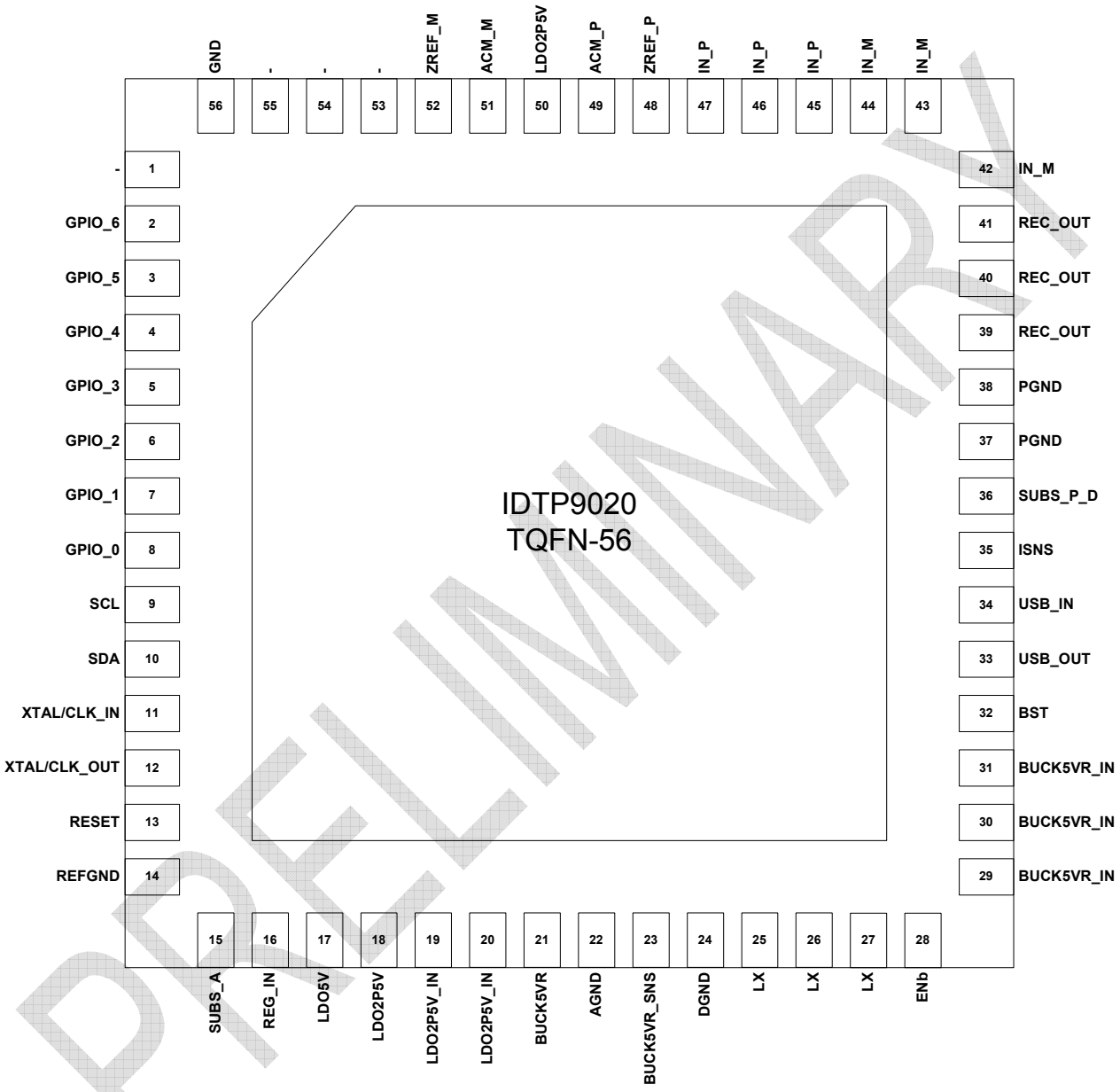

Figure 2: IDTP9020 Pin Configuration

IDTP9020

Pin # (TQFN)	Name	Absolute Max (V)	Type	Function
1	NC		-	
2	GPIO_6		I/O	General purpose input/output.
3	GPIO_5		I/O	General purpose input/output.
4	GPIO_4		I/O	General purpose input/output.
5	GPIO_3		I/O	General purpose input/output.
6	GPIO_2		I/O	General purpose input/output.
7	GPIO_1		I/O	General purpose input/output.
8	GPIO_0		I/O	General purpose input/output.
9	SCL		I	System Clock
10	SDA		I/O	Data bus
11	XTAL/CLK_IN		I	Crystal or clock input.
12	XTAL/CLK_OUT		O	Crystal or clock output.
13	RESET		I	Chip reset, active high.
14	REFGND		I	Signal ground connection.
15	SUBS_A		I	Analog substrate ground
16	REG_IN		I	Regulator power supply Input. Connect 1µF capacitor between this pin and ground.
17	LDO5V		O	Regulated output.
18	LDO2P5V		O	Regulated output.
19	LDO2P5V_IN		I	Regulator power supply input. Share 1µF input cap with LDO2P5V_IN.
20	LDO2P5V_IN		I	Regulator power supply input. Share 1µF input cap with LDO2P5V_IN.
21	BUCK5VR		I	Power and Digitlal supply input.
22	AGND		I	Analog ground connection.
23	DGND		I	Digital ground connection.
24	BUCK5VR_SNS		I	Feedback from output capacitor of buck converter.
25	LX		O	Switch Node of buck converter. Connects to one of the inductor's terminals.
26	LX		O	Switch Node of buck converter. Connects to one of the inductor's terminals.
27	LX		O	Switch Node of buck converter. Connects to one of the inductor's terminals.
28	ENb		I	Active-Low charger Enable pin. Charger is suspended and placed in low current (sleep) mode when pulled high. Tie low for stand alone mode.
29	BUCK5VR_IN		I	Buck converter power supply input.
30	BUCK5VR_IN		I	Buck converter power supply input.
31	BUCK5VR_IN		I	Buck converter power supply input.
32	BST		I	Bootstrap cap for BUCK converter gate drive supply.
33	USB_OUT		O	USB or 5V adaptor output.
34	USB_IN		I	USB or 5V adaptor input.
35	ISNS		?	Current sense.
36	SUBS_P		I	Power substrate ground
37	SUBS_D		I	Digital substrate ground
38	NC		-	
39	REC_OUT		O	Rectified output.
40	REC_OUT		O	Rectified output.
41	REC_OUT		O	Rectified output.
42	IN_M		I	Negative inductor input.
43	IN_M		I	Negative inductor input.
44	IN_M		I	Negative inductor input.
45	IN_P		I	Positive inductor input.
46	IN_P		I	Positive inductor input.
47	IN_P		I	Positive inductor input.
48	ZREF_M		I	AC clamp, negative end
49	ACM_M		I	AC modulation input, negative end.
50	ACM_P		I	AC modulation input, positive end.
51	ZREF_P		I	AC clamp, positive end.
52	LDO2P5V		I	2.5V output (Do not load).
53	NC		-	
54	NC		-	
55	NC		-	
56	GND		I	Signal ground connection.

APPLICATION DIAGRAMS

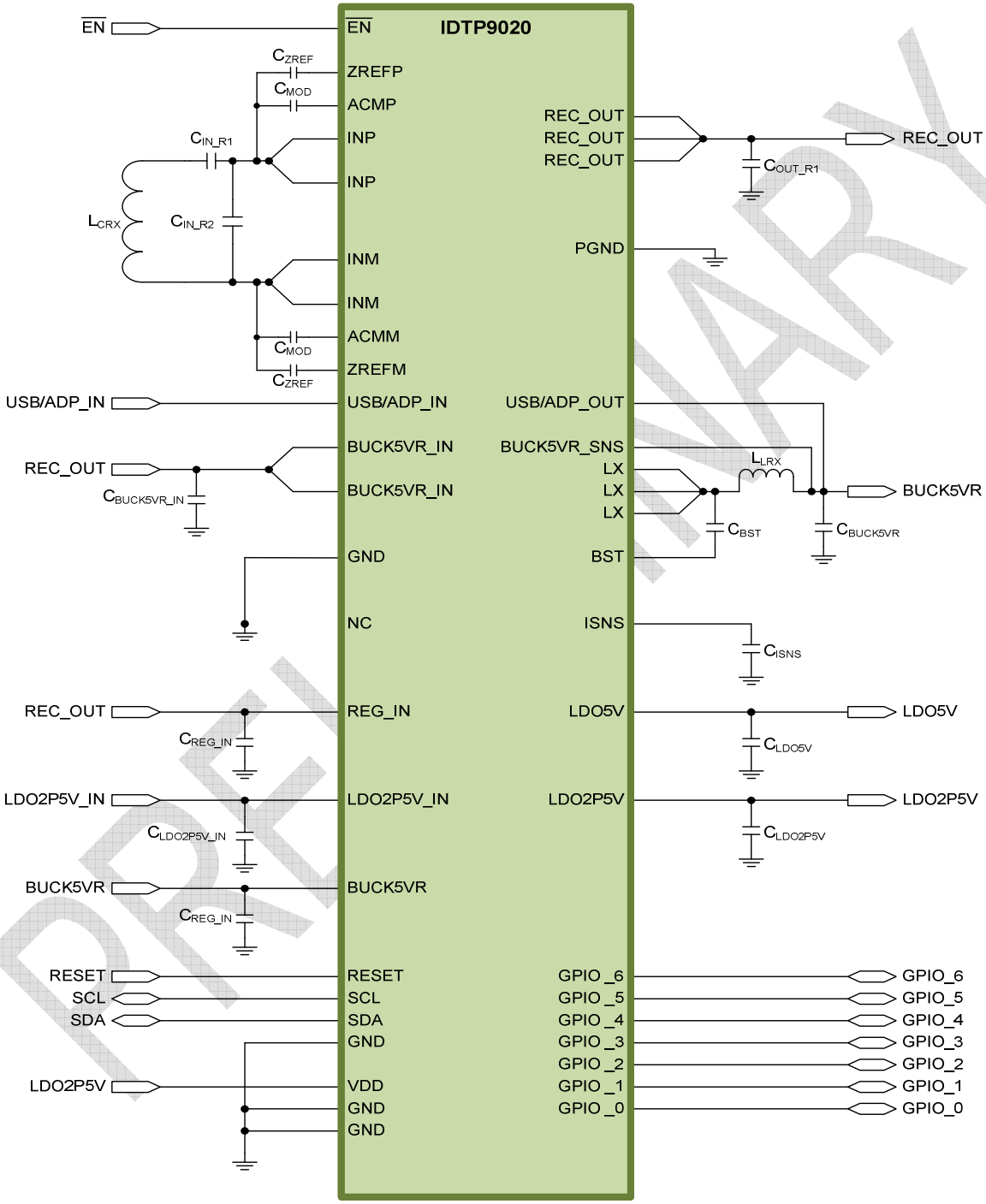

Figure3: IDTP9020 Applications Diagram

IDTP9020

SYSTEM DIAGRAM

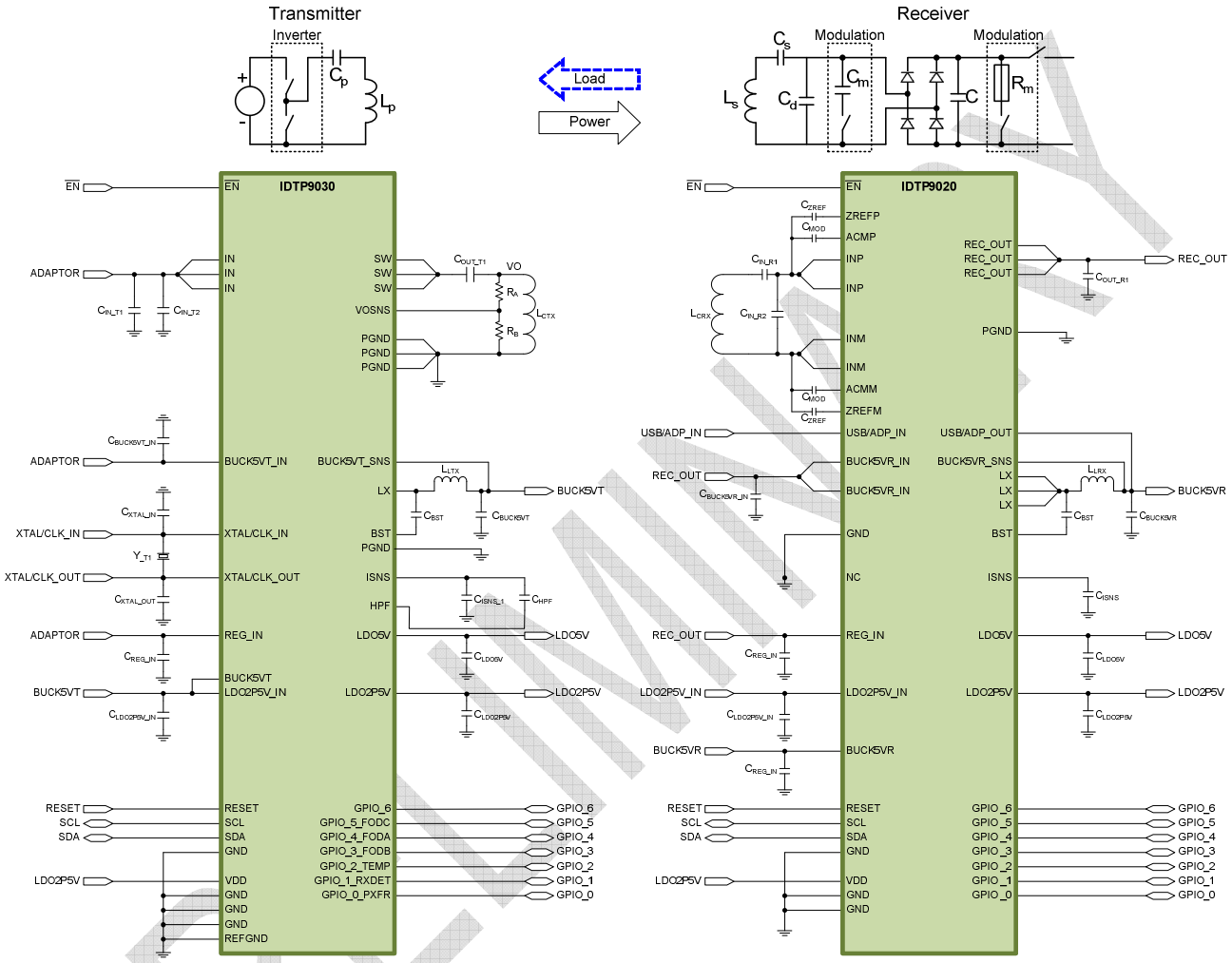

Figure 4: IDTP9030/IDTP9020 Systems Applications Diagram.

PACKAGE OUTLINE DRAWING (QFN)

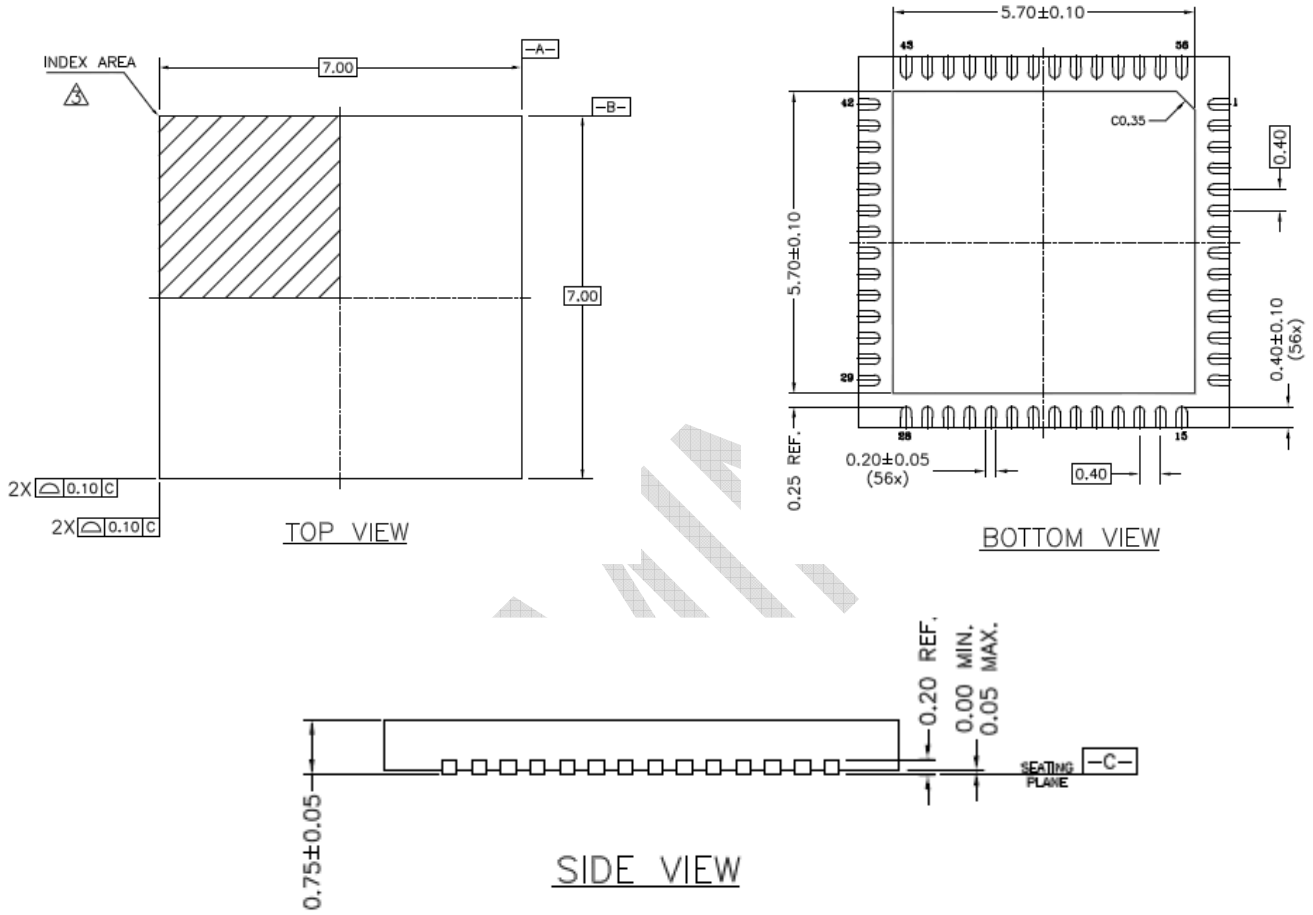

Figure 5: Package Outline Drawing (NDG QFN-56 7x7x0.75mm 56-ld)

IDTP9020

ORDERING GUIDE

Table 3: Ordering Summary

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
P9020-0NTGI		QFN-56 7x7x0.75mm	-40°C to +85°C	Tube or Tray	260
P9020-0NTGI8		QFN-56 7x7x0.75mm	-40°C to +85°C	Tape and Reel	2,000

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