

TO-252

Pin Definition:

1. Gate
2. Drain
3. Source

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (m Ω)	I_D (A)
20	30 @ $V_{GS} = 10V$	8
	40 @ $V_{GS} = 4.5V$	6

Features

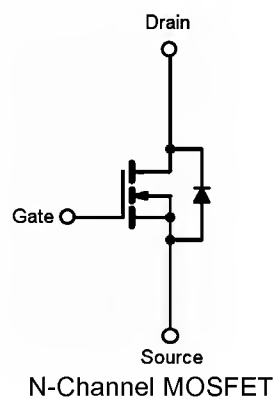
- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Load Switch
- PA Switch

Ordering Information

Part No.	Package	Packing
TSM12N02CP RO	TO-252	T&R

Block Diagram

Absolute Maximum Rating ($T_a = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current, $V_{GS} @ 4.5V$.	I_D	12	A
Pulsed Drain Current, $V_{GS} @ 4.5V$	I_{DM}	30	A
Continuous Source Current (Diode Conduction) ^{a,b}	I_S	1.7	A
Maximum Power Dissipation	P_D	60	W
		23	
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Thermal Performance

Parameter	Symbol	Limit	Unit
Lead Temperature (1/8" from case)	T_L	10	S
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.2	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta JA}$	50	$^\circ\text{C/W}$

Notes:

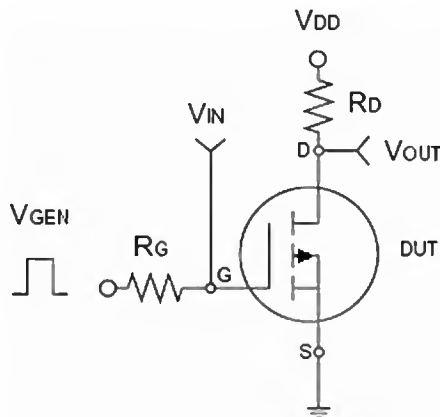
- a. Maximum DC current limited by the package
- b. Surface Mounted on 1" x 1" FR4 Board, $t \leq 10$ sec.

Electrical Specifications

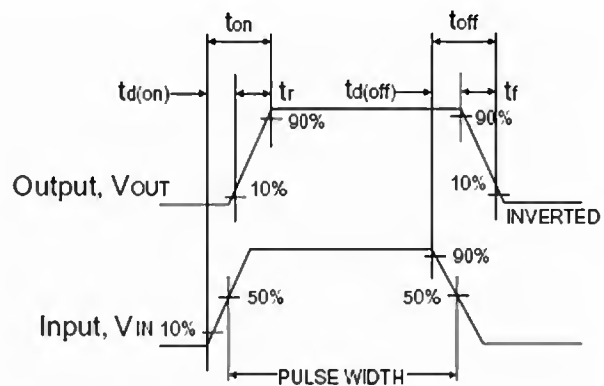
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	20	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	0.6	--	--	V
Gate Body Leakage	$V_{GS} = \pm 12V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 20V, V_{GS} = 0V$	I_{DSS}	--	--	1.0	μA
On-State Drain Current	$V_{DS} \geq 5V, V_{GS} = 10V$	$I_{D(ON)}$	12	--	--	A
Drain-Source On-State Resistance	$V_{GS} = 4.5V, I_D = 6A$	$R_{DS(ON)}$	--	30	40	m Ω
	$V_{GS} = 10V, I_D = 8A$		--	21	30	
Forward Transconductance	$V_{DS} = 10V, I_D = 6A$	g_{fs}	7	13	--	S
Diode Forward Voltage	$I_S = 1.7A, V_{GS} = 0V$	V_{SD}	--	--	1.2	V
Dynamic ^b						
Total Gate Charge	$V_{DS} = 10V, I_D = 6A,$ $V_{GS} = 4.5V$	Q_g	--	4.86	--	nC
Gate-Source Charge		Q_{gs}	--	0.92	--	
Gate-Drain Charge		Q_{gd}	--	1.4	--	
Input Capacitance	$V_{DS} = 8V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	562	--	pF
Output Capacitance		C_{oss}	--	106	--	
Reverse Transfer Capacitance		C_{rss}	--	75	--	
Switching ^c						
Turn-On Delay Time	$V_{DD} = 10V, I_D = 1A,$ $V_{GEN} = 10V,$ $R_G = 16\Omega$	$t_{d(on)}$	--	8.1	--	nS
Turn-On Rise Time		t_r	--	9.95	--	
Turn-Off Delay Time		$t_{d(off)}$	--	21.85	--	
Turn-Off Fall Time		t_f	--	5.35	--	

Notes:

- a. pulse test: $PW \leq 300\mu S$, duty cycle $\leq 2\%$
b. For DESIGN AID ONLY, not subject to production testing.
b. Switching time is essentially independent of operating temperature.



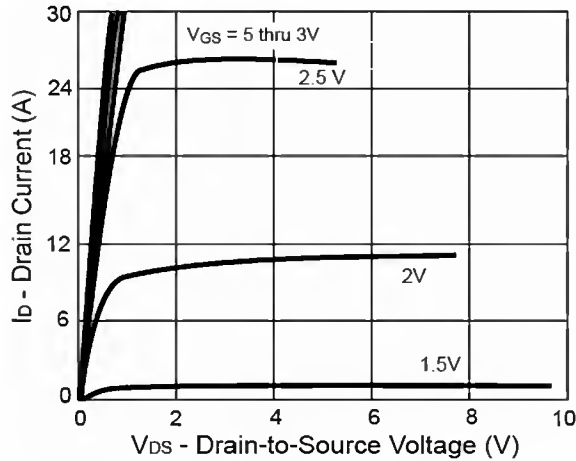
Switching Test Circuit



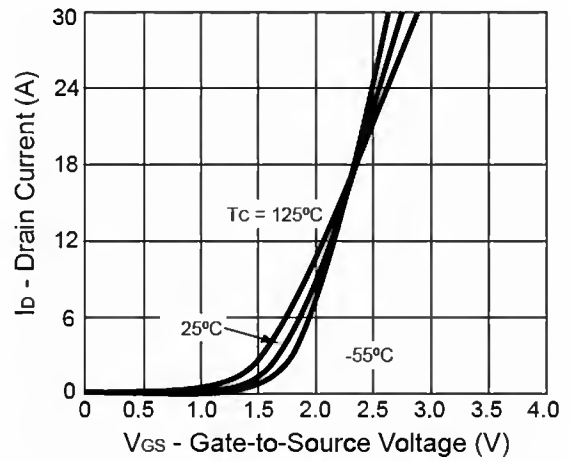
Switchin Waveforms

Electrical Characteristics Curve (Ta = 25 °C, unless otherwise noted)

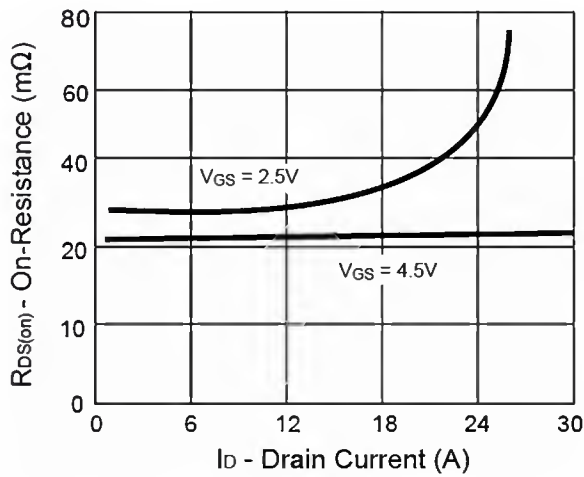
Output Characteristics



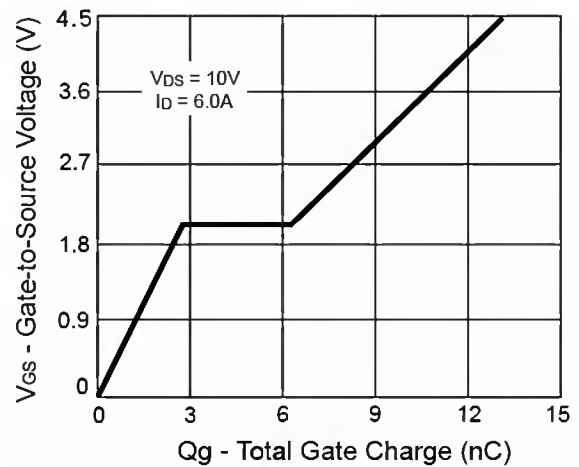
Transfer Characteristics



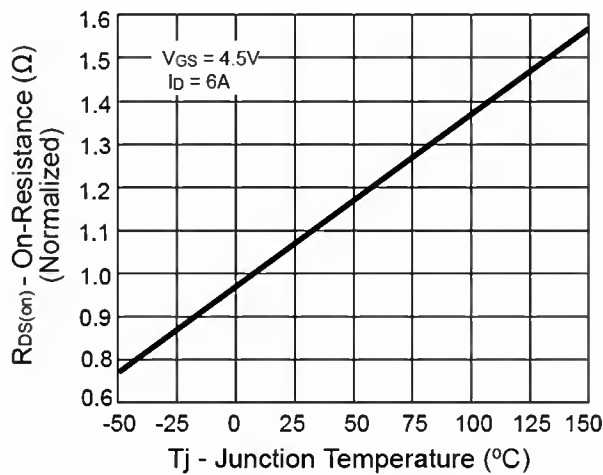
On-Resistance vs. Drain Current



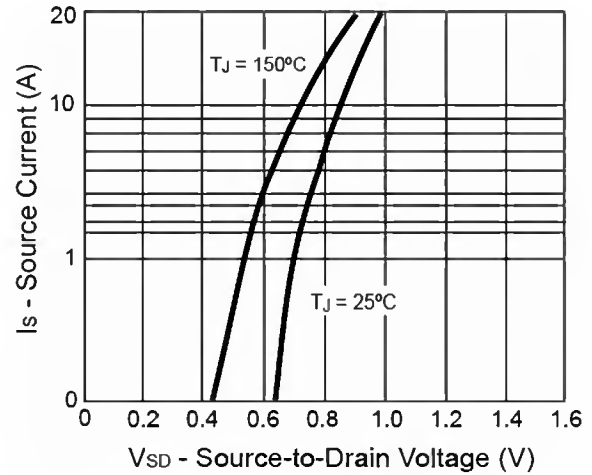
Gate Charge



On-Resistance vs. Junction Temperature

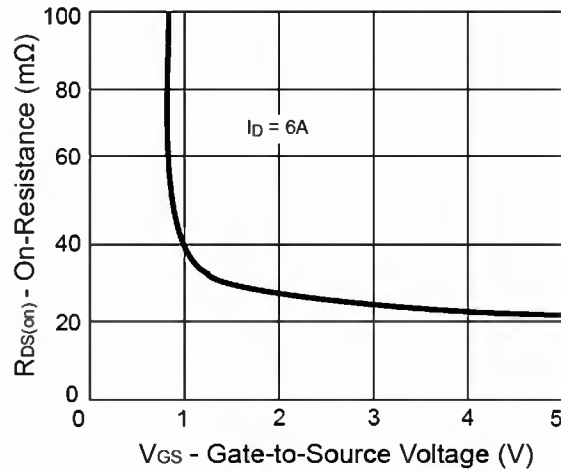


Source-Drain Diode Forward Voltage

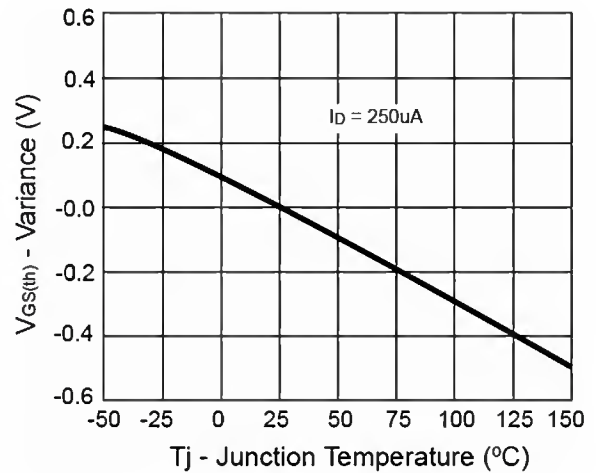


Electrical Characteristics Curve ($T_a = 25^\circ\text{C}$, unless otherwise noted)

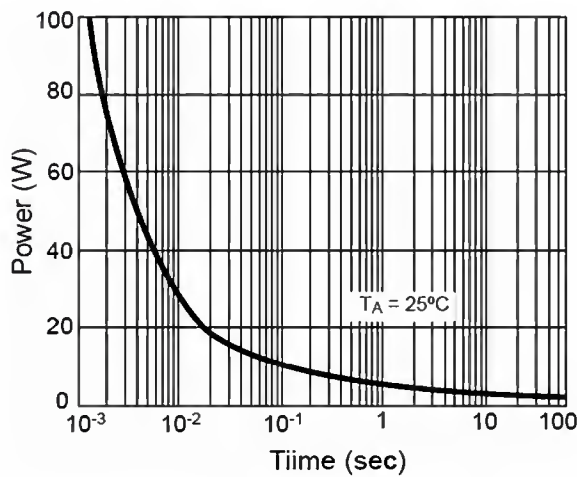
On-Resistance vs. Gate-Source Voltage



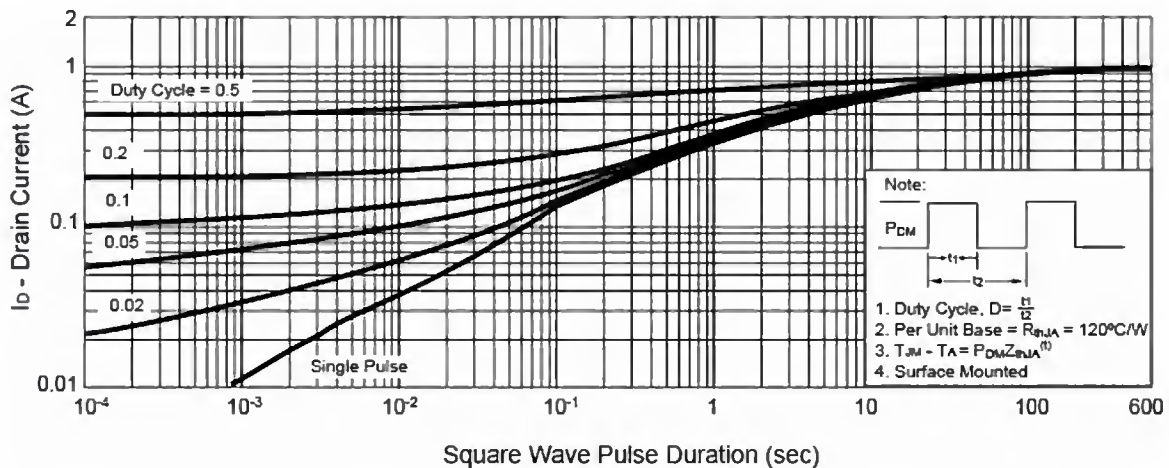
Threshold Voltage



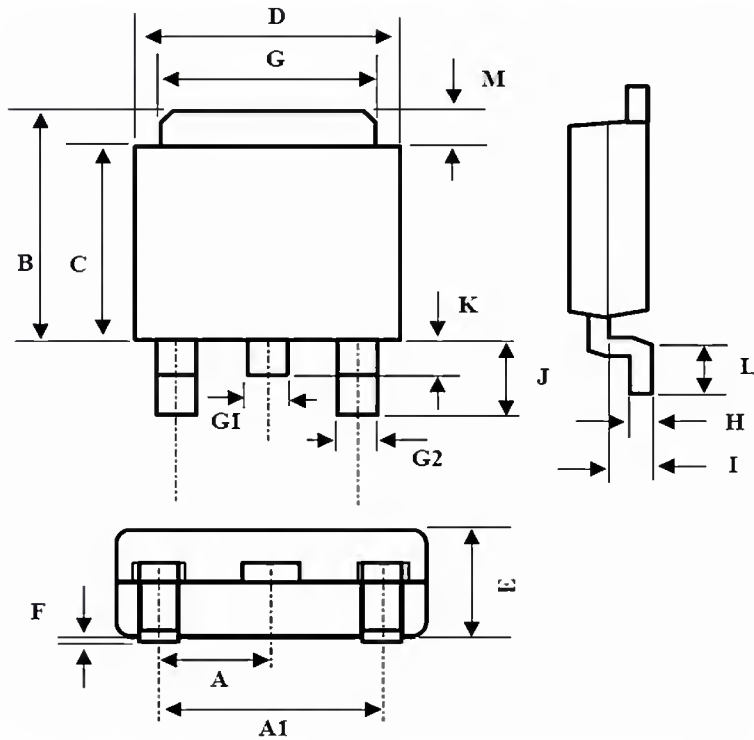
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-252 Mechanical Drawing



TO-252 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.3BSC		0.09BSC	
A1	4.6BSC		0.18BSC	
B	6.80	7.20	0.268	0.283
C	5.40	5.60	0.213	0.220
D	6.40	6.65	0.252	0.262
E	2.20	2.40	0.087	0.094
F	0.00	0.20	0.000	0.008
G	5.20	5.40	0.205	0.213
G1	0.75	0.85	0.030	0.033
G2	0.55	0.65	0.022	0.026
H	0.35	0.65	0.014	0.026
I	0.90	1.50	0.035	0.059
J	2.20	2.80	0.087	0.110
K	0.50	1.10	0.020	0.043
L	0.90	1.50	0.035	0.059
M	1.30	1.70	0.051	0.67

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