

DRA3A13Z

Silicon PNP epitaxial planar type

For digital circuits

Complementary to DRC3A13Z

DRA9A13Z in SSSMini3 type package

■ Features

- Low collector-emitter saturation voltage $V_{CE(sat)}$
- Contributes to miniaturization of sets, reduction of component count.
- Eco-friendly Halogen-free package

■ Packaging

Embossed type (Thermo-compression sealing): 10000 pcs / reel (standard)

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

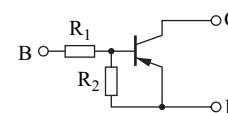
Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	-50	V
Collector-emitter voltage (Base open)	V_{CEO}	-50	V
Collector current	I_C	-80	mA
Total power dissipation	P_T	100	mW
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

■ Package

- Code
SSSMini3-F2-B
- Pin Name
 - 1: Base
 - 2: Emitter
 - 3: Collector

■ Marking Symbol: G2

■ Internal Connection



Resistance value	R_1	1	k Ω
	R_2	10	k Ω

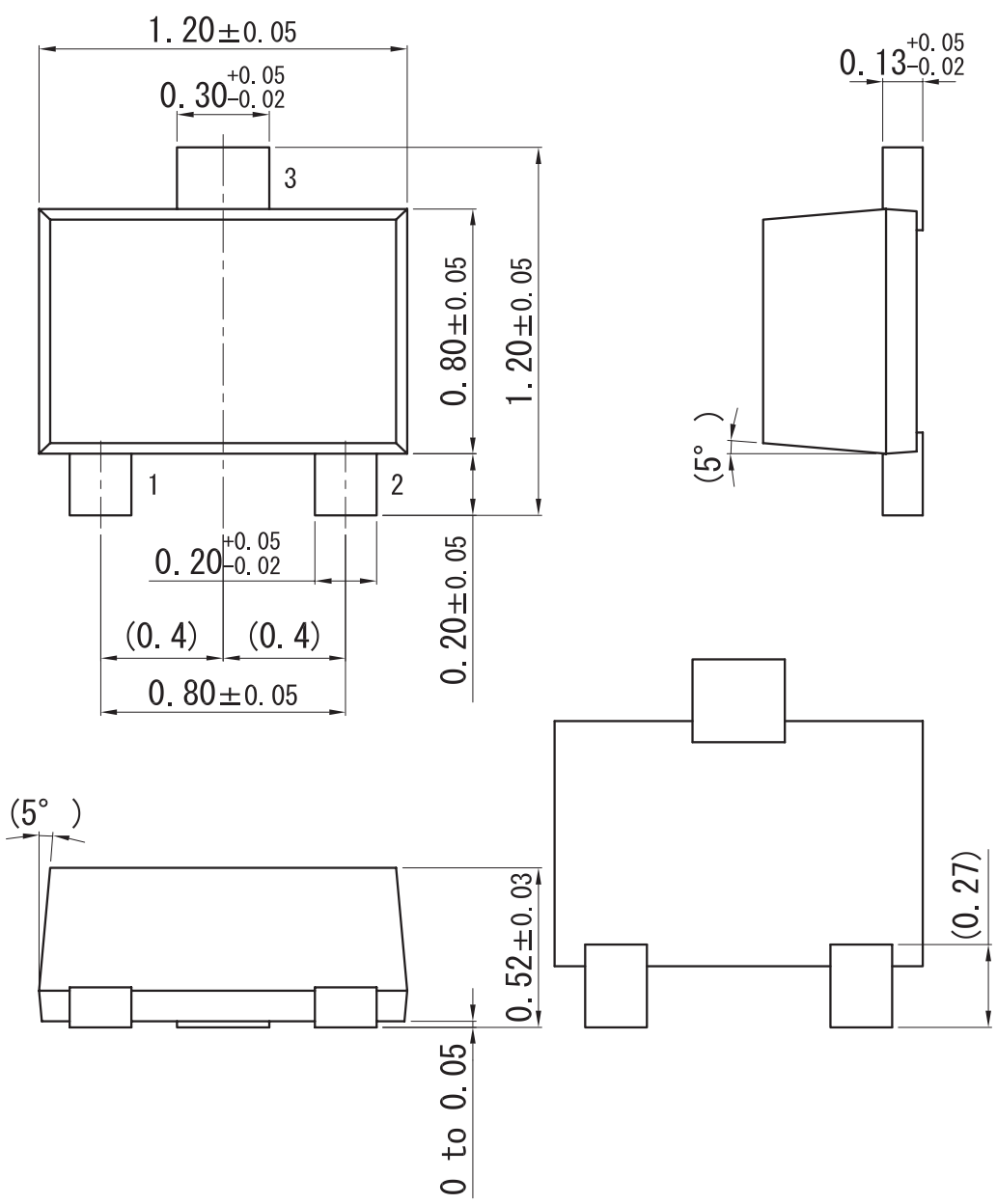
■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	V_{CBO}	$I_C = -10 \mu\text{A}$, $I_E = 0$	-50			V
Collector-emitter voltage (Base open)	V_{CEO}	$I_C = -2 \text{ mA}$, $I_B = 0$	-50			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = -50 \text{ V}$, $I_E = 0$			-0.1	μA
Collector-emitter cutoff current (Base open)	I_{CEO}	$V_{CE} = -50 \text{ V}$, $I_B = 0$			-0.5	μA
Emitter-base cutoff current (Collector open)	I_{EBO}	$V_{EB} = -6 \text{ V}$, $I_C = 0$			-1.5	mA
Forward current transfer ratio	h_{FE}	$V_{CE} = -10 \text{ V}$, $I_C = -5 \text{ mA}$	30			—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = -10 \text{ mA}$, $I_B = -0.5 \text{ mA}$			-0.25	V
Input voltage (ON)	$V_{I(on)}$	$V_{CE} = -0.2 \text{ V}$, $I_C = -5 \text{ mA}$	-1.0			V
Input voltage (OFF)	$V_{I(off)}$	$V_{CE} = -5 \text{ V}$, $I_C = -100 \mu\text{A}$			-0.4	V
Input resistance	R_1		-30%	1	+30%	k Ω
Resistance ratio	R_1 / R_2		0.08	0.10	0.12	—

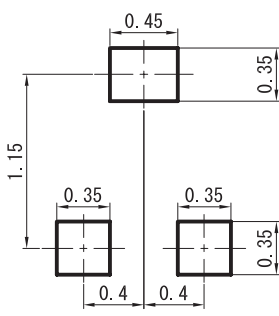
Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

SSSMini3-F2-B

Unit: mm



■ Land Pattern (Reference) (Unit: mm)



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