MMA65xx, Dual-Axis, SPI Inertial Sensor

MMA65xx, a SafeAssure solution, is a SPI-based, dual-axis, medium-*g*, over-damped lateral accelerometer designed for use in automotive airbag systems.

Features

- ±80 *g*, ±105 *g* or ±120 *g* full-scale range, independently specified for each axis
- 3.3 V or 5 V single supply operation
- SPI-compatible serial interface
- 12-bit digital signed or unsigned SPI data output
- Independent programmable arming functions for each axis
- Twelve low-pass filter options, ranging from 50 Hz to 1000 Hz
- Optional offset cancellation with > 6 s averaging period and < 0.25 LSB/s slew rate
- Pb-free, 16-pin QFN, 6 mm x 6 mm x 1.98 mm package

Referenced Documents

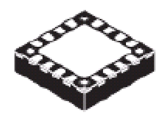
- AEC-Q100, Revision G, dated May 14, 2007 (http://www.aecouncil.com/)

Ordering information

Device	X-Axis Range	Y-Axis Range	Package	Shipping
MMA6519KCW	±80 *g*	±80 *g*	98ASA00690D	Tubes
MMA6525KCW	±105 *g*	±105 *g*	98ASA00690D	Tubes
MMA6527KCW	±120 *g*	±120 *g*	98ASA00690D	Tubes
MMA6519KCWR2	±80 *g*	±80 *g*	98ASA00690D	Tape & Reel
MMA6525KCWR2	±105 *g*	±105 *g*	98ASA00690D	Tape & Reel
MMA6527KCWR2	±120 *g*	±120 *g*	98ASA00690D	Tape & Reel

MMA65xx

Bottom view



Pb-free, 16-pin QFN
6 mm x 6 mm x 1.98 mm package

1 General Description

1.1 Application diagram

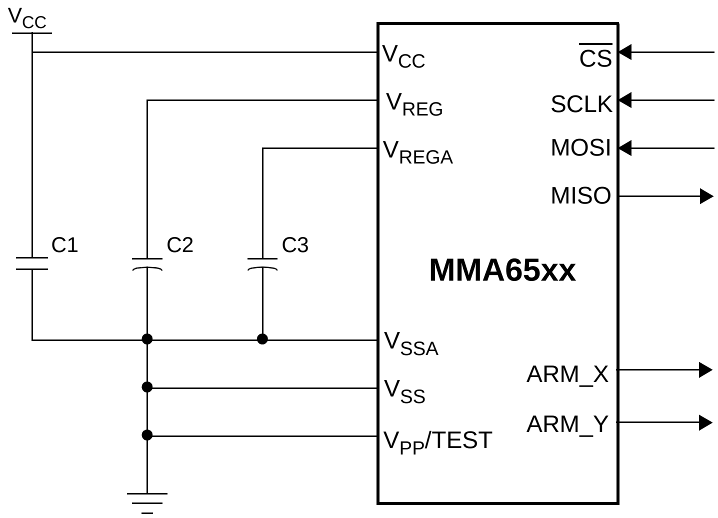


Figure 1. Application Diagram

Table 1. External Component Recommendations

Ref Des	Type	Description	Purpose
C1	Ceramic	0.1 µF, 10 %, 10 V Minimum, X7R	V_{CC} Power Supply Decoupling
C2	Ceramic	1 µF, 10 %, 10 V Minimum, X7R	Voltage Regulator Output Capacitor (C_{VREG})
C3	Ceramic	1 µF, 10 %, 10 V Minimum, X7R	Voltage Regulator Output Capacitor (C_{VREGA})

1.2 Internal block diagram

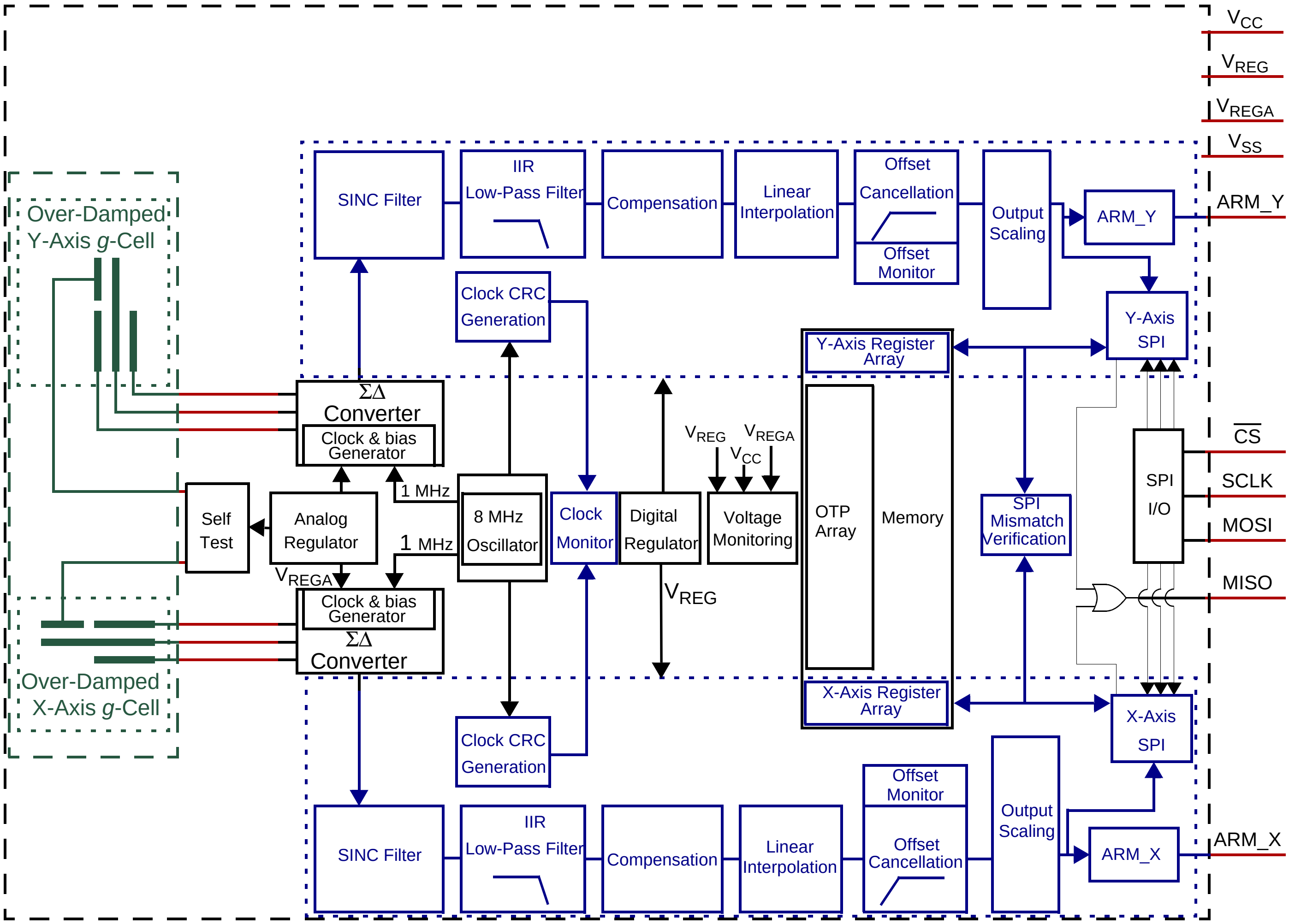


Figure 2. Internal Block Diagram

1.3 Device orientation and part marking

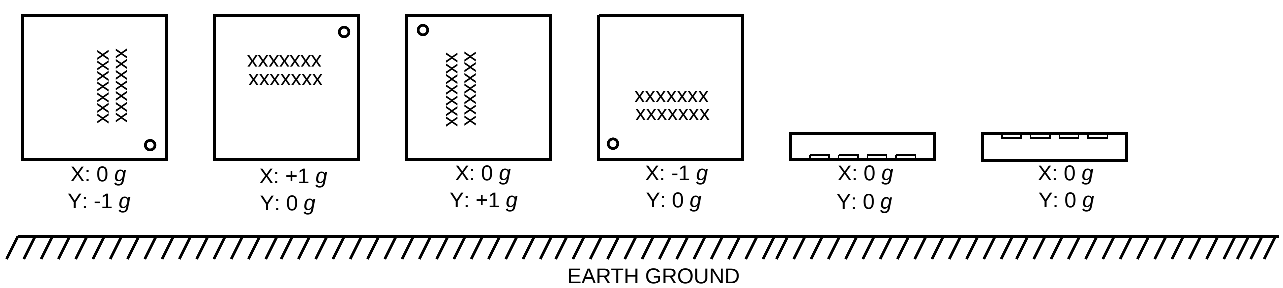
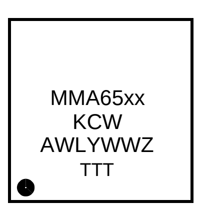


Figure 3. Device Orientation Diagram



Data Code Legend:
A: Assembly Location
WL: Wafer Lot Number (*g*-cell Lot Number)
Y: Year
WW: Work Week
Z: Assembly Lot Number

Figure 4. Part Marking

1.4 Pin Connections

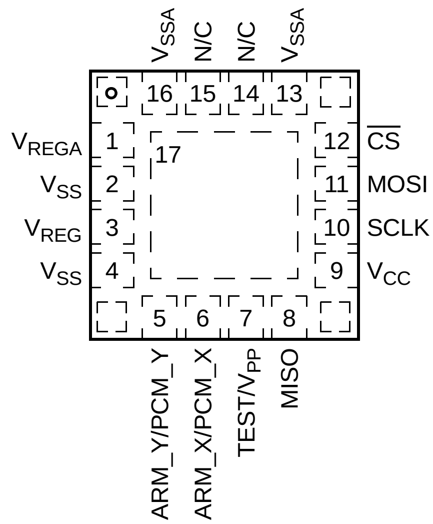


Figure 5. Top View, 16-Pin QFN Package

Table 2. Pin Descriptions

Pin	Pin Name	Formal Name	Definition
1	V_{REGA}	Analog Supply	This pin is connected to the power supply for the internal analog circuitry. An external capacitor must be connected between this pin and V_{SSA}. Reference Figure 1.
2	V_{SS}	Digital GND	This pin is the power supply return node for the digital circuitry.
3	V_{REG}	Digital Supply	This pin is connected to the power supply for the internal digital circuitry. An external capacitor must be connected between this pin and V_{SS}. Reference Figure 1.
4	V_{SS}	Digital GND	This pin is the power supply return node for the digital circuitry.
5	ARM_Y/ PCM_Y	Y-Axis Arm Output / PCM Output	The function of this pin is configurable via the DEVCFG register as described in Section 3.1.6.6. When the arming output is selected, ARM_Y can be configured as an open drain, active low output with a pullup current; or an open drain, active high output with a pulldown current. Alternatively, this pin can be configured as a digital output with PCM signal proportional to the Y axis acceleration data. Reference Section 3.8.10 and Section 3.8.11. If unused, this pin must be left unconnected.
6	ARM_X/ PCM_X	X-Axis Arm Output / PCM Output	The function of this pin is configurable via the DEVCFG register as described in Section 3.1.6.6. When the arming output is selected, ARM_X can be configured as an open drain, active low output with a pullup current; or an open drain, active high output with a pulldown current. Alternatively, this pin can be configured as a digital output with a PCM signal proportional to the X-axis acceleration data. Reference Section 3.8.10 and Section 3.8.11. If unused, this pin must be left unconnected.
7	TEST / V_{PP}	Programming Voltage	This pin provides the power for factory programming of the OTP registers. This pin must be connected to V_{SS} in the application.
8	MISO	SPI Data Out	This pin functions as the serial data output for the SPI port.
9	V_{CC}	Supply	This pin supplies power to the device. An external capacitor must be connected between this pin and V_{SS}. Reference Figure 1.
10	SCLK	SPI Clock	This input pin provides the serial clock to the SPI port. An internal pulldown device is connected to this pin.
11	MOSI	SPI Data In	This pin functions as the serial data input to the SPI port. An internal pulldown device is connected to this pin.
12	$\overline{CS}$	Chip Select	This input pin provides the chip select for the SPI port. An internal pullup device is connected to this pin.
13	V_{SSA}	Analog GND	This pin is the power supply return node for analog circuitry.
14	N/C	No Connect	Not internally connected. This pin can be unconnected or connected to V_{SS} in the application.
15	N/C	No Connect	Not internally connected. This pin can be unconnected or connected to V_{SS} in the application.
16	V_{SSA}	Analog GND	This pin is the power supply return node for analog circuitry.
17	PAD	Die Attach Pad	This pin is the die attach flag, and is internally connected to V_{SS}. Reference Section 5 for die attach pad connection details.
Corner Pads			The corner pads are internally connected to V_{SS}.

2 Electrical Characteristics

2.1 Maximum Ratings

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it.

#	Rating	Symbol	Value	Unit	
1	Supply Voltage	V_{CC}	-0.3 to +7.0	V	(3)
2	V_{REG}, V_{REGA}	V_{REG}	-0.3 to +3.0	V	(3)
3	SCLK, $\overline{CS}$, MOSI,V_{PP}/TEST	V_{IN}	-0.3 to V_{CC} + 0.3	V	(3)
4	ARM_X, ARM_Y	V_{IN}	-0.3 to V_{CC} + 0.3	V	(3)
5	MISO (high impedance state)	V_{IN}	-0.3 to V_{CC} + 0.3	V	(3)
6	Powered Shock (six sides, 0.5 ms duration)	g_{pms}	±1500	*g*	(5,18)
7	Unpowered Shock (six sides, 0.5 ms duration)	g_{shock}	±2000	*g*	(5,18)
8	Drop Shock (to concrete surface)	h_{DROP}	1.2	m	(5)
	Electrostatic Discharge				
9	Human Body Model (HBM)	V_{ESD}	±2000	V	(5)
10	Charge Device Model (CDM)	V_{ESD}	±750	V	(5)
11	Machine Model (MM)	V_{ESD}	±200	V	(5)
12	Storage Temperature Range	T_{stg}	-40 to +125	°C	(5)
13	Thermal Resistance - Junction to Case	q_{JC}	2.5	°C/W	(14)

2.2 Operating Range

The operating ratings are the limits normally expected in the application and define the range of operation.

#	Characteristic	Symbol	Min	Typ	Max	Units	
	Supply Voltage		V_L	V_{TYP}	V_H		
14	Standard Operating Voltage, 3.3 V	V_{CC}	+3.135	+3.3	+5.25	V	(15)
15	Standard Operating Voltage, 5.0 V			+5.0		V	(15)
	Operating Ambient Temperature Range		T_L		T_H		
16	Verified by 100% Final Test	T_A	-40	—	+105	C	(1)
17	Power-on Ramp Rate (V_{CC})	V_{CC_r}	0.000033	—	3300	V/µs	(19)

2.3 Electrical Characteristics - Power Supply and I/O

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $|\Delta T_A| < 25$ K/min unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	
18	Supply Current *	I_{DD}	4.0	—	8.0	mA	(1)
	Power Supply Monitor Thresholds (See Figure 9)						
19	V_{CC} Under Voltage (Falling) *	$V_{CC\_UV\_f}$	2.74	—	3.02	V	(3,6)
20	V_{REG} Under Voltage (Falling) *	$V_{REG\_UV\_f}$	2.10	—	2.25	V	(3,6)
21	V_{REG} Over Voltage (Rising) *	$V_{REG\_OV\_r}$	2.65	—	2.85	V	(3,6)
22	V_{REGA} Under Voltage (Falling) *	$V_{REGA\_UV\_f}$	2.20	—	2.35	V	(3,6)
23	V_{REGA} Over Voltage (Rising) *	$V_{REGA\_OV\_r}$	2.65	—	2.85	V	(3,6)
	Power Supply Monitor Hysteresis						
24	V_{CC} Under Voltage	V_{HYST}	65	100	110	mV	(3)
25	V_{REG} Under Voltage, V_{REG} Over Voltage	V_{HYST}	20	100	210	mV	(3)
26	V_{REGA} Under Voltage, V_{REGA} Over Voltage	V_{HYST}	20	100	150	mV	(3)
	Power Supply RESET Thresholds (See Figure 6, and Figure 9)						
27	V_{REG} Under Voltage RESET (Falling) *	$V_{REG\_UVR\_f}$	1.764	—	2.024	V	(3,6)
28	V_{REG} Under Voltage RESET (Rising) *	$V_{REG\_UVR\_r}$	1.876	—	2.152	V	(3,6)
29	V_{REG} RESET Hysteresis	V_{HYST}	80	—	140	mV	(3)
	Internally Regulated Voltages						
30	V_{REG} *	V_{REG}	2.42	2.50	2.58	V	(1,3)
31	V_{REGA} *	V_{REGA}	2.42	2.50	2.58	V	(1,3)
	External Filter Capacitor (C_{VREG}, C_{VREGA})						
32	Value	C_{VREG}, C_{VREGA}	700	1000	1500	nF	(19)
33	ESR (including interconnect resistance)	ESR	—	—	400	mΩ	(19)
	Power Supply Coupling						
34	50 kHz $\leq f_n \leq$ 20 MHz		—	—	0.004	LSB/mv	(3)
35	20 MHz $\leq f_n \leq$ 100 MHz		—	—	0.004	LSB/mv	(19)
	Output High Voltage (MISO, PCM_X, PCM_Y)						
36	3.15 V $\leq (V_{CC} - V_{SS}) \leq$ 3.45 V (I_{Load} = -1 mA) *	V_{OH_3}	V_{CC} - 0.2	—	—	V	(2,3)
37	4.75 V $\leq (V_{CC} - V_{SS}) \leq$ 5.25 V (I_{Load} = -1 mA) *	V_{OH_5}	V_{CC} - 0.4	—	—	V	(2,3)
	Output Low Voltage (MISO, PCM_X, PCM_Y)						
38	3.15 V $\leq (V_{CC} - V_{SS}) \leq$ 3.45 V (I_{Load} = 1 mA) *	V_{OL_3}	—	—	0.2	V	(2,3)
39	4.75 V $\leq (V_{CC} - V_{SS}) \leq$ 5.25 V (I_{Load} = 1 mA) *	V_{OL_5}	—	—	0.4	V	(2,3)
	Open Drain Output High Voltage (ARM_X, ARM_Y)						
40	3.15 V $\leq (V_{CC} - V_{SS}) \leq$ 3.45 V (I_{ARM} = -1 mA) *	V_{ODH_3}	V_{CC} - 0.2	—	—	V	(2,3)
41	4.75 V $\leq (V_{CC} - V_{SS}) \leq$ 5.25 V (I_{ARM} = -1 mA) *	V_{ODH_5}	V_{CC} - 0.4	—	—	V	(2,3)
	Open Drain Output Pulldown Current (ARM_X, ARM_Y)						
42	3.15 V $\leq (V_{CC} - V_{SS}) \leq$ 3.45 V (V_{ARM} = 1.5 V) *	I_{ODPD_3}	50	—	100	µA	(2,3)
43	4.75 V $\leq (V_{CC} - V_{SS}) \leq$ 5.25 V (V_{ARM} = 1.5 V) *	I_{ODPD_5}	50	—	100	µA	(2,3)
	Open Drain Output Low Voltage (ARM_X, ARM_Y)						
44	3.15 V $\leq (V_{CC} - V_{SS}) \leq$ 3.45 V (I_{ARM} = 1 mA) *	V_{ODH_3}	—	—	0.2	V	(2,3)
45	4.75 V $\leq (V_{CC} - V_{SS}) \leq$ 5.25 V (I_{ARM} = 1 mA) *	V_{ODH_5}	—	—	0.4	V	(2,3)
	Open Drain Output Pullup Current (ARM_X, ARM_Y)						
46	3.15 V $\leq (V_{CC} - V_{SS}) \leq$ 3.45 V (V_{ARM} = 1.5 V) *	I_{ODPU_3}	-100	—	-50	µA	(2,3)
47	4.75 V $\leq (V_{CC} - V_{SS}) \leq$ 5.25 V (V_{ARM} = 1.5 V) *	I_{ODPU_5}	-100	—	-50	µA	(2,3)
48	Input High Voltage $\overline{CS}$, SCLK, MOSI *	V_{IH}	2.0	—	—	V	(3,6)
49	Input Low Voltage $\overline{CS}$, SCLK, MOSI *	V_{IL}	—	—	1.0	V	(3,6)
50	Input Voltage Hysteresis $\overline{CS}$, SCLK, MOSI *	V_{I_HYST}	0.125	—	0.500	V	(19)
	Input Current						
51	High (at V_{IH}) (SCLK, MOSI) *	I_{IH}	-70	-50	-30	µA	(2,3)
52	Low (at V_{IL}) ($\overline{CS}$) *	I_{IL}	30	50	70	µA	(2,3)

2.4 Electrical Characteristics - Sensor and Signal Chain

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $|\Delta T_A| < 25$ K/min unless otherwise specified.

#	Characteristic		Symbol	Min	Typ	Max	Units	
	Digital Sensitivity (SPI)							
53	80g (12-Bit Output)	*	SENS	—	24.0	—	LSB/g	(1,9)
54	105.5g (12-Bit Output)	*	SENS	—	18.2	—	LSB/g	(1,9)
55	120g (12-Bit Output)	*	SENS	—	16.0	—	LSB/g	(1,9)
	Sensitivity Error							
56	T_A = 25 °C	*	ΔSENS	-4	—	+4	%	(1)
57	-40 °C ≤ T_A ≤ 105 °C	*	ΔSENS	-5	—	+5	%	(1)
58	-40 °C ≤ T_A ≤ 105 °C, $V_{CC\_UV\_f} \leq V_{CC} - V_{SS} \leq V_L$		ΔSENS	-5	—	+5	%	(3)
	Offset at 0g (105.5g 120g Range, No Offset Cancellation)							
59a	12 bits, unsigned	*	OFFSET	1988	2048	2108	LSB	(1)
60a	12 bits, signed	*	OFFSET	-60	0	+60	LSB	(1)
61a	12 bits, unsigned, $V_{CC\_UV\_f} \leq V_{CC} - V_{SS} \leq V_L$		OFFSET	1988	—	1988	LSB	(3)
62a	12 bits, signed, $V_{CC\_UV\_f} \leq V_{CC} - V_{SS} \leq V_L$		OFFSET	-60	—	-60	LSB	(3)
	Offset at 0g (80g Range, No Offset Cancellation)							
63a	12 bits, unsigned	*	OFFSET	1968	2048	2128	LSB	(1)
64a	12 bits, signed	*	OFFSET	-80	0	+80	LSB	(1)
65a	12 bits, unsigned, $V_{CC\_UV\_f} \leq V_{CC} - V_{SS} \leq V_L$		OFFSET	1968	—	1968	LSB	(3)
66a	12 bits, signed, $V_{CC\_UV\_f} \leq V_{CC} - V_{SS} \leq V_L$		OFFSET	-80	—	-80	LSB	(3)
	Offset at 0g (With Offset Cancellation)							
67b	12 bits, unsigned	*	OFFSET	2047.75	2048	2048.25	LSB	(9,7)
68b	12 bits, signed	*	OFFSET	-0.25	0	+0.25	LSB	(9,7)
69b	12 bits, unsigned, $V_{CC\_UV\_f} \leq V_{CC} - V_{SS} \leq V_L$		OFFSET	2047.75	—	2048.25	LSB	(9)
70b	12 bits, signed, $V_{CC\_UV\_f} \leq V_{CC} - V_{SS} \leq V_L$		OFFSET	-0.25	—	+0.25	LSB	(9)
	Offset Monitor Thresholds							
71	Positive Threshold (12 bits signed)		$OFFTHR_{POS}$	—	100	—	LSB	(7)
72	Negative Threshold (12 bits signed)		$OFFTHR_{NEG}$	—	-100	—	LSB	(7)
	Range of Output (SPI, 12 bits, unsigned)							
73	Normal		RANGE	128	—	3968	LSB	(7)
74	Fault Response Code		FAULT	—	0	—	LSB	(7)
75	Unused Codes		UNUSED	1	—	127	LSB	(7)
76	Unused Codes		UNUSED	3969	—	4095	LSB	(7)
	Range of Output (SPI, 12 bits, signed)							
77	Normal		RANGE	-1920	—	1920	LSB	(7)
78	Unused Codes		UNUSED	-2047	—	-1921	LSB	(7)
79	Unused Codes		UNUSED	1921	—	2047	LSB	(7)
80	Nonlinearity	*	NL_{OUT}	-1	—	1	% FSR	(3)
	System Output Noise							
81	RMS (12 bits, All Ranges, 400 Hz, 3-pole LPF)		n_{RMS}	—	—	1	LSB	(3)
82	Peak to Peak (12 bits, All Ranges, 400 Hz, 3-pole LPF)		n_{P-P}	—	—	3	LSB	(3)
	Cross-Axis Sensitivity							
83	V_{ZX}	*	V_{ZX}	-4	—	+4	%	(3)
84	V_{YX}	*	V_{YX}	-4	—	+4	%	(3)
85	V_{ZY}	*	V_{ZY}	-4	—	+4	%	(3)
86	V_{XY}	*	V_{XY}	-4	—	+4	%	(3)

2.5 Self Test

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $|\Delta T_A| < 25$ K/min unless otherwise specified.

#	Characteristic		Symbol	Min	Typ	Max	Units	
	Self Test Output Change (Ref Section 3.6)			ΔST_{MIN}	ΔST_{NOM}	ΔST_{MAX}		
87	80g, T_A = 25 °C	*	ΔST_{80_25}	582	727	872	LSB	(1)
88	80g, -40 °C $\le T_A \le$ 105 °C	*	$\Delta ST_{80\_\Delta T}$	545	727	909	LSB	(1)
89	80g, -40 °C $\le T_A \le$ 105 °C, $V_{CC\_UV\_f} \le V_{CC} - V_{SS} \le V_L$		$\Delta ST_{80\_\Delta T\Delta V}$	545	727	909	LSB	(3)
90	105.5 *g*, T_A = 25 °C	*	ΔST_{105_25}	442	553	663	LSB	(1)
91	105.5 g, -40 °C $\le T_A \le$ 105 °C	*	$\Delta ST_{105\_\Delta T}$	414	553	690	LSB	(1)
92	105.5 g, -40 °C $\le T_A \le$ 105 °C, $V_{CC\_UV\_f} \le V_{CC} - V_{SS} \le V_L$		$\Delta ST_{105\_\Delta T\Delta V}$	414	553	690	LSB	(3)
93	120g, T_A = 25 °C	*	ΔST_{120_25}	387	484	581	LSB	(1)
94	120g, -40 °C $\le T_A \le$ 105 °C	*	$\Delta ST_{120\_\Delta T}$	363	484	605	LSB	(1)
95	120g, -40 °C $\le T_A \le$ 105 °C, $V_{CC\_UV\_f} \le V_{CC} - V_{SS} \le V_L$		$\Delta ST_{120\_\Delta T\Delta V}$	363	484	605	LSB	(3)
	Self Test Cross-Axis Output							
96	Y-Axis Output with X-Axis Self Test		ΔSTCrossAxis	-10	—	+10	LSB	(1)
97	X-Axis Output with Y-Axis Self Test		ΔSTCrossAxis	-10	—	+10	LSB	(1)
	Self Test Output Accuracy							
98	Δ from Stored Value, including Sensitivity Error	*						
99	-40 °C $\le T_A \le$ 105 °C (Ref Section 3.6)		ΔSTACC	-10	—	+10	%	(3)
	Sigma Delta Modulator Range							
100	X/Y-Axis, Any Range Positive/Negative		g_{ADCl_Clip}	375	400	450	g	(19)
	Acceleration (without hitting internal *g*-cell stops)							
101	X/Y-Axis, Any Range Positive/Negative		$g_{g\text{-}cell\_Clip}$	500	560	600	g	(19)

2.6 Dynamic Electrical Characteristics - Signal Chain

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $|\Delta T_A| < 25$ K/min unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
102	DSP Sample Rate (LPF 0,1,2,3,4,5)	t_S	—	$64/f_{OSC}$	—	s	(7)
103	DSP Sample Rate (LPF 8,9,10,11,12,13)	t_S	—	$128/f_{OSC}$	—	s	(7)
104	Interpolation Sample Rate	t_{INTERP}	—	$t_S/2$	—	s	(7)
	Data Path Latency (excluding *g*-cell and Low-pass Filter)						
105	$T_S = 64/f_{OSC}$ *	$t_{DataPath\_8}$	33.0	34.8	36.5	µs	(7,16)
106	$T_S = 128/f_{OSC}$ *	$t_{DataPath\_16}$	51.9	54.6	57.4	µs	(7,16)
	Low-Pass Filter (t_s = 8µs)						
107	Cutoff frequency 0: 100 Hz, 4-pole *	$f_{C0(LPF)}$	95	100	105	Hz	(3,7,17)
108	Cutoff frequency 1: 300 Hz, 4-pole *	$f_{C1(LPF)}$	285	300	315	Hz	(3,7,17)
109	Cutoff frequency 2: 400 Hz, 4-pole *	$f_{C2(LPF)}$	380	400	420	Hz	(3,7,17)
110	Cutoff frequency 3: 800 Hz, 4-pole *	$f_{C3(LPF)}$	760	800	840	Hz	(3,7,17)
111	Cutoff frequency 4: 1000 Hz, 4-pole *	$f_{C4(LPF)}$	950	1000	1050	Hz	(3,7,17)
112	Cutoff frequency 5: 400 Hz, 3-pole *	$f_{C5(LPF)}$	380	400	420	Hz	(3,7,17)
	Low-Pass Filter (t_s = 16µs)						
113	Cutoff frequency 8: 50 Hz, 4-pole *	$f_{C8(LPF)}$	47.5	50	52.5	Hz	(3,7,17)
114	Cutoff frequency 9: 150 Hz, 4-pole *	$f_{C9(LPF)}$	142.5	150	157.5	Hz	(3,7,17)
115	Cutoff frequency 10: 200 Hz, 4-pole *	$f_{C10(LPF)}$	190	200	210	Hz	(3,7,17)
116	Cutoff frequency 11: 400 Hz, 4-pole *	$f_{C11(LPF)}$	380	400	420	Hz	(3,7,17)
117	Cutoff frequency 12: 500 Hz, 4-pole *	$f_{C12(LPF)}$	475	500	525	Hz	(3,7,17)
118	Cutoff frequency 13: 200 Hz, 3-pole *	$f_{C13(LPF)}$	190	200	210	Hz	(3,7,17)
	Offset Cancellation (Normal Mode, 12-Bit Output)						
119	Offset Averaging Period *	OFF_{AVEPER}	—	6.29146	—	s	(3,7)
120	Offset Slew Rate *	OFF_{SLEW}	—	0.2384	—	LSB/s	(3,7)
121	Offset Update Rate *	OFF_{RATE}	—	1049	—	ms	(3,7)
122	Offset Correction Value per Update Positive *	OFF_{CORRP}	—	0.25	—	LSB	(3,7)
123	Offset Correction Value per Update Negative *	OFF_{CORRN}	—	-0.25	—	LSB	(3,7)
124	Offset Correction Threshold Positive *	OFF_{THP}	—	0.125	—	LSB	(3,7)
125	Offset Correction Threshold Negative *	OFF_{THN}	—	0.125	—	LSB	(3,7)
	Self Test Activation Time ($\overline{CS}$ rising edge to 90% of ST Final Value)						
126	Cutoff frequency 0: 100 Hz, 4-pole	ST_ACT_{100}	—	—	7.00	ms	(19)
127	Cutoff frequency 1: 300 Hz, 4-pole	ST_ACT_{300}	—	—	3.00	ms	(19)
128	Cutoff frequency 2: 400 Hz, 4-pole	ST_ACT_{400}	—	—	2.50	ms	(19)
129	Cutoff frequency 3: 800 Hz, 4-pole	ST_ACT_{800}	—	—	1.70	ms	(19)
130	Cutoff frequency 4: 1000 Hz, 4-pole	ST_ACT_{1000}	—	—	1.60	ms	(19)
131	Cutoff frequency 5: 400 Hz, 3-pole	$ST\_ACT_{400\_3}$	—	—	2.40	ms	(19)
132	Offset Monitor Bypass Time after Self Test Deactivation	t_{ST_OMB}	—	320	—	t_S	(3,7)
133	Time Between Acceleration Data Requests (Same Axis)	t_{ACC_REQ}	15	—	—	µs	(3,7,20)
	Arming Output Activation Time (ARM_X, ARM_Y, I_{ARM} = 200µA)						
134	Moving Average and Count Arming Modes (2,3,4,5)	t_{ARM}	0	—	1.51	µs	(3,12)
135	Unfiltered Mode Activation Delay (Reference Figure 30)	$t_{ARM\_UF\_DLY}$	0	—	1.51	µs	(3,12)
136	Unfiltered Mode Arm Assertion Time (Reference Figure 30)	$t_{ARM\_UF\_ASSERT}$	5.00	—	6.579	µs	(3)
137	Sensing Element Natural Frequency	f_{gcell}	10791	13464	15879	Hz	(19)
138	Sensing Element Cutoff Frequency (-3 dB ref. to 0 Hz)	f_{gcell}	0.851	1.58	2.29	kHz	(19)
139	Sensing Element Damping Ratio	ζ_{gcell}	2.46	4.31	9.36	—	(19)
140	Sensing Element Delay (@100 Hz)	f_{gcell_delay}	70	101	187	µs	(19)
141	Sensing Element Step Response (0% - 90%)	t_{Step_gcell}	—	—	200	µs	(19)
142	Package Resonance Frequency	$f_{Package}$	100	—	—	kHz	(19)
143	Package Quality Factor	$q_{Package}$	1	—	5	—	(19)

2.7 Dynamic Electrical Characteristics - Supply and SPI

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $|\Delta T_A| < 25$ K/min unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	
144	Power-On Recovery Time (VCC = VCCMIN to first SPI access)	t_{OP}	—	—	10	ms	(3)
145	Power-On Recovery Time (Internal POR to first SPI access)	t_{OP}	—	—	840	µs	(3,7)
146	SPI Reset Activation Time (CS high to Reset)	t_{SPI_RESET}	—	—	300	ns	(7)
147	Internal Oscillator Frequency *	f_{OSC}	7.6	8	8.4	MHz	(7)
148	Test Frequency - Divided from Internal Oscillator	f_{OSCTST}	0.95	1	1.05	MHz	(1)
	Serial Interface Timing (See Figure 7, $C_{MISO} \leq 80$pF, $R_{MISO} \geq 10$kW)						
149	Clock (SCLK) period (10% of V_{CC} to 10% of V_{CC}) *	t_{SCLK}	120	—	—	ns	(3)
150	Clock (SCLK) high time (90% of V_{CC} to 90% of V_{CC}) *	t_{SCLKH}	40	—	—	ns	(3)
151	Clock (SCLK) low time (10% of V_{CC} to 10% of V_{CC}) *	t_{SCLKL}	40	—	—	ns	(3)
152	Clock (SCLK) rise time (10% of V_{CC} to 90% of V_{CC})	t_{SCLKR}	—	15	40	ns	(19)
153	Clock (SCLK) fall time (90% of V_{CC} to 10% of V_{CC})	t_{SCLKF}	—	15	28	ns	(19)
154	$\overline{CS}$ asserted to SCLK high ($\overline{CS}$ = 10% of V_{CC} to SCLK = 10% of V_{CC})	t_{LEAD}	60	—	—	ns	(3)
155	$\overline{CS}$ asserted to MISO valid ($\overline{CS}$ = 10% of V_{CC} to MISO = 10/90% of V_{CC})	t_{ACCESS}	—	—	60	ns	(3)
156	Data setup time (MOSI = 10/90% of V_{CC} to SCLK = 10% of V_{CC}) *	t_{SETUP}	20	—	—	ns	(3)
157	MOSI Data hold time (SCLK = 90% of V_{CC} to MOSI = 10/90% of V_{CC}) *	t_{HOLD_IN}	10	—	—	ns	(3)
158	MISO Data hold time (SCLK = 90% of V_{CC} to MISO = 10/90% of V_{CC}) *	t_{HOLD_OUT}	0	—	—	ns	(3)
159	SCLK low to data valid (SCLK = 10% of V_{CC} to MISO = 10/90% of V_{CC}) *	t_{VALID}	—	—	35	ns	(3)
160	SCLK low to $\overline{CS}$ high (SCLK = 10% of V_{CC} to $\overline{CS}$ = 90% of V_{CC}) *	t_{LAG}	60	—	—	ns	(3)
161	$\overline{CS}$ high to MISO disable ($\overline{CS}$ = 90% of V_{CC} to MISO = Hi Z) *	$t_{DISABLE}$	—	—	60	ns	(3)
162	$\overline{CS}$ high to $\overline{CS}$ low ($\overline{CS}$ = 90% of V_{CC} to $\overline{CS}$ = 90% of V_{CC}) *	t_{CSN}	526	—	—	ns	(3)
163	SCLK low to $\overline{CS}$ low (SCLK = 10% of V_{CC} to $\overline{CS}$ = 90% of V_{CC}) *	t_{CLKCS}	50	—	—	ns	(3)
164	$\overline{CS}$ high to SCLK high ($\overline{CS}$ = 90% of V_{CC} to SCLK = 90% of V_{CC})	t_{CSCLK}	50	—	—	ns	(19)

1. Parameters tested 100% at final test.
2. Parameters tested 100% at wafer probe.
3. Parameters verified by characterization
4. (*) Indicates a critical characteristic.
5. Verified by qualification testing.
6. Parameters verified by pass/fail testing in production.
7. Functionality verified 100% via scan. Timing characteristic is directly determined by internal oscillator frequency.
8. N/A.
9. Devices are trimmed at 100 Hz with 1000 Hz low-pass filter option selected. Response is corrected to 0 Hz response.
10. Low-pass filter cutoff frequencies shown are -3 dB referenced to 0 Hz response.
11. Power supply ripple at frequencies greater than 900 kHz should be minimized to the greatest extent possible.
12. Time from falling edge of $\overline{CS}$ to ARM_X, ARM_Y output valid
13. N/A.
14. Thermal resistance between the die junction and the exposed pad; cold plate is attached to the exposed pad.
15. Device characterized at all values of V_L and V_H. Production test is conducted at all typical voltages (V_{TYP}) unless otherwise noted.
16. Data Path Latency is the signal latency from *g*-cell to SPI output disregarding filter group delays.
17. Filter characteristics are specified independently, and do not include *g*-cell frequency response.
18. Electrostatic Deflection Test completed during wafer probe.
19. Verified by Simulation.
20. Acceleration Data Request timing constraint only applies for proper operation of the Arming Function.

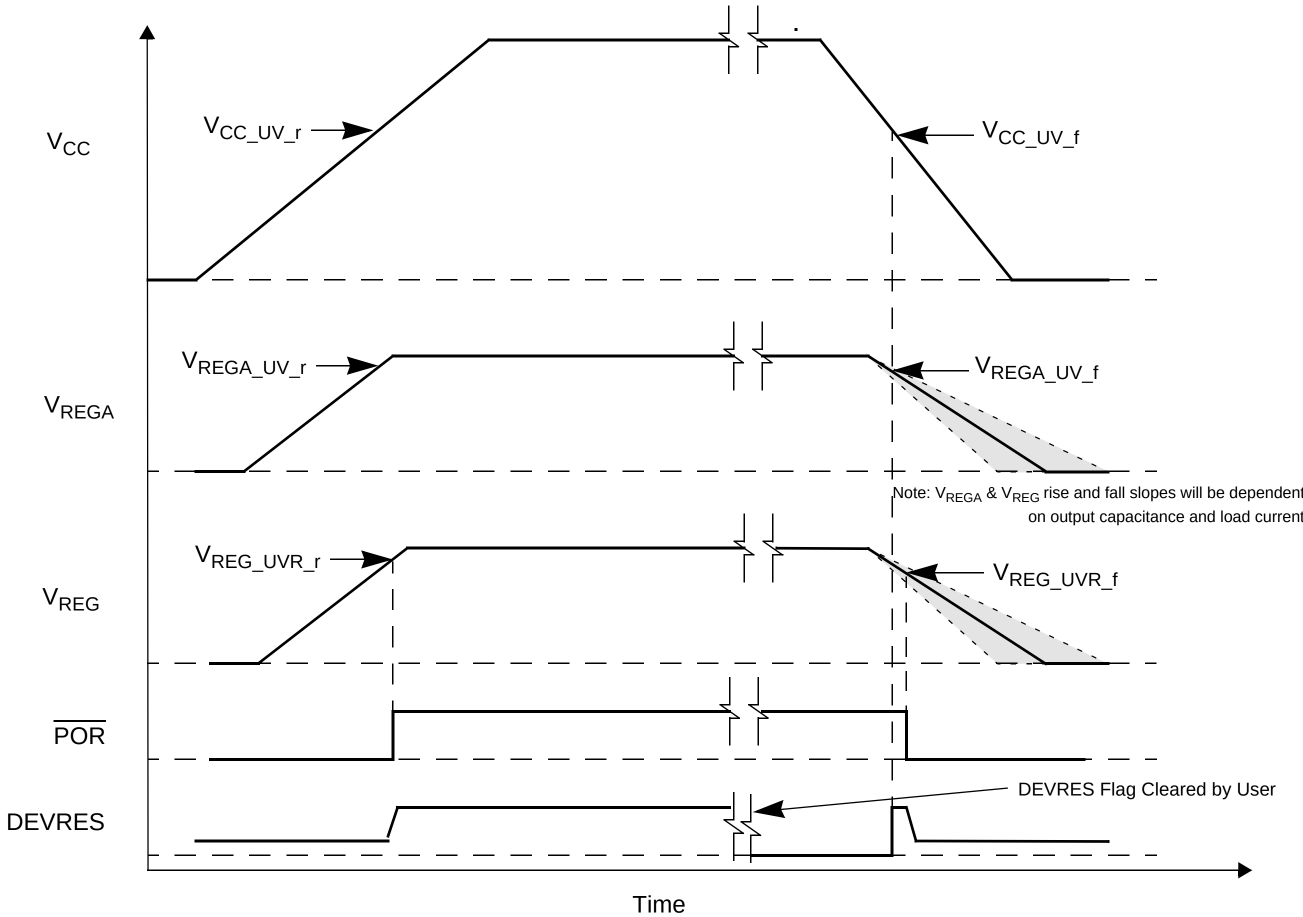


Figure 6. Power-Up Timing

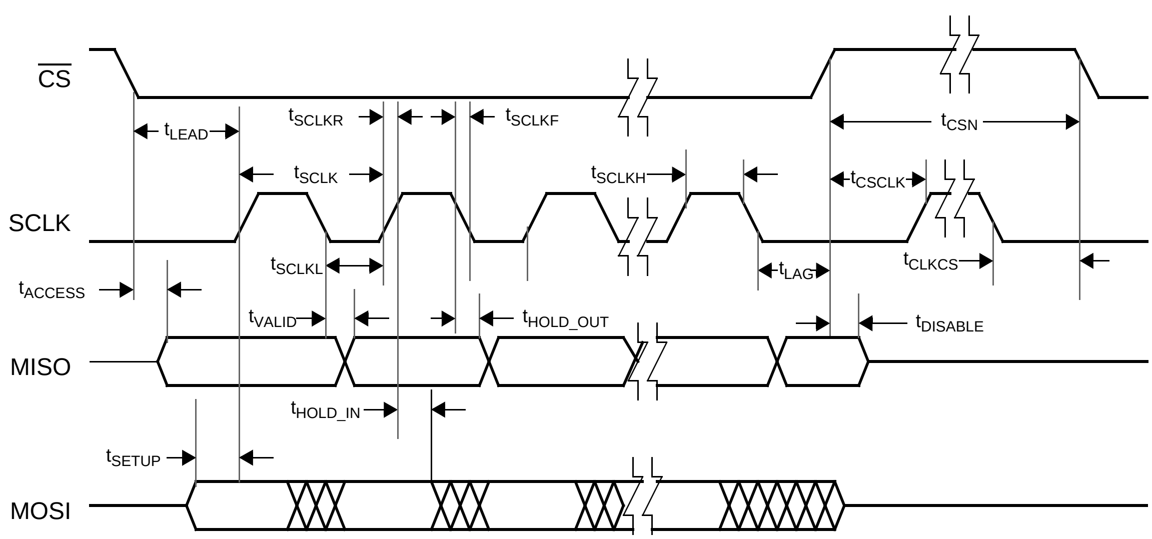


Figure 7. Serial Interface Timing

3 Functional Description

3.1 Customer Accessible Data Array

A customer accessible data array allows for each device to be customized. The array consists of an OTP factory programmable block and read/write registers for device programmability and status. The OTP and writable register blocks incorporate independent CRC circuitry for fault detection (reference Section 3.2). The writable register block includes a locking mechanism to prevent unintended changes during normal operation. Portions of the array are reserved for factory-programmed trim values. The customer accessible data is shown in the table below.

Table 3. Customer Accessible Data

Location		Bit Function								Type
Addr	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
$00	SN0	SN[7]	SN[6]	SN[5]	SN[4]	SN[3]	SN[2]	SN[1]	SN[0]	F
$01	SN1	SN[15]	SN[14]	SN[13]	SN[12]	SN[11]	SN[10]	SN[9]	SN[8]	
$02	SN2	SN[23]	SN[22]	SN[21]	SN[20]	SN[19]	SN[18]	SN[17]	SN[16]	
$03	SN3	SN[31]	SN[30]	SN[29]	SN[28]	SN[27]	SN[26]	SN[25]	SN[24]	
$04	STDEFL_X	STDEFL_X[7]	STDEFL_X[6]	STDEFL_X[5]	STDEFL_X[4]	STDEFL_X[3]	STDEFL_X[2]	STDEFL_X[1]	STDEFL_X[0]	
$05	STDEFL_Y	STDEFL_Y[7]	STDEFL_Y[6]	STDEFL_Y[5]	STDEFL_Y[4]	STDEFL_Y[3]	STDEFL_Y[2]	STDEFL_Y[1]	STDEFL_Y[0]	
$06	FCTCFG_X	1	0	0	0	0	0	0	1	
$07	FCTCFG_Y	1	0	0	0	0	0	0	1	
$08	PN	PN[7]	PN[6]	PN[5]	PN[4]	PN[3]	PN[2]	PN[1]	PN[0]	
$09	Invalid Address: “Invalid Register Request”									
$0A	DEVCTL	RES_1	RES_0	OCPHASE[1]	OCPHASE[0]	OFFCFG_EN	Reserved	Reserved	Reserved	R/W
$0B	DEVCFG	$\overline{\text{OC}}$	Reserved	ENDINIT	$\overline{\text{SD}}$	OFMON	A_CFG[2]	A_CFG[1]	A_CFG[0]	
$0C	DEVCFG_X	ST_X	Reserved	Reserved	Reserved	LPF_X[3]	LPF_X[2]	LPF_X[1]	LPF_X[0]	
$0D	DEVCFG_Y	ST_Y	Reserved	Reserved	Reserved	LPF_Y[3]	LPF_Y[2]	LPF_Y[1]	LPF_Y[0]	
$0E	ARMCFGX	Reserved	Reserved	APS_X[1]	APS_X[0]	AWS_XN[1]	AWS_XN[0]	AWS_XP[1]	AWS_XP[0]	
$0F	ARMCFGY	Reserved	Reserved	APS_Y[1]	APS_Y[0]	AWS_YN[1]	AWS_YN[0]	AWS_YP[1]	AWS_YP[0]	
$10	ARMT_XP	AT_XP[7]	AT_XP[6]	AT_XP[5]	AT_XP[4]	AT_XP[3]	AT_XP[2]	AT_XP[1]	AT_XP[0]	
$11	ARMT_YP	AT_YP[7]	AT_YP[6]	AT_YP[5]	AT_YP[4]	AT_YP[3]	AT_YP[2]	AT_YP[1]	AT_YP[0]	
$12	ARMT_XN	AT_XN[7]	AT_XN[6]	AT_XN[5]	AT_XN[4]	AT_XN[3]	AT_XN[2]	AT_XN[1]	AT_XN[0]	
$13	ARMT_YN	AT_YN[7]	AT_YN[6]	AT_YN[5]	AT_YN[4]	AT_YN[3]	AT_YN[2]	AT_YN[1]	AT_YN[0]	
$14	DEVSTAT	UNUSED	IDE	UNUSED	DEVINIT	MISOERR	OFF_Y	OFF_X	DEVRES	R
$15	COUNT	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]	
$16	OFFCORR_X	OFFCORR_X[7]	OFFCORR_X[6]	OFFCORR_X[5]	OFFCORR_X[4]	OFFCORR_X[3]	OFFCORR_X[2]	OFFCORR_X[1]	OFFCORR_X[0]	
$17	OFFCORR_Y	OFFCORR_Y[7]	OFFCORR_Y[6]	OFFCORR_Y[5]	OFFCORR_Y[4]	OFFCORR_Y[3]	OFFCORR_Y[2]	OFFCORR_Y[1]	OFFCORR_Y[0]	
$1C	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
$1D	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	

Type codes

F: Factory programmed OTP locationR/W:Read/write register

R: Read-only registerN/A:Not applicable

3.1.1 Device Serial Number Registers

A unique serial number is programmed into the serial number registers of each device during manufacturing. The serial number is composed of the following information:

Bit Range	Content
S12 - S0	Serial Number
S31 - S13	Lot Number

Serial numbers begin at 1 for all produced devices in each lot, and are sequentially assigned. Lot numbers begin at 1 and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 13-bit serial number. Depending on lot size and quantities, all possible lot numbers and serial numbers may not be assigned.

The serial number registers are included in the OTP shadow register array CRC verification. Reference Section 3.2.1 for details regarding the CRC verification. Beyond this, the contents of the serial number registers have no impact on device operation or performance, and are only used for traceability purposes.

3.1.2 Self Test Deflection Registers (STDEFL_X, STDEFL_Y)

These read-only registers provide the nominal self test deflection values for each axis at ambient temperature. The self test value is a positive deflection value, measured at the factory, and factory programmed for each device. The minimum stored value ($00) equates to the minimum deflection specified in Section 2.4 (ΔST_{MIN}), and the maximum stored value ($FF) equates to the maximum deflection specified in Section 2.4 (ΔST_{MAX}).

Table 4. Self Test Deflection Registers

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$04	STDEFL_X	STDEFL_X[7]	STDEFL_X[6]	STDEFL_X[5]	STDEFL_X[4]	STDEFL_X[3]	STDEFL_X[2]	STDEFL_X[1]	STDEFL_X[0]
$05	STDEFL_Y	STDEFL_Y[7]	STDEFL_Y[6]	STDEFL_Y[5]	STDEFL_Y[4]	STDEFL_Y[3]	STDEFL_Y[2]	STDEFL_Y[1]	STDEFL_Y[0]

When self test is activated, the acceleration reading can be compared to the value in this register. The difference from the measured deflection value, and the nominal deflection value stored in the register shall not fall outside the self test accuracy limits specified in Section 2.4 (ΔST_{ACC}). Reference Section 3.6 for more details on calculating the self test limits.

3.1.3 Factory Configuration Registers

The factory configuration registers are one time programmable, read only registers which contain customer specific device configuration information that is programmed by NXP.

Table 5. Factory Configuration Register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$06	FCTCFG_X	1	0	0	0	0	0	0	1
$07	FCTCFG_Y	1	0	0	0	0	0	0	1

3.1.4 Part Number Register (PN)

The part number register is a one time programmable, read only register which contains two digits of the device part number to identify the axis and range information. The contents of this register have no impact on device operation or performance.

Table 6. Part Number Register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$08	PN	PN[7]	PN[6]	PN[5]	PN[4]	PN[3]	PN[2]	PN[1]	PN[0]

PN Register Value		X-Axis Range Section 2.4	Y-Axis Range Section 2.4
Decimal	**HEX**		
219	$DB	80	80
225	$E1	105	105
227	$E3	120	120

3.1.5 Device Control Register (DEVCTL

The device control register is a read-write register which contains device control operations. The upper 2 bits of this register can be written during both initialization and normal operation. Bits 5 through 0 can be programmed during initialization and then are ignored once the ENDINIT bit is set.

Table 7. Device Control Register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0A	DEVCTL	RES_1	RES_0	OCPHASE[1]	OCPHASE[0]	OFFCFG_EN	Reserved	Reserved	Reserved
Reset Value		0	0	0	0	0	0	0	0

3.1.5.1 Reset Control (RES_1, RES_0)

A series of three consecutive register write operations to the reset control bits in the DEVCTL register will cause a device reset. To reset the internal digital circuitry, the following register write operations must be performed in the order shown below. The register write operations must be consecutive SPI commands in the order shown or the device will not be reset.

Register Write to DEVCTL	RES_1	RES_0	Effect
SPI Register Write 1	0	0	No Effect
SPI Register Write 2	1	1	No Effect
SPI Register Write 3	0	1	Device RESET

The response to the Register Write returns ‘0’ for RES_1 and RES_0, and the existing register value bits 5 through 0. A Register Read of RES_1 and RES_0 returns ‘0’ and terminates the reset sequence. If ENDINIT is cleared, the bits 2 through 0 in the DEVCTL register are modified as described in Section 4.4. If ENDINIT is set, a Register Write will not modify bits 2 through 0 and the response to a Register Read or Write will include the last successful written values for these bits.

3.1.5.2 Offset Cancellation Phase Control Bits (OCPHASE[1:0])

The offset cancellation phase control bits control the offset cancellation start up phase. These bits can be written at any time ENDINIT is '0' if the OFFCFG_EN bit is set.

OFFCFG_EN	OCPHASE[1]	OCPHASE[0]	Writes to OCPHASE[1:0]	Offset Cancellation Phase
0	Don't Care	Don't Care	Ignored	Continues from the previously written phase (OCPHASE[1:0]) as specified in Section 3.8.4.
1	0	0	Accepted	Remains in Start 1 until OFFCFG_EN is cleared or ENDINIT is set
1	0	1	Accepted	Remains in Start 2 until OFFCFG_EN is cleared or ENDINIT is set
1	1	0	Accepted	Remains in Start 3 until OFFCFG_EN is cleared or ENDINIT is set
1	1	1	Accepted	Remains in Normal Mode until OFFCFG_EN is cleared or ENDINIT is set

When ENDINIT is set, the OCPHASE[1:0] bits in a write command are ignored and the offset cancellation phase is set to "Normal". This can only be changed by a device reset. The response to a register read or write of the DEVCTL register once ENDINIT is set will return the last successfully written values of OCPHASE[1:0].

3.1.5.3 Offset Cancellation Configuration Enable Bit (OFFCFG_EN)

The offset cancellation phase configuration enable bit enables modification of the offset cancellation phase control bits (OCPHASE[1:0]) as shown in Section 3.1.5.2

When ENDINIT is set, the OFFCFG_EN bit in a write command is ignored, and the offset cancellation phase is set to "Normal". This can only be changed by a device reset. The response to a register read or write of the DEVCTL register once ENDINIT is set will return the last successfully written value of OFFCFG_EN.

3.1.5.4 Reserved Bits (DEVCTL[2:0])

Bits 2 through 0 of the DEVCTL register are reserved. A write to the reserved bits must always be logic '0' for normal device operation and performance.

3.1.6 Device Configuration Register (DEVCFG)

The device configuration register is a read/write register which contains data for general device configuration. The register can be written during initialization but is locked once the ENDINIT bit is set. This register is included in the writable register CRC check. Refer to Section 3.2.2 for details.

Table 8. Device Configuration Register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0B	DEVCFG	$\overline{\text{OC}}$	Reserved	ENDINIT	$\overline{\text{SD}}$	OFMON	A_CFG[2]	A_CFG[1]	A_CFG[0]
Reset Value		0	0	0	0	0	0	0	0

3.1.6.1 Offset Cancelled Data Selection Bits ($\overline{\text{OC}}$)

The Offset Cancelled Data Selection Bit determines whether the SPI transmitted data is raw data or offset cancelled data.

$\overline{\text{OC}}$	SPI Data
0	Offset Cancelled
1	Raw Data

If the $\overline{\text{OC}}$ bit is cleared (Offset Cancelled Data), then the Offset Monitor is automatically enabled (OFMON = '1') regardless of the value written to DEVCFG[3].

3.1.6.2 Reserved Bit (Reserved)

Bits 6 of the DEVCFG register is reserved. A write to the reserved bit must always be logic '0' for normal device operation and performance.

3.1.6.3 End of Initialization Bit (ENDINIT)

The ENDINIT bit is a control bit used to indicate that the user has completed all device and system level initialization tests, and that the device will operate in normal mode. Once the ENDINIT bit is set, writes to all writable register bits are inhibited except for the DEVCTL register. Once written, the ENDINIT bit can only be cleared by a device reset. The writable register CRC check (reference Section 3.2.2) is only enabled when the ENDINIT bit is set.

When ENDINIT is set, the following occurs:

- Offset Cancellation is forced to normal mode. OCPHASE[1:0], and OFFCFG_EN remain in their previously set states.
- X-Axis Self Test is disabled. ST_X remains in its previously set states.
- Y-Axis Self Test is disabled. ST_Y remains in its previously set states.

3.1.6.4 $\overline{\text{SD}}$ Bit

The $\overline{\text{SD}}$ bit determines the format of acceleration data results. If the $\overline{\text{SD}}$ bit is set to a logic ‘1’, unsigned results are transmitted, with the zero-g level represented by a nominal value of 512. If the $\overline{\text{SD}}$ bit is cleared, signed results are transmitted, with the zero-*g* level represented by a nominal value of 0.

$\overline{\text{SD}}$	Operating Mode
1	Unsigned Data Output
0	Signed Data Output

3.1.6.5 OFMON Bit

The OFMON bit determines if the offset monitor circuit is enabled. If the OFMON bit is set to a logic ‘1’, the offset monitor is enabled. Reference Section 3.8.5. If the OFMON bit is cleared, the offset monitor is disabled.

OFMON	Operating Mode
1	Offset Monitor Circuit Enabled
0	Offset Monitor Circuit Disabled

If the $\overline{\text{OC}}$ bit in the DEVCFG register is cleared (Offset Cancelled Data), then the Offset Monitor is automatically enabled (OFMON = ‘1’) regardless of the value written to DEVCFG[3].

3.1.6.6 ARM Configuration Bits (A_CFG[2:0])

The ARM Configuration Bits (A_CFG[2:0]) select the mode of operation for the ARM_X/PCM_X, ARM_Y/PCM_Y pins.

Table 9. Arming Output Configuration

A_CFG[2]	A_CFG[1]	A-CFG[0]	Operating Mode	Output Type	Reference
0	0	0	Arm Output Disabled	Hi Impedance	
0	0	1	PCM Output	Digital Output	Section 3.8.11
0	1	0	Moving Average Mode	Active High with Pulldown Current	Section 3.8.10.1
0	1	1	Moving Average Mode	Active Low with Pullup Current	Section 3.8.10.1
1	0	0	Count Mode	Active High with Pulldown Current	Section 3.8.10.2
1	0	1	Count Mode	Active Low with Pullup Current	Section 3.8.10.2
1	1	0	Unfiltered Mode	Active High with Pulldown Current	Section 3.8.10.3
1	1	1	Unfiltered Mode	Active Low with Pullup Current	Section 3.8.10.3

3.1.7 Axis Configuration Registers (DEVCFG_X, DEVCFG_Y)

The Axis configuration registers are read/write registers which contain axis specific configuration information. These registers can be written during initialization, but are locked once the ENDINIT bit is set. These registers are included in the writable register CRC check. Refer to Section 3.2.2 for details.

Table 10. Axis Configuration Registers

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0C	DEVCFG_X	ST_X	Reserved	Reserved	Reserved	LPF_X[3]	LPF_X[2]	LPF_X[1]	LPF_X[0]
$0D	DEVCFG_Y	ST_Y	Reserved	Reserved	Reserved	LPF_Y[3]	LPF_Y[2]	LPF_Y[1]	LPF_Y[0]
Reset Value		0	0	0	0	0	0	0	0

3.1.7.1 Self Test Control (ST_X, ST_Y)

The ST_X and ST_Y bits enable and disable the self test circuitry for their respective axes. Self test circuitry is enabled if a logic '1' is written to ST_X, or ST_Y and the ENDINIT bit has not been set. Enabling the self test circuitry results in a positive acceleration value on the enabled axis. Self test deflection values are specified in Section 2.4. ST_X and ST_Y are always cleared following internal reset.

When the self test circuitry is active, the offset cancellation block and the offset monitor status are suspended, and the status bits in the Acceleration Data Request Response will indicate "Self Test Active". Reference Section 3.8.4 and Section 4.2 for details. When the self test circuitry is disabled by clearing the ST_X or ST_Y bit, the offset monitor remains disabled until the time t_{ST_OMB} specified in Section 2.6 expires. However, the status bits in the Acceleration Data Request Response will immediately indicate that self test is deactivated.

When ENDINIT is set, self test is disabled. This can only be changed by a reset. A Register Write will not modify the ST_X and ST_Y bits and the response to a Register Read or Write will include the last successful written values for these bits.

3.1.7.2 Reserved Bits (Reserved)

Bits 6 through 4 of the DEVCFG_X and DEVCFG_Y registers are reserved. A write to the reserved bits must always be logic '0' for normal device operation and performance.

3.1.7.3 Low-Pass Filter Selection Bits (LPF_X[3:0], LPF_Y[3:0])

The Low-pass Filter selection bits independently select a low-pass filter for each axis as shown in Table 11. Refer to Section 3.8.3 for details regarding filter configurations.

Table 11. Low-pass Filter Selection Bits

LPF_X[3] / LPF_Y[3]	LPF_X[2] / LPF_Y[2]	LPF_X[1] / LPF_Y[1]	LPF_X[0] / LPF_Y[0]	Low-pass Filter Selected	Nominal Sample Rate (μs)
0	0	0	0	100 Hz, 4-pole	8
0	0	0	1	300 Hz, 4-pole	8
0	0	1	0	400 Hz, 4-pole	8
0	0	1	1	800 Hz, 4-pole	8
0	1	0	0	1000 Hz, 4-pole	8
0	1	0	1	400 Hz, 3-pole	8
0	1	1	0	Reserved	Reserved
0	1	1	1	Reserved	Reserved
1	0	0	0	50 Hz, 4-pole	16
1	0	0	1	150 Hz, 4-pole	16
1	0	1	0	200 Hz, 4-pole	16
1	0	1	1	400 Hz, 4-pole	16
1	1	0	0	500 Hz, 4-pole	16
1	1	0	1	200 Hz, 3-pole	16
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

Note: Filter characteristics do not include *g*-cell frequency response.

3.1.8 Arming Configuration Registers (ARMCFGX, ARMCFGY)

The arming configuration registers contain configuration information for the arming function. The values in these registers are only relevant if the arming function is operating in moving average mode, or count mode.

These registers can be written during initialization but are locked once the ENDINIT bit is set. Refer to Section 3.1.6.3. These registers are included in the writable register CRC check. Refer to Section 3.2.2 for details.

Table 12. Arming Configuration Register

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$0E	ARMCFGX	Reserved	Reserved	APS_X[1]	APS_X[0]	AWS_XN[1]	AWS_XN[0]	AWS_XP[1]	AWS_XP[0]
$0F	ARMCFGY	Reserved	Reserved	APS_Y[1]	APS_Y[0]	AWS_YN[1]	AWS_YN[0]	AWS_YP[1]	AWS_YP[0]
Reset Value		0	0	0	0	1	1	1	1

3.1.9 Reserved Bits (Reserved)

Bits 7 through 6 of the ARMCFGX and ARMCFGY registers are reserved. A write to the reserved bits must always be logic ‘0’ for normal device operation and performance.

3.1.9.1 Arming Pulse Stretch (APS_X[1:0], APS_Y[1:0])

The APS_X[1:0] and APS_Y[1:0] bits set the programmable pulse stretch time for the arming outputs. Refer to Section 3.8.10 for more details regarding the arming function. Pulse stretch times are derived from the internal oscillator, so the tolerance on this oscillator applies.

Table 13. Arming Pulse Stretch Definitions

APS_X[1], APS_Y[1]	APS_X[0], APS_Y[0]	Pulse Stretch Time (Typical Oscillator)
0	0	0 mS
0	1	16.256 ms - 16.384 ms
1	0	65.408ms - 65.536 ms
1	1	261.888ms - 262.016 ms

3.1.9.2 Arming Window Size (AWS_Xx[1:0], AWS_Yx[1:0])

The AWS_Xx[1:0] & AWS_Yx[1:0] bits have different functions depending on the state of the A_CFG bits in the DEVCFG register. If the arming function is set to moving average mode, the AWS bits set the number of acceleration samples used for the arming function moving average. The number of samples is set independently for each axis and polarity. If the arming function is set to count mode, the AWS bits set the sample count limit for the arming function. The sample count limit is set independently for each axis. Refer to Section 3.8.10 for more details regarding the arming function.

Table 14. X-Axis Positive Arming Window Size Definitions (Moving Average Mode)

AWS_XP[1]	AWS_XP[0]	X-Axis Positive Window Size
0	0	2
0	1	4
1	0	8
1	1	16

Table 15. X-Axis Negative Arming Window Size Definitions (Moving Average Mode)

AWS_XN[1]	AWS_XN[0]	X-Axis Negative Window Size
0	0	2
0	1	4
1	0	8
1	1	16

Table 16. Y-Axis Positive Arming Window Size Definitions (Moving Average Mode)

AWS_YP[1]	AWS_YP[0]	Y-Axis Positive Window Size
0	0	2
0	1	4
1	0	8
1	1	16

Table 17. Y-Axis Negative Arming Window Size Definitions (Moving Average Mode)

AWS_YN[1]	AWS_YN[0]	Y-Axis Negative Window Size
0	0	2
0	1	4
1	0	8
1	1	16

Table 18. Arming Count Limit Definitions (Count Mode)

AWS_XN[1]	AWS_XN[0]	AWS_XP[1]	AWS_XP[0]	X-Axis Sample Count Limit
Don't Care	Don't Care	0	0	1
Don't Care	Don't Care	0	1	3
Don't Care	Don't Care	1	0	7
Don't Care	Don't Care	1	1	15

Table 19. Arming Count Limit Definitions (Count Mode)

AWS_YN[1]	AWS_YN[0]	AWS_YP[1]	AWS_YP[0]	Y-Axis Sample Count Limit
Don't Care	Don't Care	0	0	1
Don't Care	Don't Care	0	1	3
Don't Care	Don't Care	1	0	7
Don't Care	Don't Care	1	1	15

3.1.10 Arming Threshold Registers (ARMT_XP, ARMT_XN, ARMT_YP, ARMT_YN)

The arming threshold registers contain the X-axis and Y-axis positive and negative thresholds to be used by the arming function. Refer to Section 3.8.10 for more details regarding the arming function.

The arming threshold registers can be written during initialization but are locked once the ENDINIT bit is set. Refer to Section 3.1.6.3. The arming threshold registers are included in the writable register CRC check. Refer to Section 3.2.2 for details.

Table 20. Arming Threshold Registers

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$10	ARMT_XP	AT_XP[7]	AT_XP[6]	AT_XP[5]	AT_XP[4]	AT_XP[3]	AT_XP[2]	AT_XP[1]	AT_XP[0]
$11	ARMT_YP	AT_YP[7]	AT_YP[6]	AT_YP[5]	AT_YP[4]	AT_YP[3]	AT_YP[2]	AT_YP[1]	AT_YP[0]
$12	ARMT_XN	AT_XN[7]	AT_XN[6]	AT_XN[5]	AT_XN[4]	AT_XN[3]	AT_XN[2]	AT_XN[1]	AT_XN[0]
$13	ARMT_YN	AT_YN[7]	AT_YN[6]	AT_YN[5]	AT_YN[4]	AT_YN[3]	AT_YN[2]	AT_YN[1]	AT_YN[0]
Reset Value		0	0	0	0	0	0	0	0

The values programmed into the threshold registers are the threshold values used for the arming function as described in Section 3.8.10. The threshold registers hold independent unsigned 8-bit values for each axis and polarity. Each threshold increment is equivalent to one output LSB. Table 21 shows examples of some threshold register values and the corresponding threshold.

Table 21. Threshold Register Value Examples

Axis Type		Programmed Thresholds		Positive Threshold (g)	Negative Threshold (g)
Range (g)	Sensitivity (LSB/g)	Positive (Decimal)	Negative (Decimal)		
80	24	100	50	4.17	-2.08
80	24	255	0	10.625	Disabled
80	24	50	20	2.08	-0.83
80	24	150	75	6.25	-3.125
105.5	18.2	100	50	5.50	-2.75
105.5	18.2	255	0	14.0	Disabled
105.5	18.2	50	20	2.75	-1.10
105.5	18.2	150	75	8.24	-4.12

If either the positive or negative threshold for one axis is programmed to $00, comparisons are disabled for only that polarity. The arming function still operates for the opposite polarity. If both the positive and negative arming thresholds for one axis are programmed to $00, the Arming function for the associated axis is disabled, and the associated output pin is disabled, regardless of the value of the A_CFG bits in the DEVCFG register.

3.1.11 Device Status Register (DEVSTAT)

The device status register is a read-only register. A read of this register clears the status flags affected by transient conditions. Reference Section 4.5 for details on the response for each status condition.

Table 22. Device Status Register

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$14	DEVSTAT	UNUSED	IDE	UNUSED	DEVINIT	MISOERR	OFF_Y	OFF_X	DEVRES

3.1.11.1 Unused Bits (UNUSED)

The unused bits have no impact on operation or performance. When read these bits may be ‘1’ or ‘0’.

3.1.11.2 Internal Data Error Flag (IDE)

The internal data error flag is set if a customer or OTP register data CRC fault or other internal fault is detected as defined in Section 4.5.5. The internal data error flag is cleared by a read of the DEVSTAT register. If the error is associated with a CRC fault in the writable register array, the fault will be re-asserted and will require a device reset to clear. If the error is associated with the data stored in the fuse array, the fault will be re-asserted even after a device reset.

3.1.11.3 Device Initialization Flag (DEVINIT)

The device initialization flag is set during the interval between negation of internal reset and completion of internal device initialization. DEVINIT is cleared automatically. The device initialization flag is not affected by a read of the DEVSTAT register.

3.1.11.4 SPI MISO Data Mismatch Error Flag (MISOERR)

The MISO data mismatch flag is set when a MISO Data mismatch fault occurs as specified in Section 4.5.2. The MISOERR flag is cleared by a read of the DEVSTAT register.

3.1.11.5 Offset Monitor Error Flags (OFF_X, OFFSET_Y)

The offset monitor error flags are set if the acceleration signal of the associated axis reaches the specified offset limit. The offset monitor error flags are cleared by a read of the DEVSTAT register.

3.1.11.6 Device Reset Flag (DEVRES)

The device reset flag is set during device initialization following a device reset. The device reset flag is cleared by a read of the DEVSTAT register.

3.1.12 Count Register (COUNT)

The count register is a read-only register which provides the current value of a free-running 8-bit counter derived from the primary oscillator. A 10-bit pre-scaler divides the primary oscillator frequency by 1024. Thus, the value in the register increases by one count every 128 μs and the counter rolls over every 32.768 ms.

Table 23. Count Register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$15	COUNT	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
Reset Value		0	0	0	0	0	0	0	0

3.1.13 Offset Correction Value Registers (OFFCORR_X, OFFCORR_Y)

The offset correction value registers are read-only registers which contain the most recent offset correction increment / decrement value from the offset cancellation circuit. The values stored in these registers indicate the amount of offset correction being applied to the SPI output data. The values have a resolution of 1 LSB.

Table 24. Offset Correction Value Register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$16	OFFCORR_X	OFFCORR_X[7]	OFFCORR_X[6]	OFFCORR_X[5]	OFFCORR_X[4]	OFFCORR_X[3]	OFFCORR_X[2]	OFFCORR_X[1]	OFFCORR_X[0]
$17	OFFCORR_Y	OFFCORR_Y[7]	OFFCORR_Y[6]	OFFCORR_Y[5]	OFFCORR_Y[4]	OFFCORR_Y[3]	OFFCORR_Y[2]	OFFCORR_Y[1]	OFFCORR_Y[0]
Reset Value		0	0	0	0	0	0	0	0

3.1.14 Reserved Registers (Reserved)

Registers $1C and $1D are reserved. A write to the reserved bits must always be logic ‘0’ for normal device operation and performance.

Table 25. Reserved Registers

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$1C	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
$1D	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset Value		0	0	0	0	0	0	0	0

3.2 Customer Accessible Data Array CRC Verification

3.2.1 OTP Shadow Register Array CRC Verification

The OTP shadow register array is verified for errors using a 3-bit CRC. The CRC verification uses a generator polynomial of $g(x) = X^3 + X + 1$, with a seed value = ‘111’. If a CRC error is detected in the OTP array, the IDE bit is set in the DEVSTAT register.

3.2.2 Writable Register CRC Verification

The writable registers in the data array are verified for errors using a 3-bit CRC. The CRC verification is enabled only when the ENDINIT bit is set in the DEVCFG register. The CRC verification uses a generator polynomial of $g(x) = X^3+X+1$, with a seed value = ‘111’. If a CRC error is detected in the writable register array, the IDE bit is set in the DEVSTAT register.

3.3 Voltage Regulators

Separate internal voltage regulators supply the analog and digital circuitry. External filter capacitors are required, as shown in Figure 1. The voltage regulator module includes voltage monitoring circuitry which indicates a device reset until the external supply and all internal regulated voltages are within predetermined limits. A reference generator provides a stable voltage which is used by the ΣΔ converters.

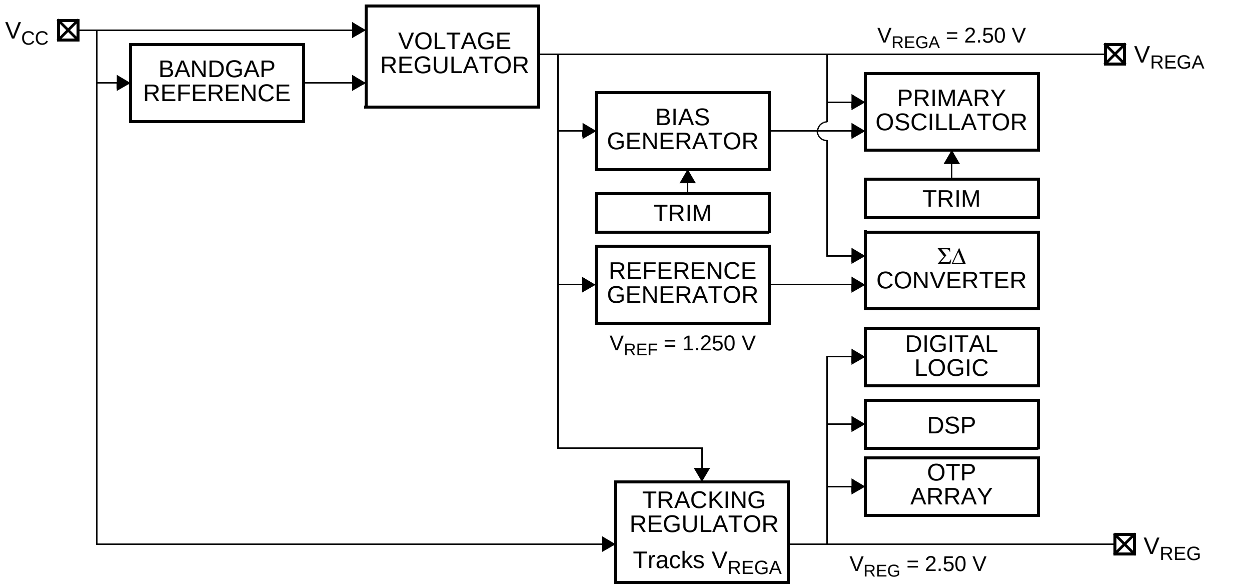


Figure 8. Power Supply Block Diagram

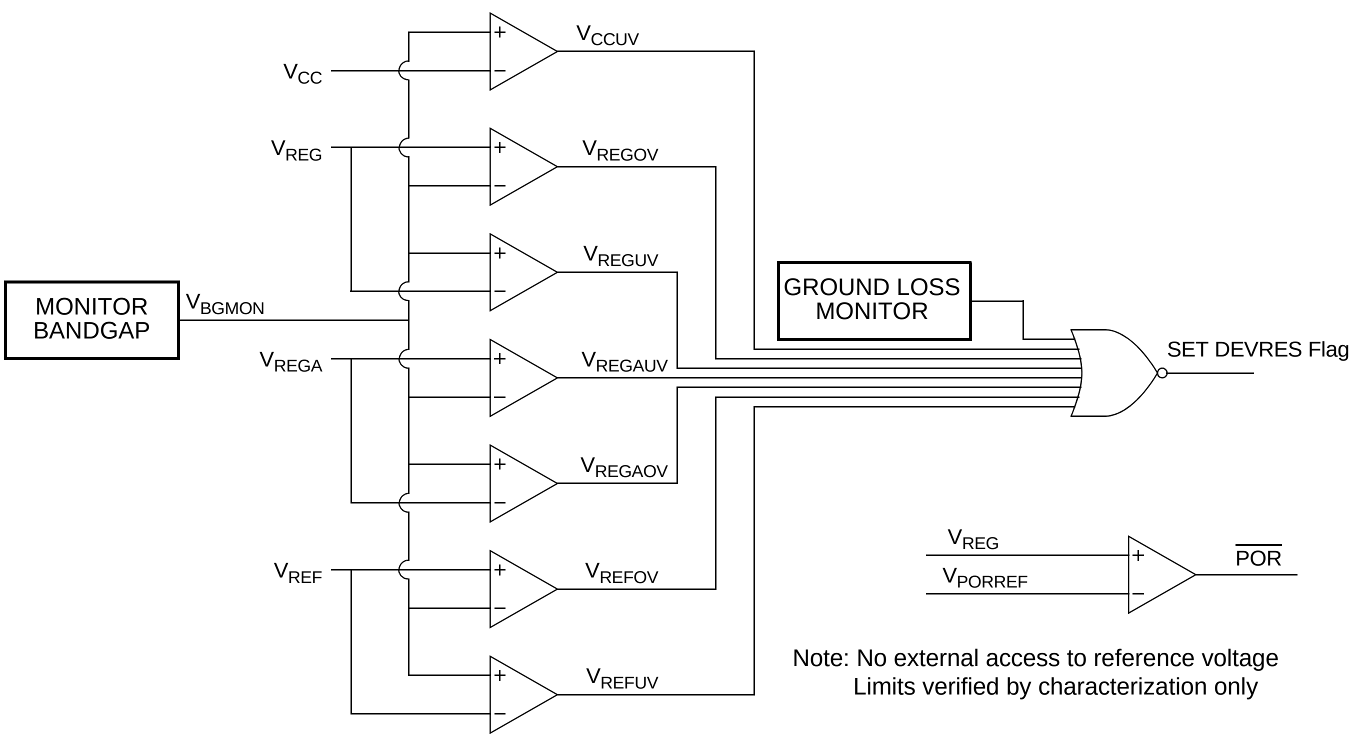


Figure 9. Voltage Monitoring

3.3.1 C_{VREG} Failure Detection

The digital supply voltage regulator is designed to be unstable with low capacitance. If the connection to the V_{REG} capacitor becomes open, the digital supply voltage will oscillate and cause either an under voltage, or over voltage failure within one internal sample time. This failure will result in one of the following:

1. The DEVRES flag in the DEVSTAT register will be set. The device will respond to SPI acceleration requests as defined in Table 30.
2. The device will be held in RESET and be non-responsive to SPI requests.

3.3.2 C_{VREGA} Failure Detection

The analog supply voltage regulator is designed to be unstable with low capacitance. If the connection to the V_{REGA} capacitor becomes open, the analog supply voltage will oscillate and cause either an under voltage, or over voltage failure within one internal sample time. The DEVRES flag in the DEVSTAT register will be set. The device will respond to SPI acceleration requests as defined in Table 30.

3.3.3 V_{SS} and V_{SSA} Ground Loss Monitor

The device detects the loss of ground connection to either V_{SS} or V_{SSA}. A loss of ground connection to V_{SS} will result in a V_{REG} overvoltage failure. A loss of ground connection to V_{SSA} will result in a V_{REG} undervoltage failure. Both failures result in a device reset.

3.3.4 SPI Initiated Reset

In addition to voltage monitoring, a device reset can be initiated by a specific series of three write operations involving the RES_1 and RES_0 bits in the DEVCTL register. Reference Section 3.1.5.1. for details regarding the SPI initiated reset.

3.4 Internal Oscillator

The device includes a factory trimmed oscillator as specified in Section 2.7.

3.4.1 Oscillator Monitor

The COUNT register in the customer accessible array is a read-only register which provides the current value of a free-running 8-bit counter derived from the primary oscillator. A 10-bit pre-scaler divides the primary oscillator by 1024. Thus, the value in the COUNT register increases by one count every 128 µs, and the register rolls over every 32.768 ms. The SPI master can periodically read the COUNT register, and verify the difference between subsequent register reads against the system time base.

1. The SPI access rates and deviations must be taken into account for this oscillator verification method.

3.4.2 CRC Based Clock Monitor

The device includes unique DSP cores for the X-Axis and Y-Axis. Each DSP core uses multiple frequencies derived from the oscillator, ranging from the base oscillator frequency to the base oscillator frequency divided by 256. In order to guarantee that the clocks for the two DSP cores are synchronized, a clock CRC monitor is employed. The CRC monitor is updated every cycle of the base oscillator.

3.5 Transducer

The transducer is an overdamped mass-spring-damper system described by the following transfer function:

$$H(s) = \frac{\omega_n^2}{s^2 + 2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2}$$

where:

ζ= Damping Ratio
ω_n= Natural Frequency = $2 * \Pi * f_n$

Reference Section 2.4 for transducer parameters.

3.6 Self Test Interface

When self test is enabled, the self test interface applies a voltage to the *g*-cell, causing a deflection of the proof mass. Once enabled, offset cancellation is suspended and the deflection results in an acceleration which is superimposed upon the input acceleration.

The resulting acceleration readings can be compared either against absolute limits, or the values stored in the Self Test Deflection Registers (Reference Section 3.1.2). The self test interface is controlled through SPI write operations to the DEVCFG_X and DEVCFG_Y registers described in Section 3.1.7 only if the ENDINIT bit in the DEVCFG register is cleared. A diagram of the self test interface is shown in Figure 10.

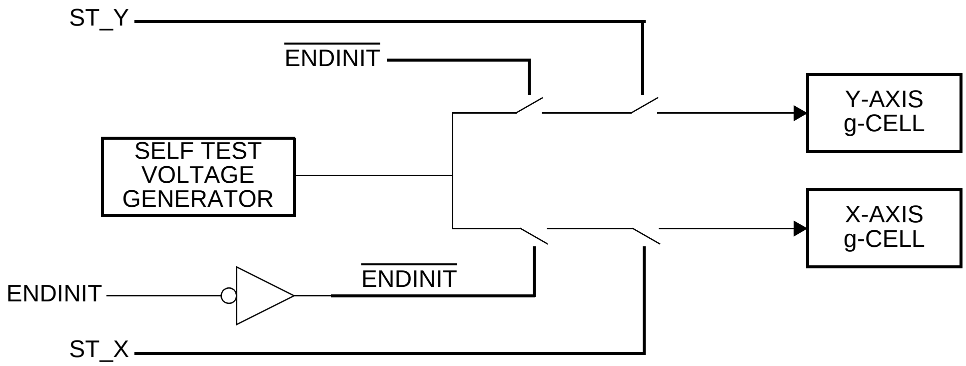


Figure 10. Self Test Interface

3.6.1 Raw Self Test Deflection Verification

The raw self test deflection can be directly verified against raw self test limits listed in Section 2.4.

3.6.2 Delta Self Test Deflection Verification

The raw self test deflection can be verified against the ambient temperature self test deflection value recorded at the time the device was produced. The production self test deflection is stored in the STDEFL_X and STDDEFL_Y registers such that the minimum stored value (0x00) is equivalent to ΔST_{MIN}, and the maximum stored value (0xFF) is equivalent to ΔST_{MAX}. The Delta Self Test Deflection limits can then be determined by the following equations:

$$\Delta ST_{ACCMINLIMIT} = FLOOR \cdot \left[\left(\Delta ST_{MIN} + \left[\frac{\Delta STDEFLx_{CNTS}}{255}\right] \times [\Delta ST_{MAX} - \Delta ST_{MIN}]\right) \times (1 - \Delta ST_{ACC})\right]$$

$$\Delta ST_{ACCMAXLIMIT} = CEIL \cdot \left[\left(\Delta ST_{MIN} + \left[\frac{\Delta STDEFLx_{CNTS}}{255}\right] \times [\Delta ST_{MAX} - \Delta ST_{MIN}]\right) \times (1 + \Delta ST_{ACC})\right]$$

where:

ΔST_{ACC}	The accuracy of the self test deflection relative to the stored deflection as specified in Section 2.4.
$\Delta STDEFLx_{CNTS}$	The value stored in the STDEFL_X or STDEFL_Y register.
ΔST_{MIN}	The minimum self test deflection at 25C as specified in Section 2.4.
ΔST_{MAX}	The maximum self test deflection at 25C as specified in Section 2.4.

3.7 ΣΔ Converter

A sigma delta converter provides the interface between the transducer and the DSP. The output of the ΣΔ converter is a data stream at a nominal frequency of 1 MHz.

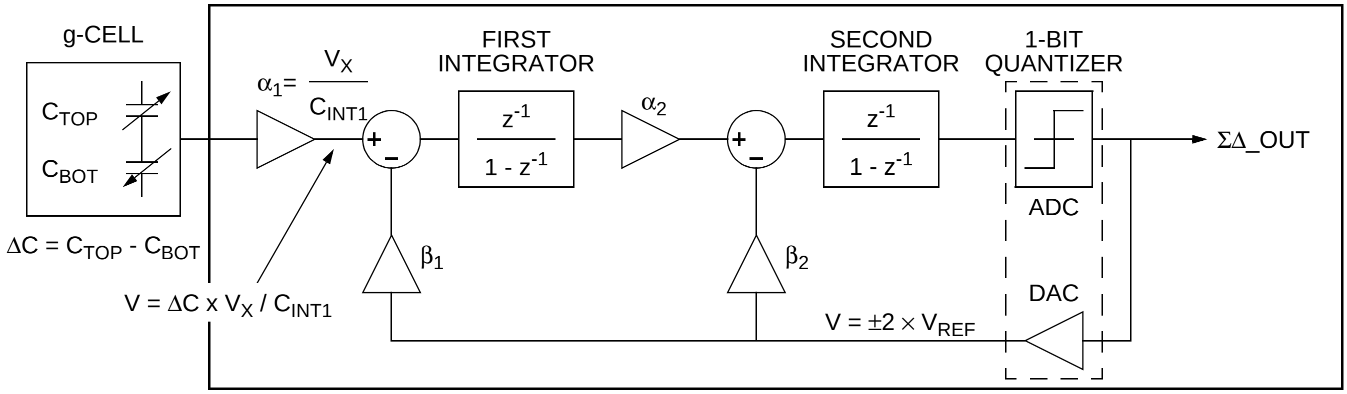


Figure 11. ΣΔ Converter Block Diagram

3.8 Digital Signal Processing Block

A digital signal processing (DSP) block is used to perform signal filtering and compensation operations. A diagram illustrating the signal processing flow is shown in Figure 12.

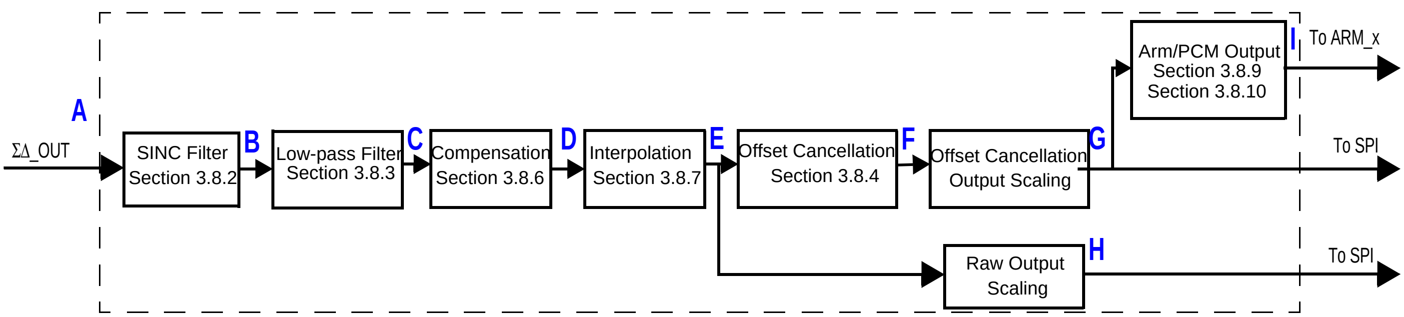


Figure 12. Signal Chain Diagram

Table 26. Signal Chain Characteristics

	Description	Sample Time (µs)	Data Width Bits	Over Range Bits	Effective Bits	Rounding Resolution Bits	Typical Block Latency	Reference
A	ΣΔ	1	1		1		3.2µs	Section 3.7
B	SINC Filter	8	14		13		11.2µs	Section 3.8.2
C	Low-pass Filter	8/16	20	4	12	4	Reference Section 3.8.3	Section 3.8.3
D	Compensation	8/16	20	4	12	4	7.875µs	Section 3.8.6
E	Interpolation	4/8	20	4	12	4	t_s / 2	Section 3.8.8
F	Offset Cancellation	256	20	4	12	4	N/A	Section 3.8.4
GH	SPI Output	4/8	—	—	12	—	t_s / 2	
I	PCM Output	4/8	—	—	9	—		Section 3.8.11

3.8.1 DSP Clock

The DSP is clocked at 8 MHz, with an effective 6MHz operating frequency. The clock to the DSP is disabled for 1 clock prior to each edge of the ΣΔ modulator clock to minimize noise during data conversion.

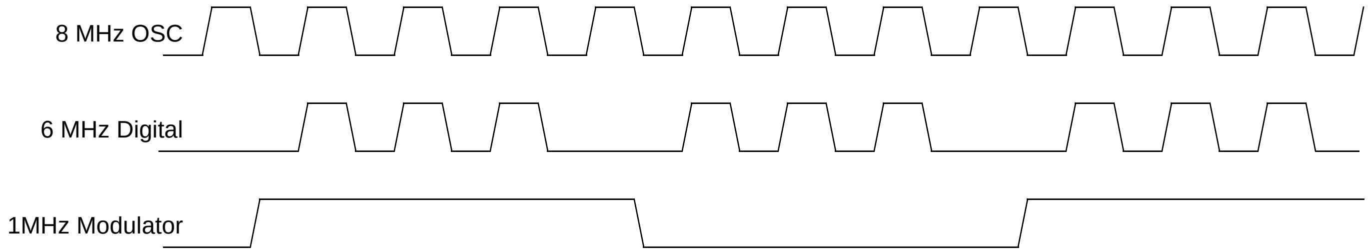


Figure 13. Clock Generation

3.8.2 Decimation Sinc Filter

The serial data stream produced by the ΣΔ converter is decimated and converted to parallel values by a 3rd order 16:1 sinc filter with a decimation factor of 8 or 16, depending on the Low-pass Filter selected.

$$H(z) = \left[\frac{1 - z^{-16}}{16 \times (1 - z^{-1})}\right]^3$$

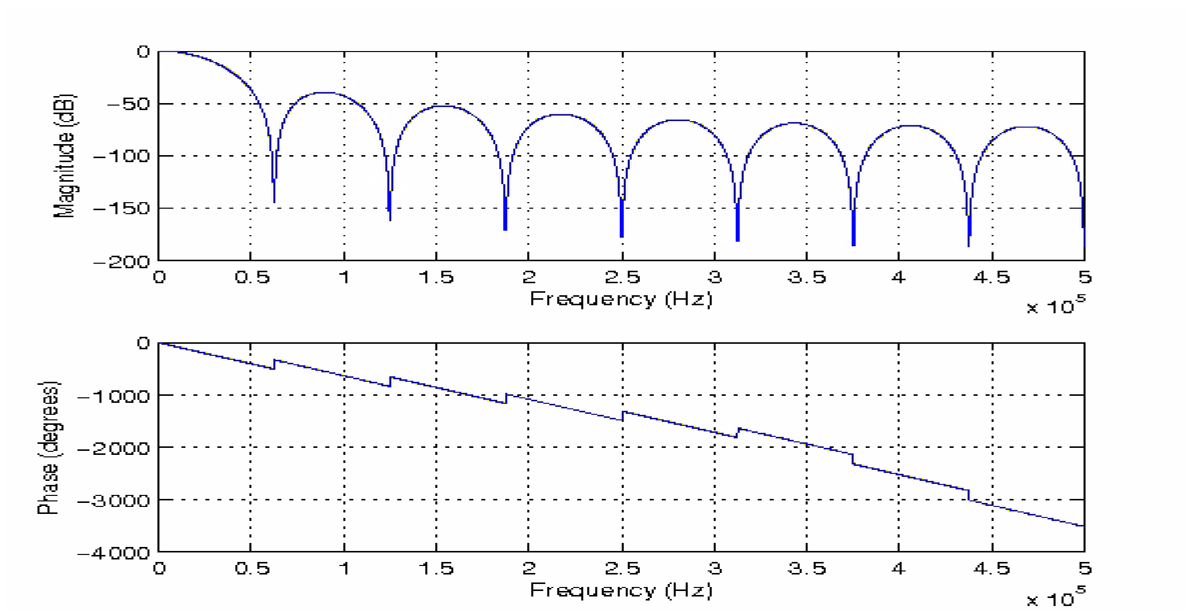


Figure 14. Sinc Filter Response, t_S = 8 µs

3.8.3 Low-pass Filter

Data from the Sinc filter is processed by an infinite impulse response (IIR) low-pass filter.

.

$$H(z) = \frac{n_0 + (n_1 \cdot z^{-1}) + (n_2 \cdot z^{-2}) + (n_3 \cdot z^{-3}) + (n_4 \cdot z^{-4})}{d_0 + (d_1 \cdot z^{-1}) + (d_2 \cdot z^{-2}) + (d_3 \cdot z^{-3}) + (d_4 \cdot z^{-4})}$$

The device provides the option for one of twelve low-pass filters. The filter is selected independently for each axis with the LPF_X[3:0] and LPF_Y[3:0] bits in the DEVCFG_X and DEVCFG_Y registers. The filter selection options are listed in Section 3.1.7.3, Table 11. Response parameters for the low-pass filter are specified in Section 2.4. Filter characteristics are illustrated in the figures on the following pages.

Table 27. Low-pass Filter Coefficients

Filter Number	LPF_X/ LPF_Y Value (HEX)	Description -3dB Frequency (±5%)	Filter Order	Sample Time (μs ±5%)	Filter Coefficients				Group Delay	Self Test Step Response (ms)
8	0x08	50 Hz LPF	4	16	n_0	2.08729034056887e-10	d_0	1	26816/ f_{osc}	14.00
					n_1	8.349134489240434e-10	d_1	-3.976249694824219		
					n_2	1.25237777794924e-09	d_2	5.929003009577855		
0	0x00	100 Hz LPF	4	8	n_3	8.349103355433541e-10	d_3	-3.929255528257727		7.00
					n_4	2.087307211059861e-10	d_4	0.9765022168437554		
9	0x09	150 Hz LPF	4	16	n_0	1.639127731323242e-08	d_0	1	9024/ f_{osc}	6.00
					n_1	6.556510925292969e-08	d_1	-3.928921222686768		
					n_2	9.834768482194806e-08	d_2	5.789028996785419		
1	0x01	300 Hz LPF	4	8	n_3	6.556510372902331e-08	d_3	-3.791257019240902		3.00
					n_4	1.639128257923422e-08	d_4	0.9311495074496179		
10	0x0A	200 Hz LPF	4	16	n_0	5.124509334564209e-08	d_0	1	6784/ f_{osc}	5.00
					n_1	2.049803733825684e-07	d_1	-3.905343055725098		
					n_2	3.074705789151505e-07	d_2	5.72004239520561		
2	0x02	400 Hz LPF	4	8	n_3	2.049803958150164e-07	d_3	-3.723967810019985		2.50
					n_4	5.124510693742625e-08	d_4	0.9092692903507213		
13	0x0D	200 Hz LPF	3	16	n_0	2.720393240451813e-06	d_0	1	5632/ f_{osc}	4.80
					n_1	8.161179721355438e-06	d_1	-2.931681632995605		
					n_2	8.161180123840722e-06	d_2	2.865296718275204		
5	0x05	400 Hz LPF	3	8	n_3	2.720393634345496e-06	d_3	-0.9335933215174919		2.40
					n_4	0	d_4	0		
11	0x0B	400 Hz LPF	4	16	n_0	7.822513580322266e-07	d_0	1	3392/ f_{osc}	2.50
					n_1	3.129005432128906e-06	d_1	-3.811614513397217		
					n_2	4.693508163398543e-06	d_2	5.450666051045118		
3	0x03	800 Hz LPF	4	8	n_3	3.129005428784364e-06	d_3	-3.465805771100349		1.70
					n_4	7.822513604678875e-07	d_4	0.8267667478030489		
12	0x0C	500 Hz LPF	4	16	n_0	1.865386962890625e-06	d_0	1	2688/ f_{osc}	3.20
					n_1	7.4615478515625e-06	d_1	-3.765105724334717		
					n_2	1.119232176112846e-05	d_2	5.319861050818872		
4	0x04	1000 Hz LPF	4	8	n_3	7.4615478515625e-06	d_3	-3.34309015036024		1.60
					n_4	1.865386966264658e-06	d_4	0.7883646729233078		

Note: Low-pass Filter figures do not include *g*-cell frequency response.

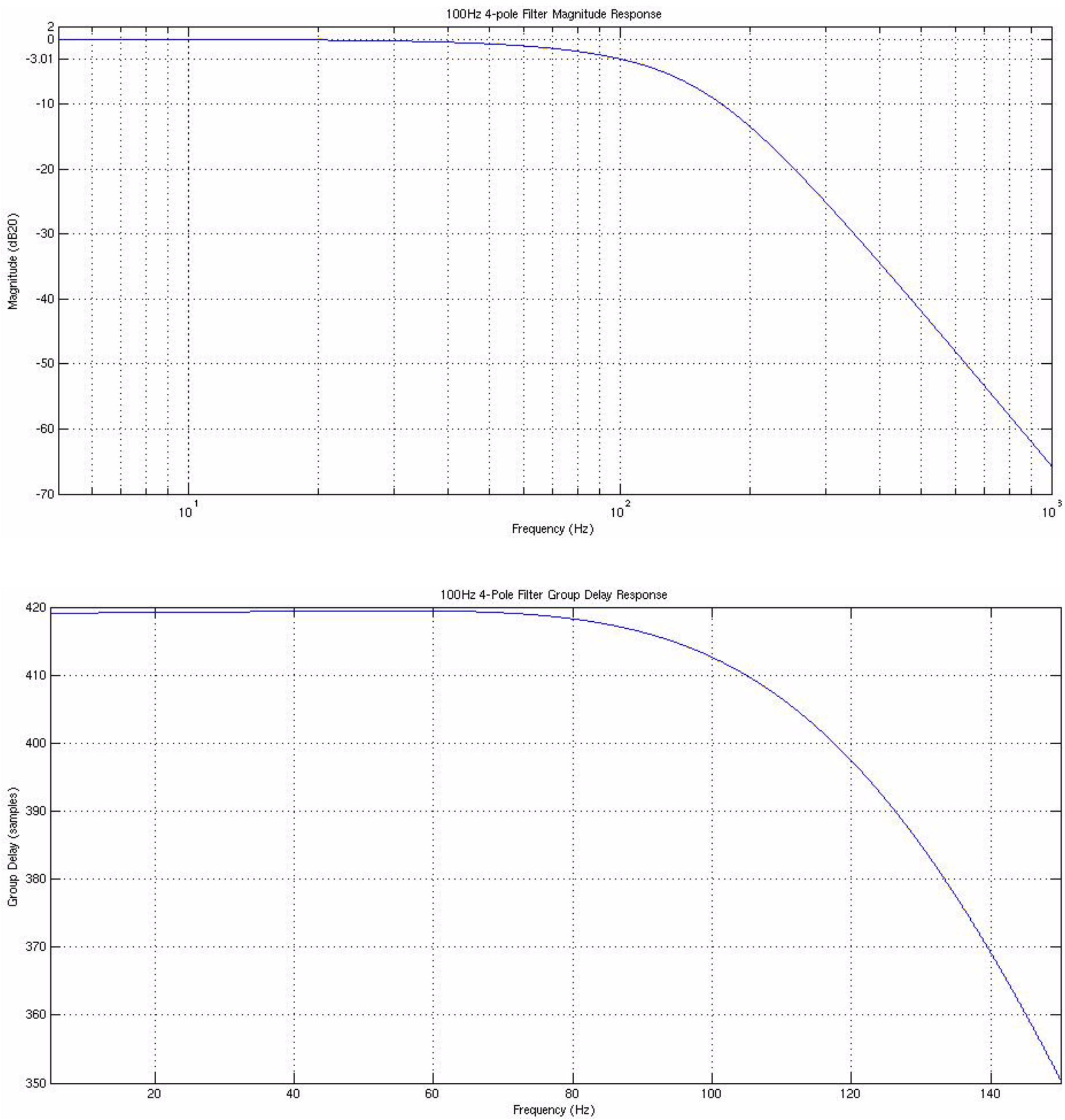


Figure 15. Low-Pass Filter Characteristics: f_C = 100 Hz, Poles = 4, t_S = 8 µs

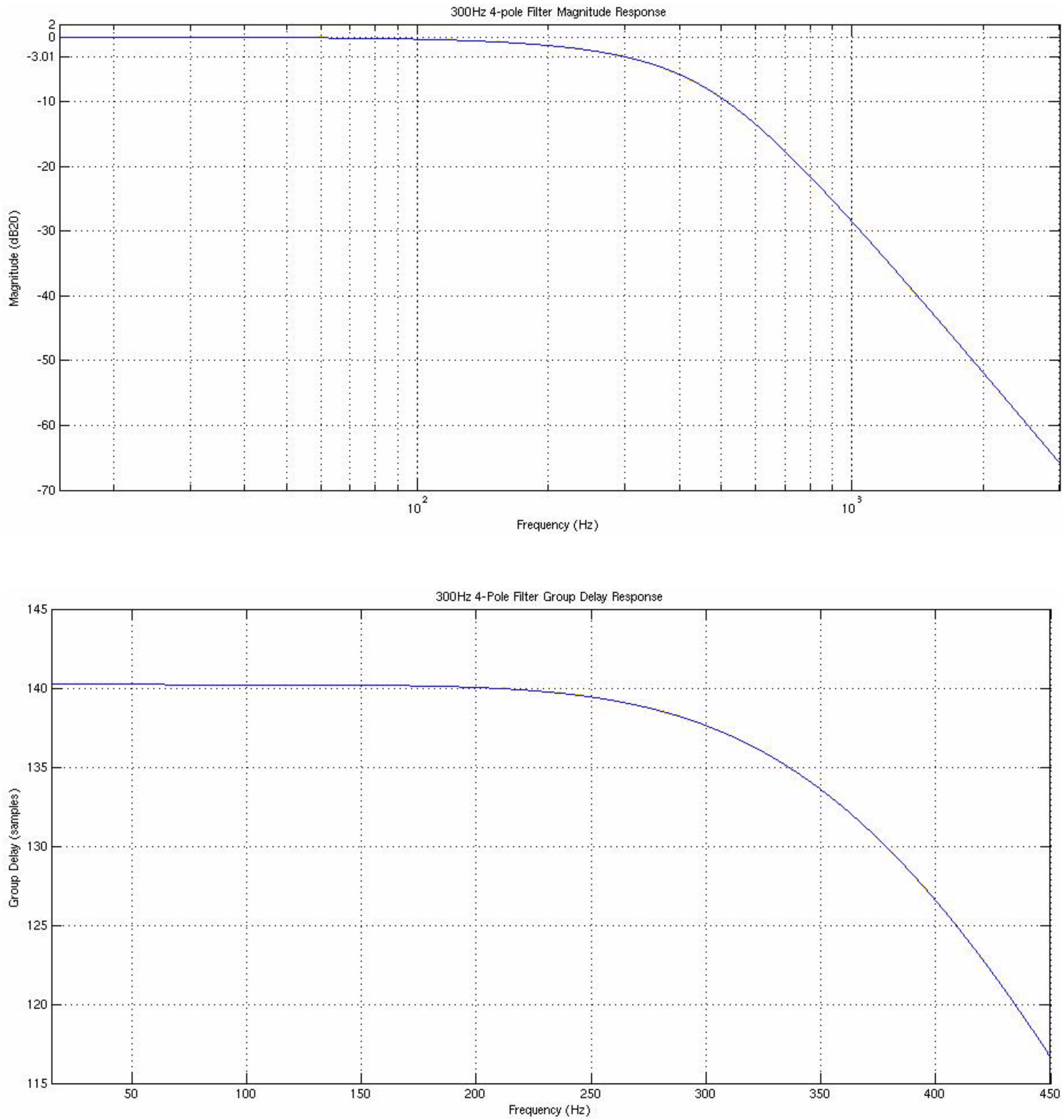


Figure 16. Low-Pass Filter Characteristics: f_C = 300 Hz, Poles = 4, t_S = 8 μs

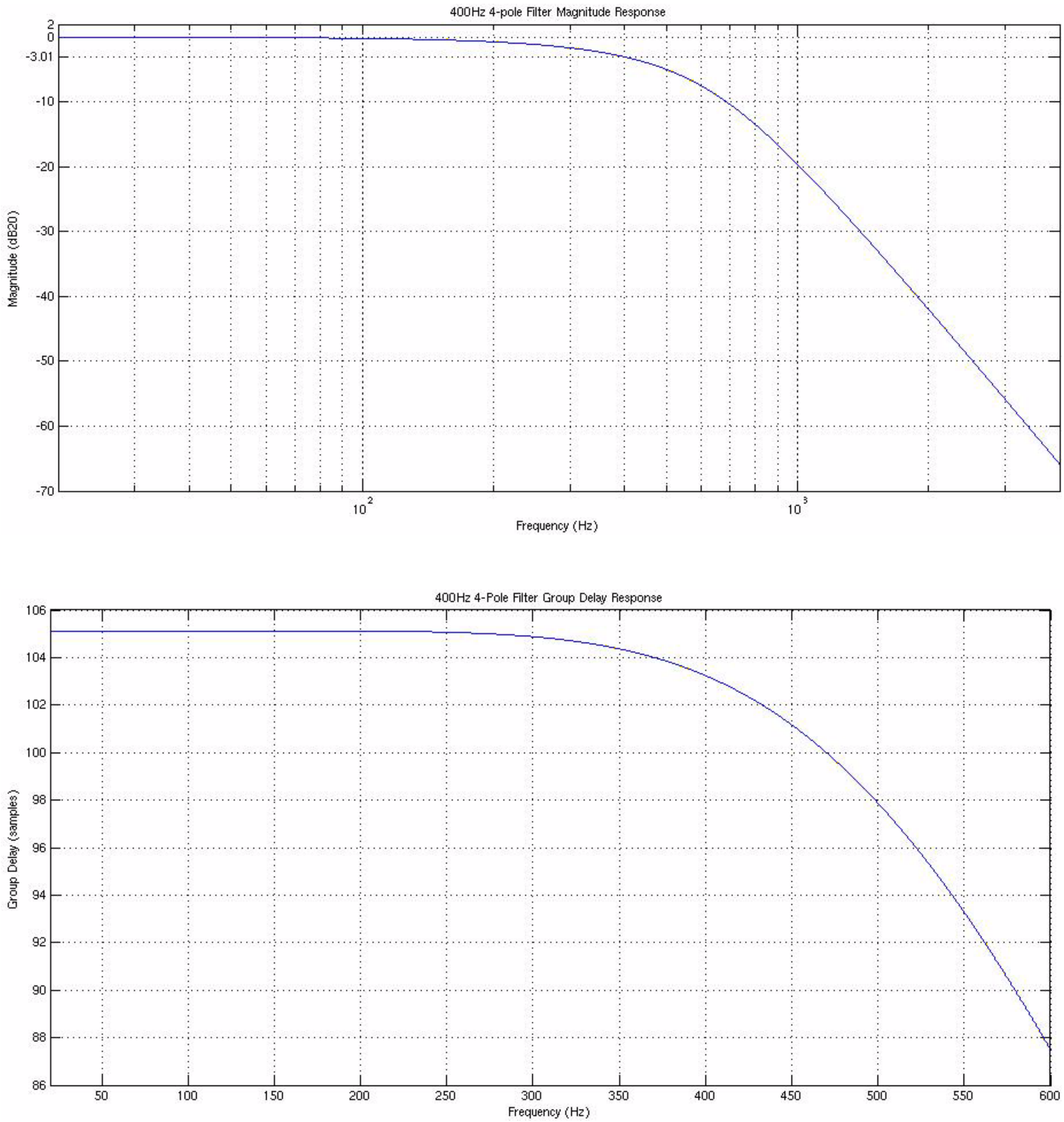
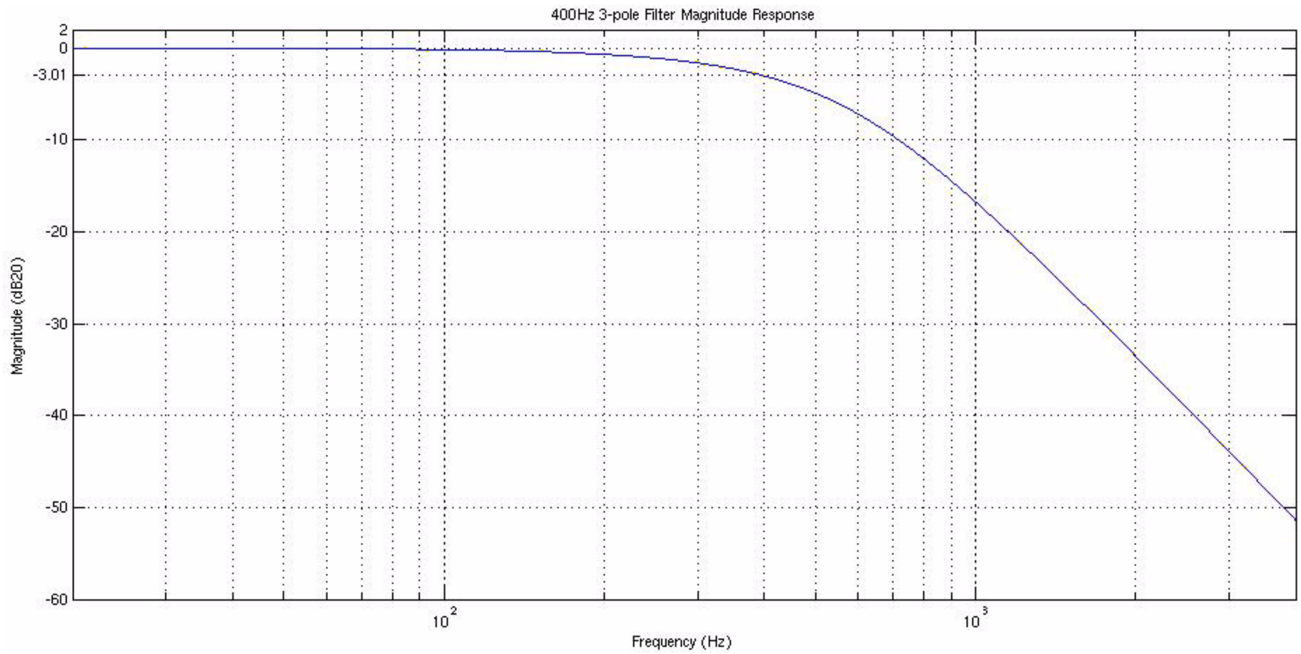


Figure 17. Low-Pass Filter Characteristics: f_C = 400 Hz, Poles = 4, t_S = 8 μs



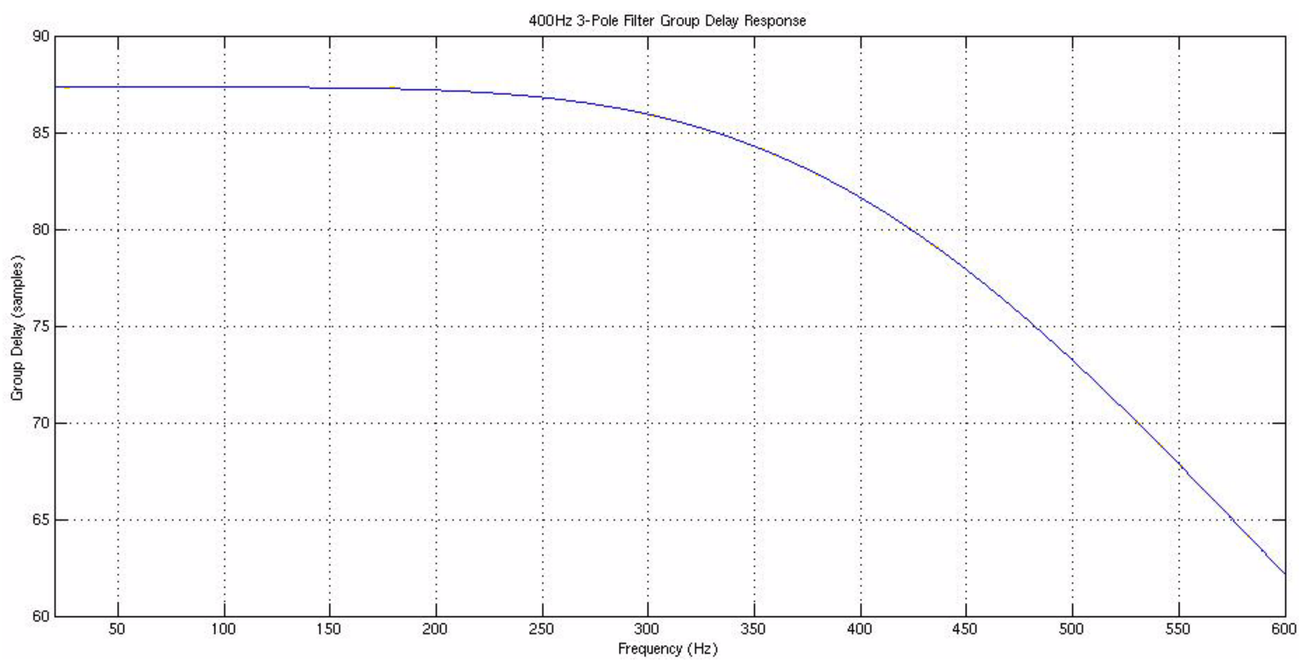


Figure 18. Low-Pass Filter Characteristics: f_C = 400 Hz, Poles = 3, t_S = 8 μs

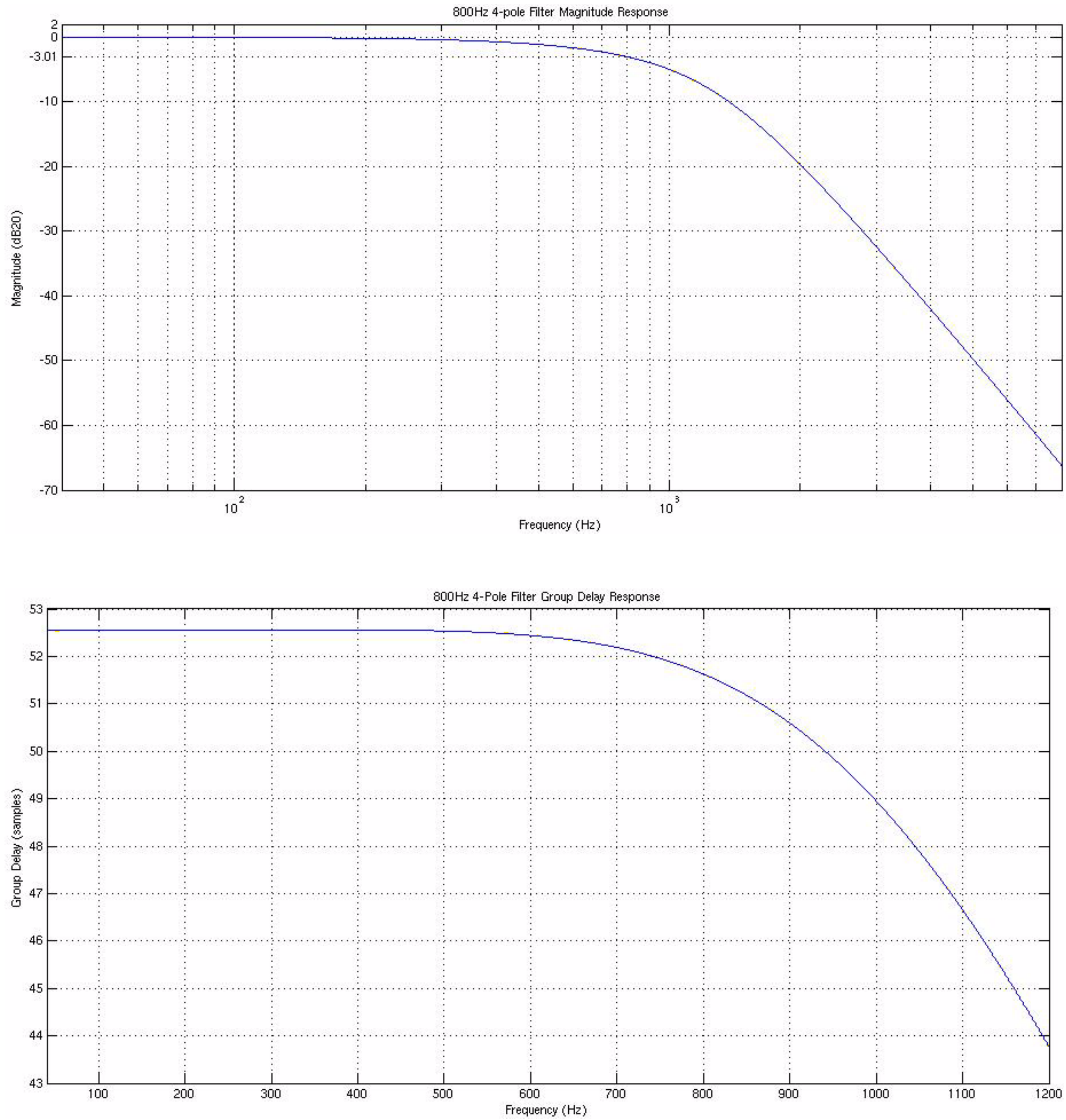
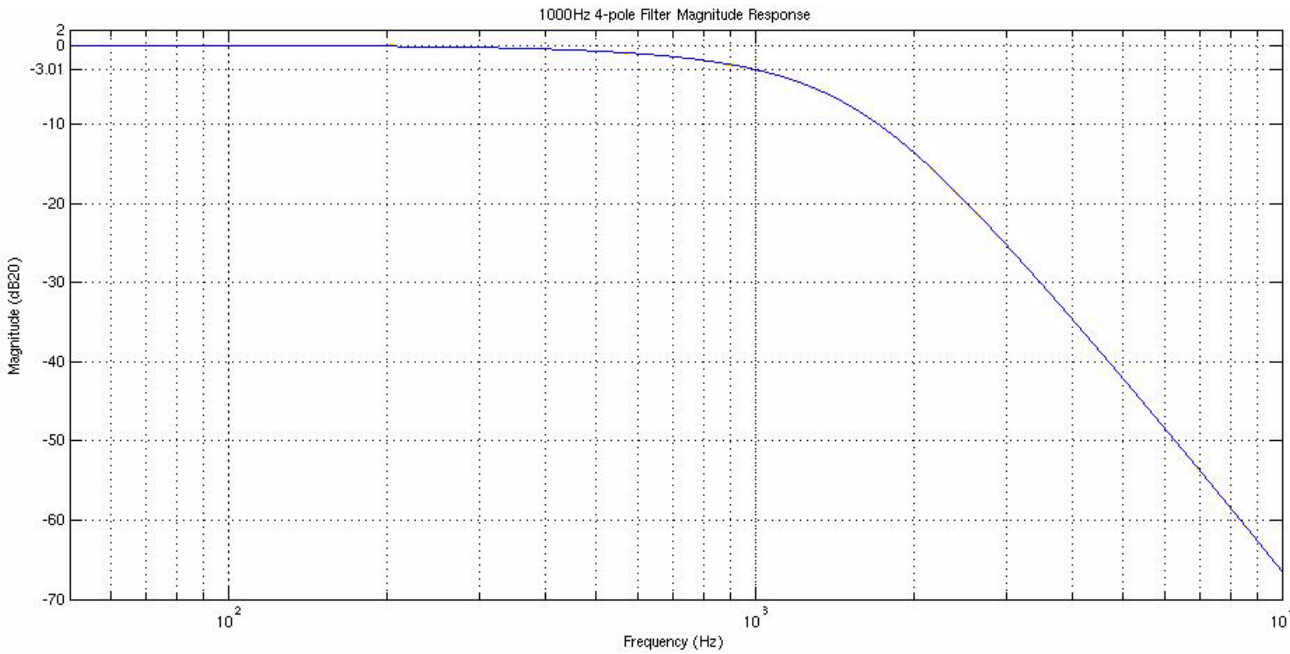


Figure 19. Low-Pass Filter Characteristics: f_C = 800 Hz, Poles = 4, t_S = 8 μs



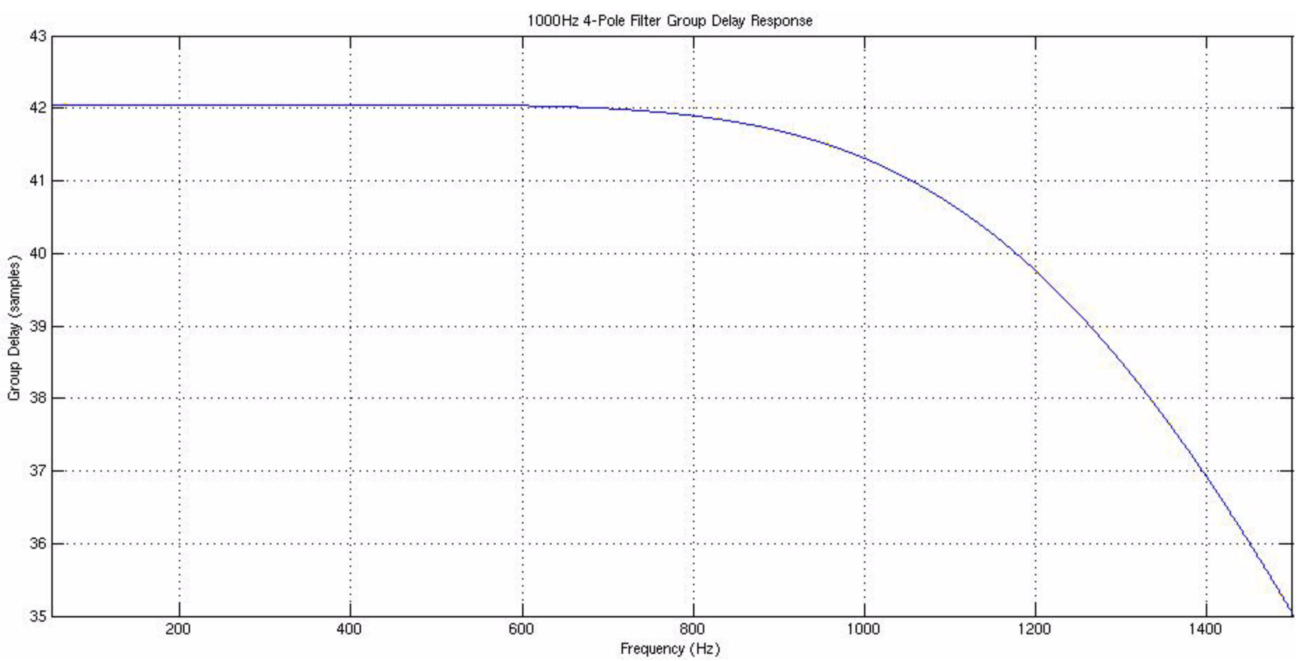


Figure 20. Low-Pass Filter Characteristics: f_C = 1000 Hz, Poles = 4, t_S = 8 μs

3.8.4 Offset Cancellation

The device provides the option to read offset cancelled acceleration data via the SPI by clearing the $\overline{OC}$ bit in the DEVCFG register (reference Section 3.1.6.1) and in the SPI command (reference Section 4.1). A block diagram of the offset cancellation is shown in Figure 21, and response parameters are specified in Section 2.4 and in Table 28.

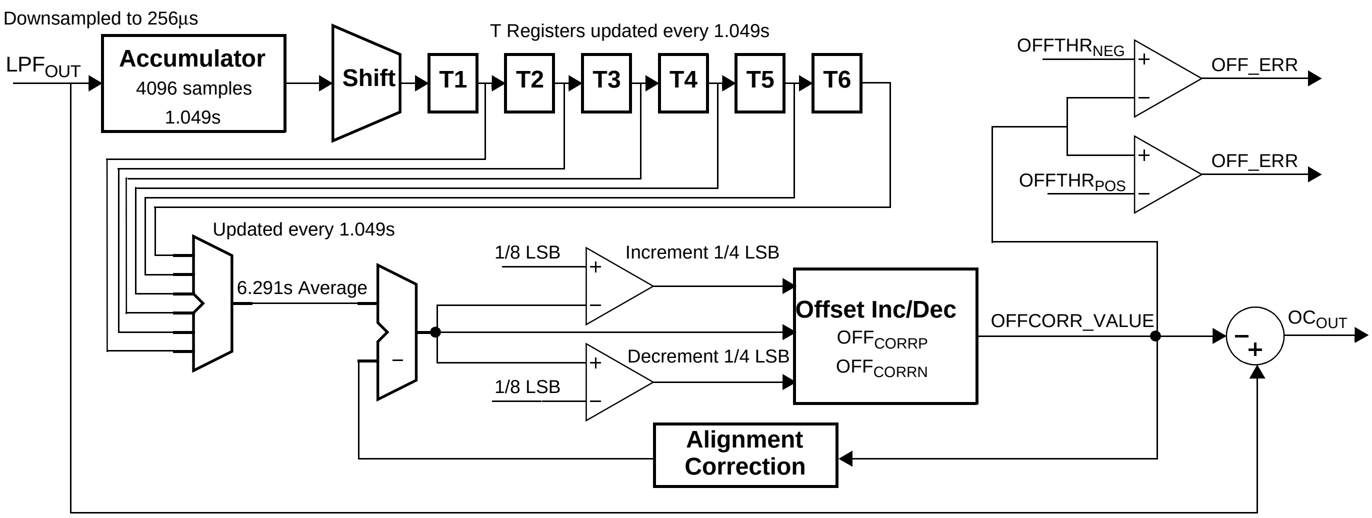


Figure 21. Offset Cancellation Block Diagram

In normal operation, the offset cancellation circuit computes a 24,576 sample running average of the acceleration data downsampled to 256 µs. The running average is compared against positive and negative thresholds to determine the offset correction value that will be applied to the acceleration data.

During start up, three phases of moving average sizes are used to allow for faster convergence of misuse input signals. Reference Table 28 for offset cancellation timing information during startup and normal operation. The offset cancellation startup phase can also be directly controlled during initialization (ENDINIT = ‘0’) using the OCPHASE[1:0] bits and the OFFCFG_EN bit in the DEVCTL register, as described in Section 3.1.5.2 and Section 3.1.5.3.

Table 28. Offset Cancellation Timing Specifications

Phase	Start Time of Phase (from POR)	Typical Time in Phase (ms)	# of Samples in Phase	Samples Averaged	OFFCORR_VALUE Update Rate (ms)	Averaging Period (ms)	Maximum Slew Rate (LSB/s)	Averaging Filter -3dB Frequency (Hz)
Start 1	t_{OP}	524.288	2048	48	2.048	12.288	122.1	36.05
Start 2	t_{OP} + 524.288	524.288	2048	384	16.38	98.304	15.26	4.506
Start 3	t_{OP} + 1048.576	524.288	2048	3072	131.1	786.432	1.907	0.5632
Normal	t_{OP} + 1572.864	—	—	24576	1049	6291.456	0.2384	0.07040

When the self test circuitry is active, the offset cancellation block and the offset monitor block are suspended, and the offset correction value is constant. Once the self test circuitry is disabled, the offset cancellation block remains suspended for the time t_{ST_OMB} to allow the acceleration output to return to it’s nominal offset.

3.8.5 Offset Monitor

The device provides the option for an offset monitor circuit. The offset monitor circuit is enabled when the OFMON bit in the DEVCFG register is programmed to a logic ‘1’. The output of the offset cancellation circuit is compared against a high and low threshold. If the offset correction value exceeds either the $OFFTHR_{POS}$, or $OFFTHR_{NEG}$ threshold, an Offset Over Range Error condition is indicated.

The offset correction value update rate is listed in Table 28: “Maximum Slew Rate”. Because the offset monitor uses this value, the offset monitor will also update at this rate. The time to indicate an Offset Over Range Error is dependent upon the input signal.

The offset monitor status remains suspended during self test, because the offset monitor is based on the offset cancellation circuit, which is also suspended during self test. The offset monitor is disabled for 2.1 seconds following reset regardless of the state of the OFMON bit.

3.8.6 Signal Compensation

The device includes internal OTP and signal processing to compensate for sensitivity error and offset error. This compensation is necessary to achieve the specified parameters in Section 2.4.

3.8.7 Output Scaling

The 20 bit digital output from the DSP is clipped and scaled to a 12-bit data word which spans the acceleration range of the device. Figure 22 shows the method used to establish the output acceleration data word from the DSP output.

Over Range				**Signal**												**Noise**			
D19	**D18**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
12-Bit Data Word				**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	Using Rounding			

Figure 22. 12-Bit Output Scaling Diagram

3.8.8 Data Interpolation

The device includes 2 to 1 data interpolation to minimize the system sample jitter. Each result produced by the digital signal processing chain is delayed one half of a sample time, and the interpolated value of successive samples is provided between sample times. This operation is illustrated below.

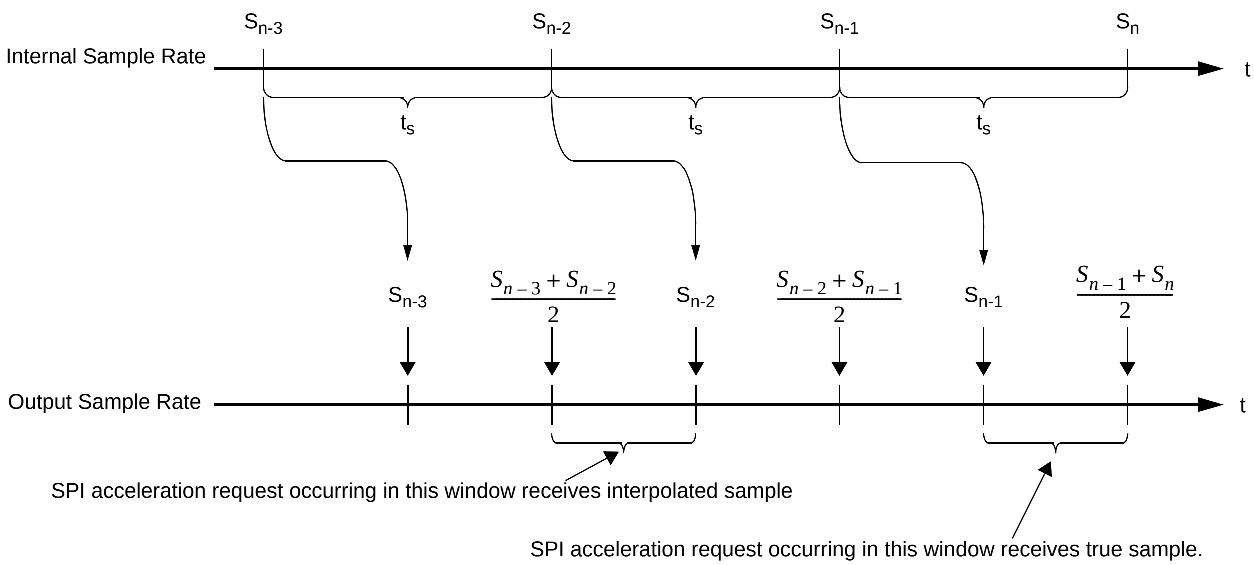


Figure 23. Data Interpolation Timing

The effect of this interpolation at the system level is a 50% reduction in sample jitter. Figure 24 shows the resulting output data for an input signal.

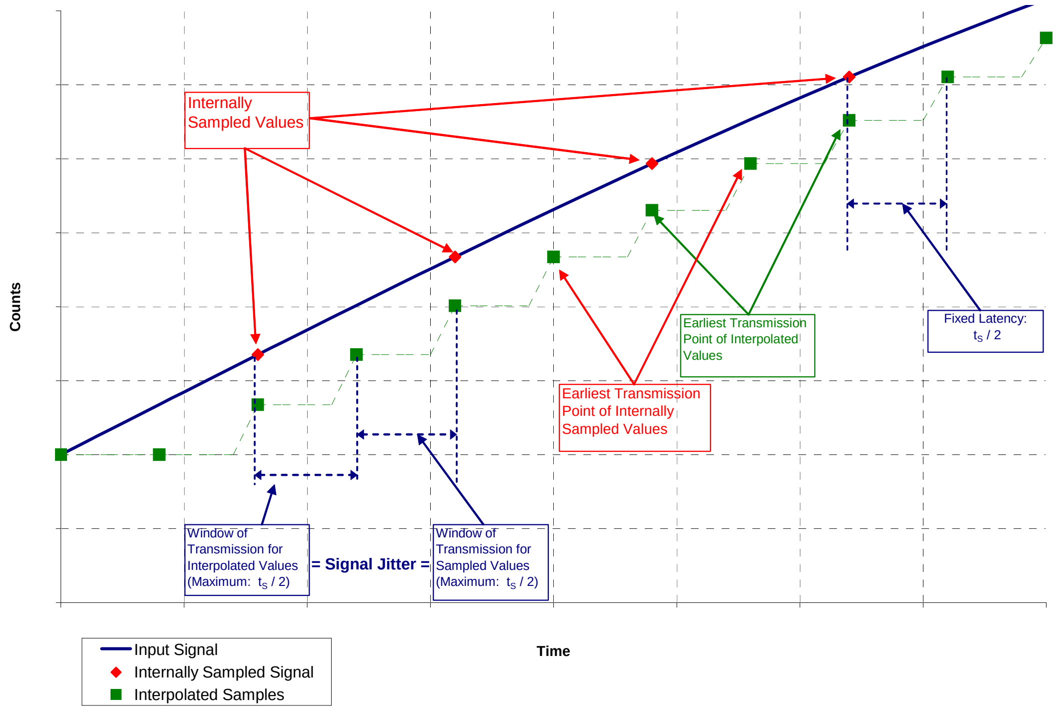


Figure 24. Data Interpolation Example

3.8.9 Acceleration Data Timing

The SPI uses a request/response protocol, where a SPI transfer is completed through a sequence of 2 phases. Reference Section 4 for more details regarding the SPI protocol. The device latches the associated data for an acceleration request at the rising edge of $\overline{CS}$. The most recent sample available from the DSP (including interpolation) is latched, and transmitted during the subsequent SPI transfer.

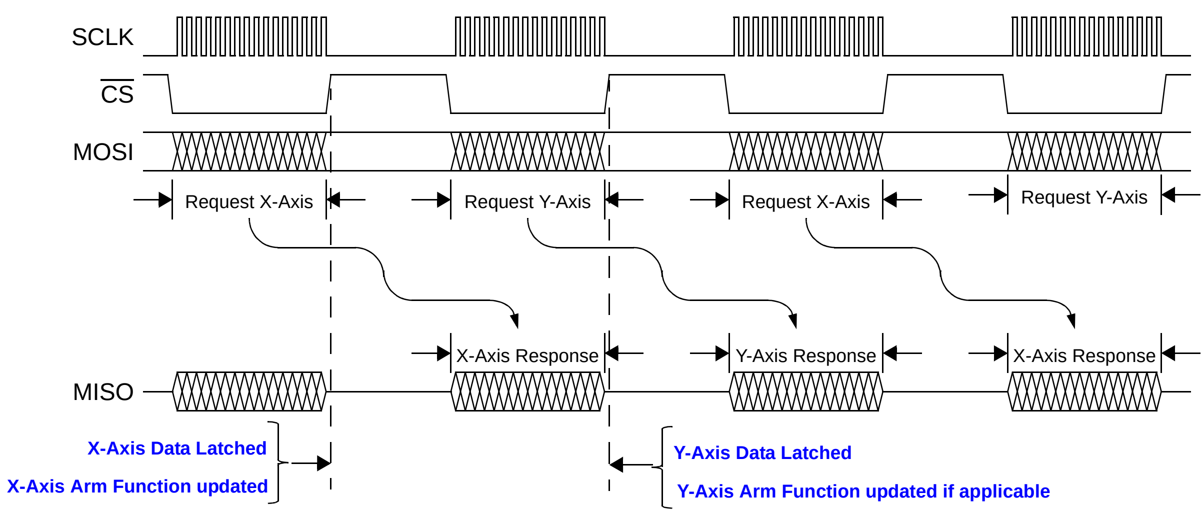


Figure 25. Acceleration Data Timing

3.8.10 ARMING FUNCTION

The device provides the option for an arming function with 3 modes of operation. The operation of the arming function is selected by the state of the A_CFG bits in the DEVCFG register.

Reference Section 4.5 for the operation of the Arming function with exception conditions. Error conditions do not impact prior arming function responses. If an error occurs after an arming activation, the corresponding pulse stretch for the existing arming condition will continue. However, new acceleration reads will not update the arming function regardless of the acceleration value.

3.8.10.1 Arming Function: Moving Average Mode

In moving average mode, the arming function runs a moving average on the offset cancelled output of each acceleration axis. The number of samples used for the moving average (k) is programmable via the AWS_Xx[1:0] and ARM_Yx[1:0] bits in the ARMCFGX and ARMCFGY registers. Reference Section 3.1.8 for register details.

$$ARM\_MA_n = (OC_n + OC_{n-1} + \ldots + OC_{n+1-k})/k$$

Where n is the current sample.

The sample rate for each axis is determined by the SPI acceleration data sample rate. At the rising edge of $\overline{CS}$ for an acceleration data SPI request, the moving average for the associated axis is updated with a new sample. Reference Figure 28. The SPI acceleration data sample rate must meet the minimum time between requests ($t_{ACC\_REQ\_x}$) specified in Section 2.6.

The moving average output is compared against positive and negative 8-bit thresholds that are individually programmed for each axis via the ARMT_Xx and ARMT_Yx registers. Reference Section 3.1.10 for register details. If the moving average equals or exceeds either threshold, an arming condition is indicated, the ARM_X or ARM_Y output is asserted for the associated axis, and the pulse stretch counter is set as described in Section 3.8.10.4.

The ARM_X or ARM_Y output is de-asserted only when the pulse stretch counter expires. Figure 28 shows the arming output operation for different SPI conditions.

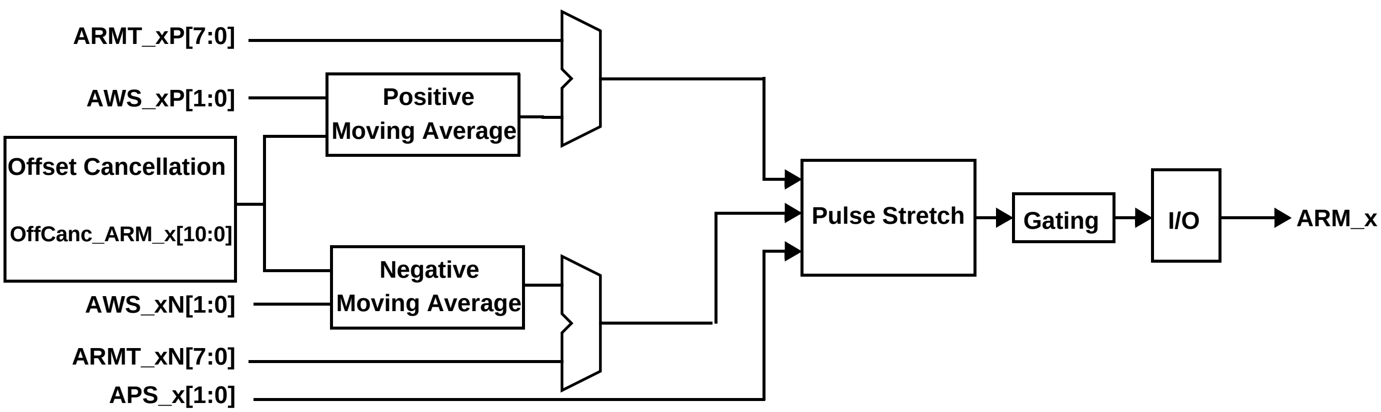


Figure 26. Arming Function Block Diagram - Moving Average Mode

The moving average window size must be set prior to setting the arming function to moving average mode, or prior to requesting acceleration data via the SPI. If the moving average window size is changed after enabling moving average mode, the arming function must first be disabled by setting the A_CFG bits to “000”. Once the desired moving average window size is set, the moving average mode can be re-enabled.

3.8.10.2 Arming Function: Count Mode

In count mode, the arming function compares each offset cancelled sample against positive and negative thresholds that are individually programmed for each axis via the ARMT_Xx and ARMT_Yx registers. Reference Section 3.1.10 for register details. If the sample equals or exceeds either threshold, a sample counter is incremented. If the sample does not exceed either threshold, the sample counter is reset to zero.

The sample rate for each axis is determined by the SPI acceleration data sample rate. At the rising edge of $\overline{CS}$ for an acceleration data SPI request, a new sample for the associated axis is compared against the thresholds. Reference Figure 28. The SPI acceleration data sample rate must meet the minimum time between requests ($t_{ACC\_REQ\_x}$) specified in Section 2.6.

A sample count limit is programmable via the AWS_Xx[1:0] and AWS_Yx[1:0] bits in the ARMCFGX and ARMCFGY registers. If the sample count reaches the programmable sample count limit, an arming condition is indicated, the ARM_X or ARM_Y output is asserted for the associated axis, and the pulse stretch counter is set as described in Section 3.8.10.4.

The ARM_X or ARM_Y output is de-asserted only when the pulse stretch counter expires. Figure 28 shows the arming output operation for different SPI conditions.

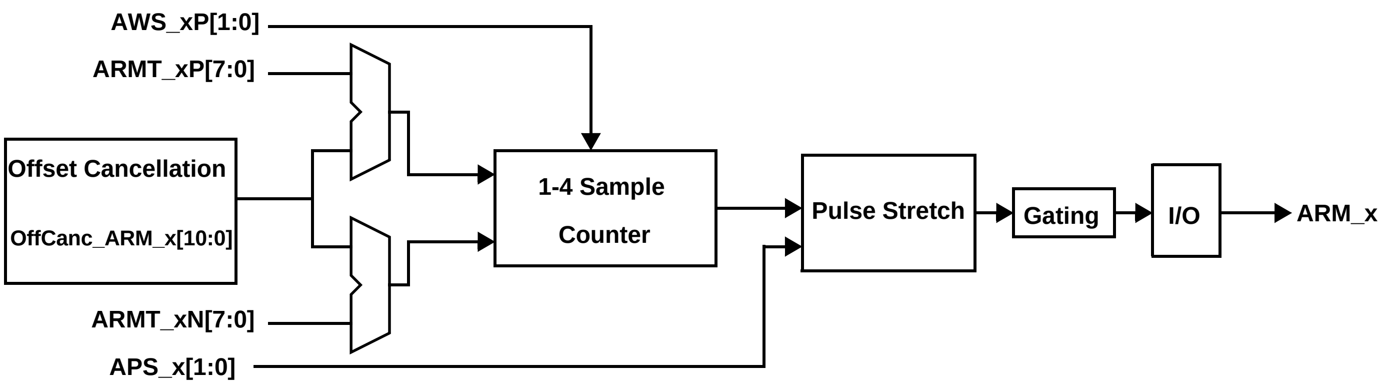


Figure 27. Arming Function Block Diagram - Count Mode

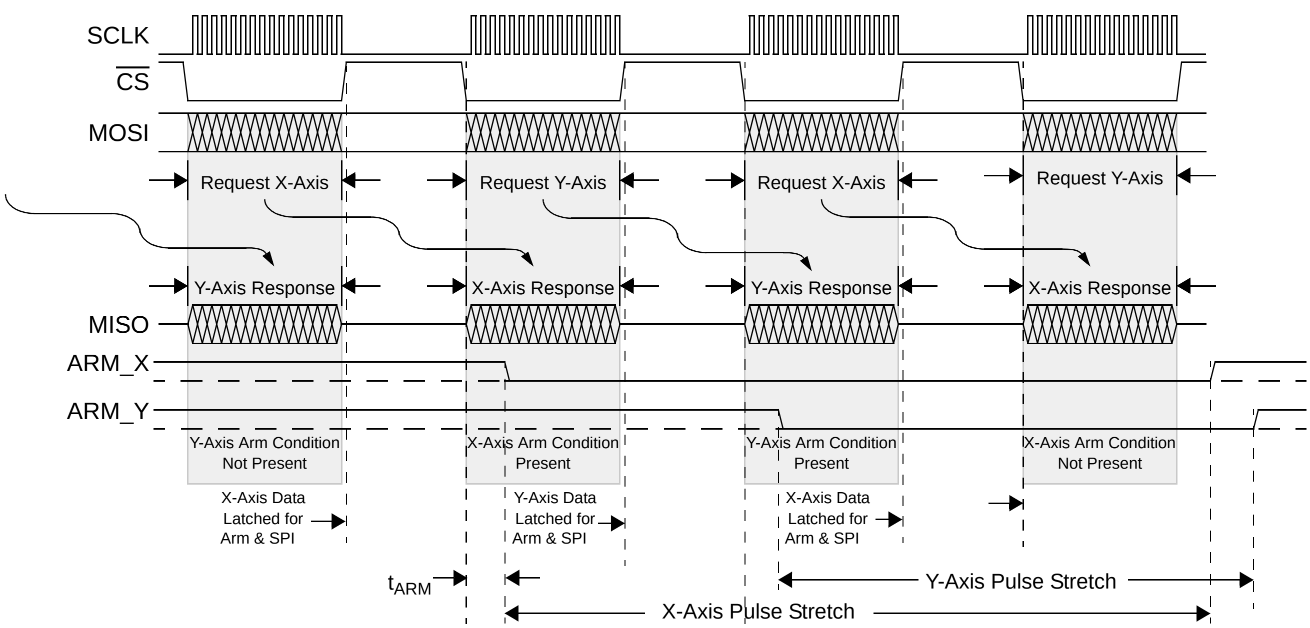


Figure 28. X and Y Axis Arming Conditions, Moving Average and Count Mode

3.8.10.3 Arming Function: Unfiltered Mode

On the rising edge of $\overline{CS}$ for an acceleration request, the most recent available offset cancelled sample for the requested axis is compared against positive and negative thresholds that are individually programmed for each axis via the ARMT_Xx and ARMT_Yx registers. Reference Section 3.1.10 for register details. If the sample equals or exceeds either threshold, an arming condition is indicated.

Once an arming condition is indicated for the X-Axis, the ARM_X output is asserted when $\overline{CS}$ is asserted and the MISO data includes an acceleration response for that axis.

Once an arming condition is indicated for the Y-Axis, the ARM_Y output is asserted when $\overline{CS}$ is asserted and the MISO data includes an acceleration response for that axis.

The pulse stretch function is not applied in Unfiltered mode.

Figure 29 contains a block diagram of the Arming Function operation in Unfiltered Mode. Figure 30 shows the Arming output operation under the different SPI request conditions.

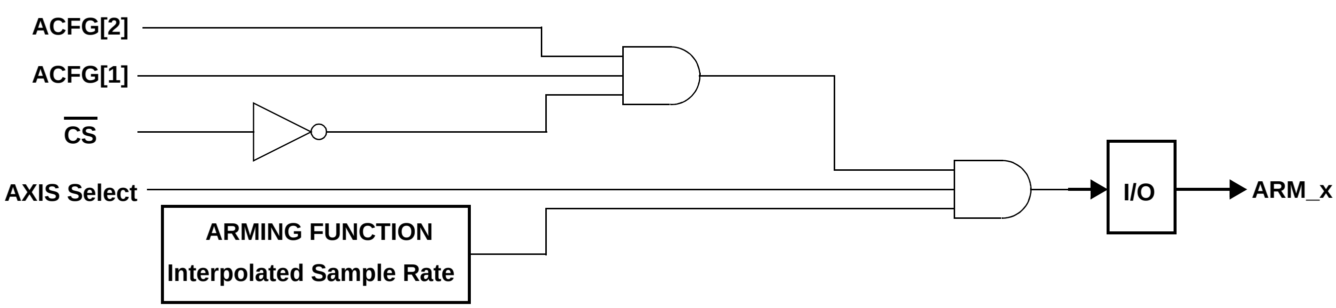


Figure 29. Arming Function Block Diagram - Unfiltered Mode

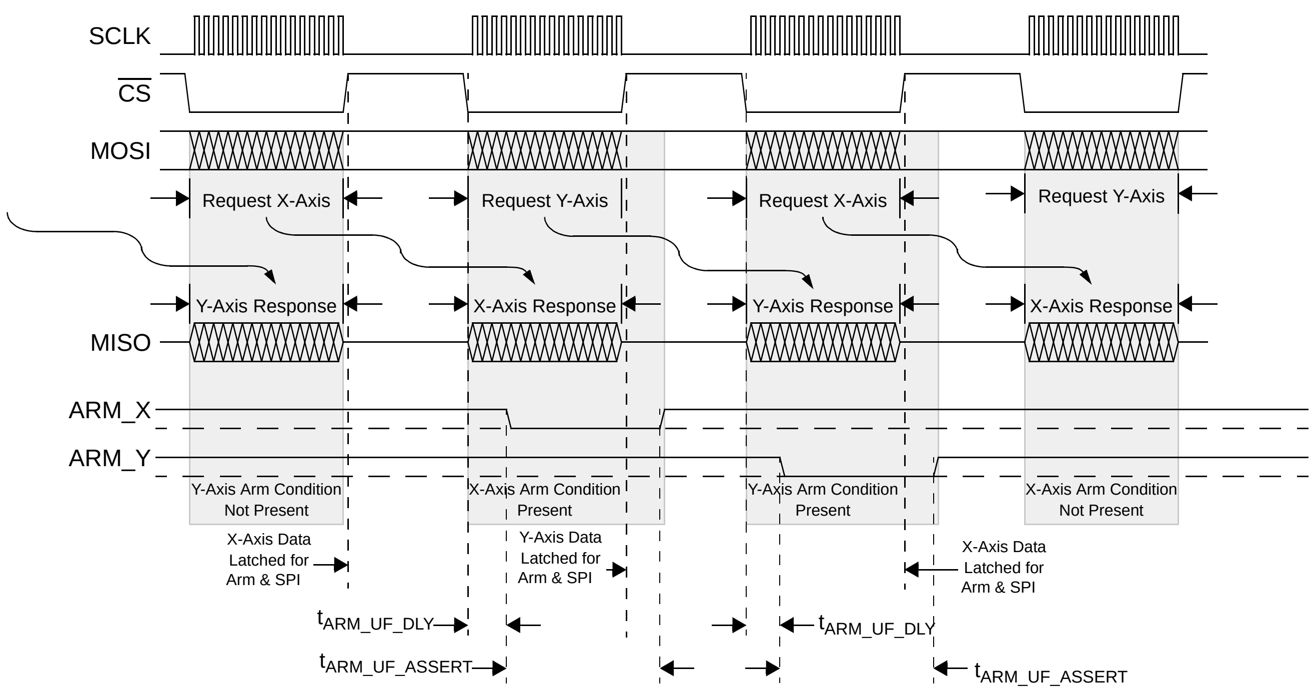


Figure 30. X and Y Axis Arming Conditions, Unfiltered Mode

3.8.10.4 Arming Pulse Stretch Function

A pulse stretch function can be applied to the arming outputs in moving average mode, or count mode.

If the pulse stretch function is not used (APS_X[1:0] = ‘00’ or APS_Y[1:0] = ‘00’), the arming output is asserted if and only if an arming condition exists for the associated axis after the most recent evaluated sample. The arming output is de-asserted if and only if an arming condition does not exist for the associated axis after the most recent evaluated sample.

If the pulse stretch function is used, (APS_X[1:0] not equal ‘00’ or APS_Y[1:0] not equal ‘00’), the arming output is controlled only by the value of the pulse stretch timer value. If the pulse stretch timer value is non-zero, the arming output is asserted. If the pulse stretch timer is zero, the arming output is de-asserted. The pulse stretch counter continuously decrements until it reaches zero. The pulse stretch counter is reset to the programmed pulse stretch value if and only if an arming condition exists for the associated axis after the most recent evaluated sample. Reference Figure 28.

The desired pulse stretch time is individually programmable for each axis via the APS_X[1:0] and APS_Y[1:0] bits in the ARMCFG register.

Exception conditions listed in Section 4.5 do not impact prior arming function responses. If an exception occurs after an arming activation, the corresponding pulse stretch for the existing arming condition will continue. However, new acceleration reads will not reset the pulse stretch counter regardless of the acceleration value.

3.8.10.5 Arming Pin Output Structure

The arming output pin structure can be set to active high, or active low with the A_CFG bits in the DEVCFG register as described in Section 3.1.6.6. The active high and active low pin output structures are shown in Figure 31.

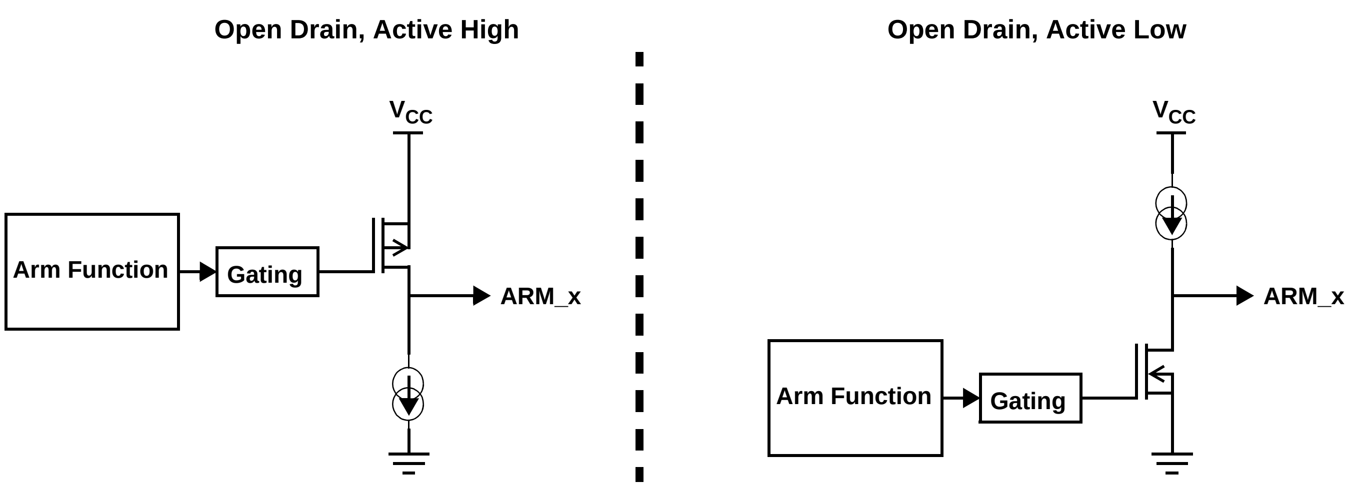


Figure 31. Arming Function - Pin Output Structure

3.8.11 PCM Output Function

The device provides the option for a PCM output function. The PCM output is enabled by setting the A_CFG bits in the DEVCFG register to the appropriate state as described in Section 3.1.6.6. Selecting the PCM output enables the following functions:

- The PCM_X and PCM_Y pins are programmed as a digital outputs. Reference Section 2.3 for the pin electrical parameters.
- The acceleration value output from the offset cancellation block is saturated to 9-bits and converted to an unsigned value. Note, the 9-bit unsigned acceleration value uses the full range of values (0 - 511).
- The 9-bit acceleration value is input into a summer clocked at 8MHz.
- The carry from the summer circuit is output to the PCM pin.

A block diagram of the PCM output is shown in Figure 32.

Exception conditions affect the PCM output as listed in Section 4.5.

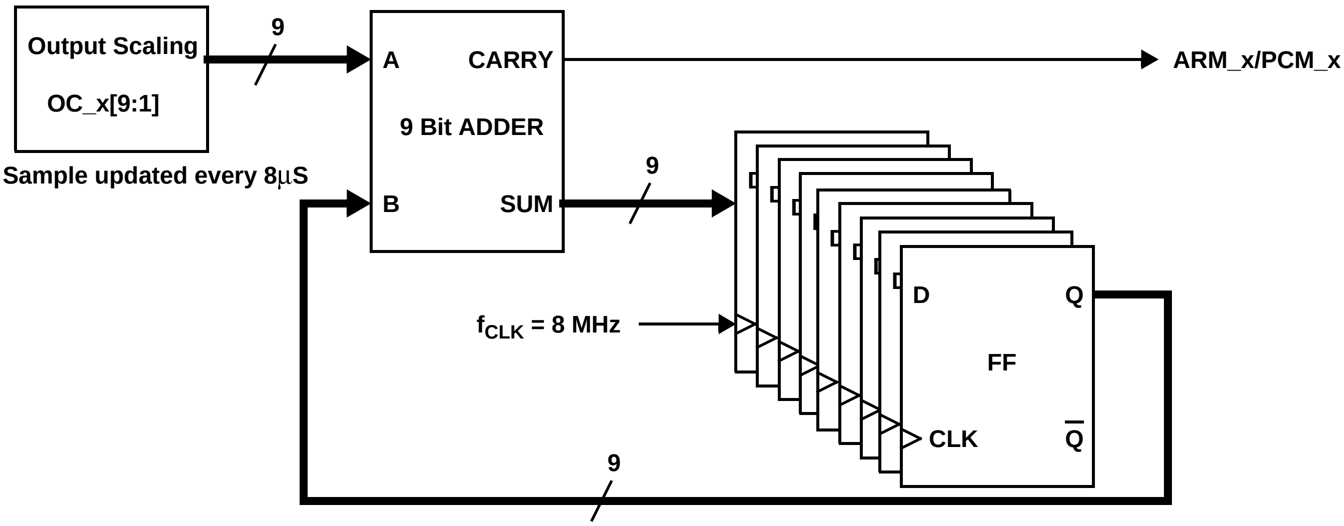


Figure 32. PCM Output Function Block Diagram

3.9 Serial Peripheral Interface

The device includes a Serial Peripheral Interface (SPI) to provide access to the configuration registers and digital data. Reference Section 4 for details regarding the SPI protocol and available commands.

To maximize independence between the X and Y channels, the device includes two interface blocks, one for each axis. The X-axis interface block responds only to X-axis acceleration requests, or even addressed register commands. The Y-axis interface block responds only to Y-axis acceleration requests, or odd addressed register commands. To the SPI master, the device operates as a single device. The internal independent blocks are transparent.

Each SPI block has an independent shift register. Once a message is received (rising edge of $\overline{CS}$), the contents of the two shift registers are compared. If the contents do not match, the Y-Axis SPI block will not respond, and the X-Axis SPI block will respond with a SPI Error as shown in Table 30. If the contents match, each SPI block decodes the message, and the appropriate block enables DO for a response during the next SPI message.

Figure 33 shows an internal diagram of the SPI.

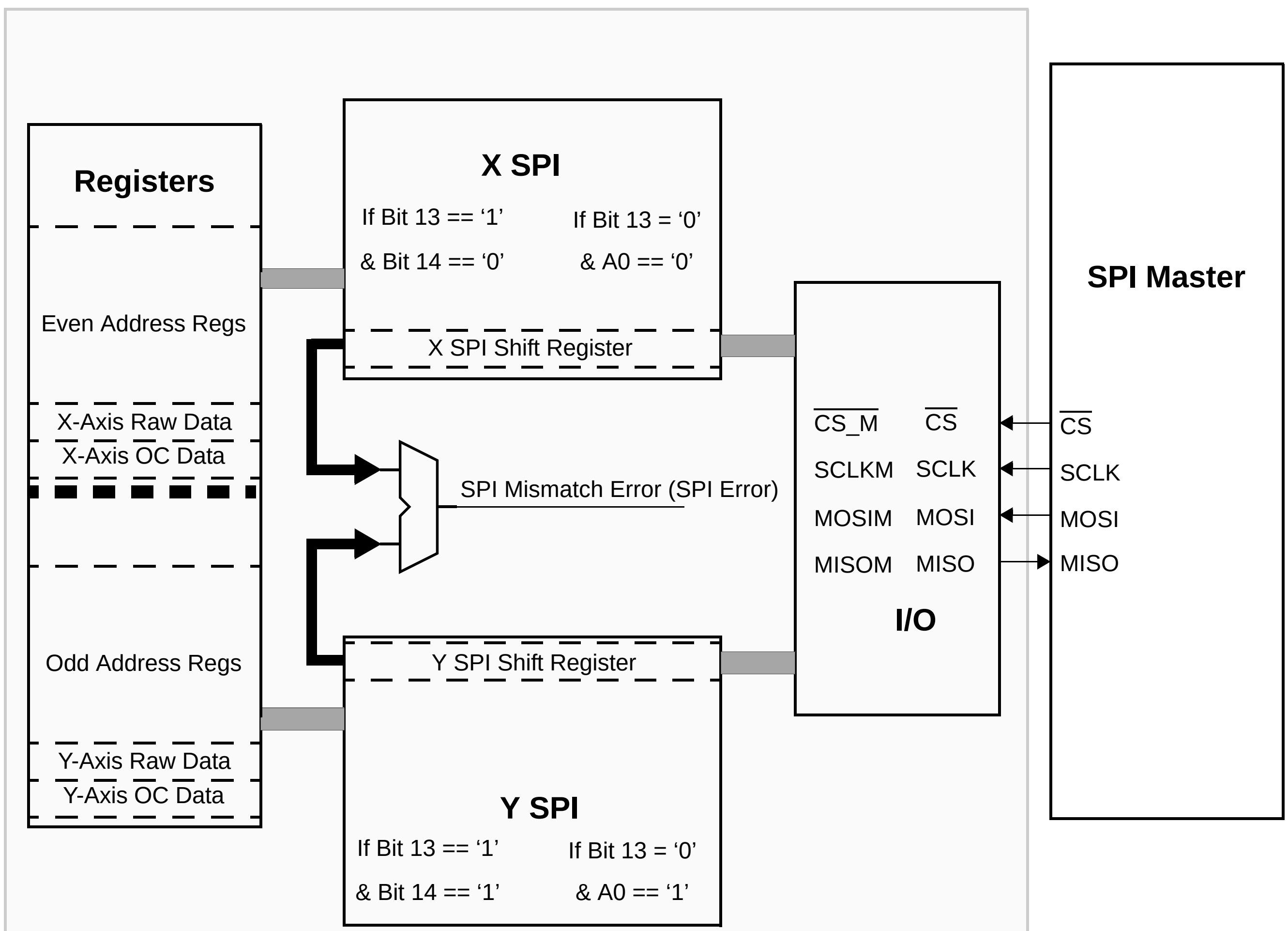
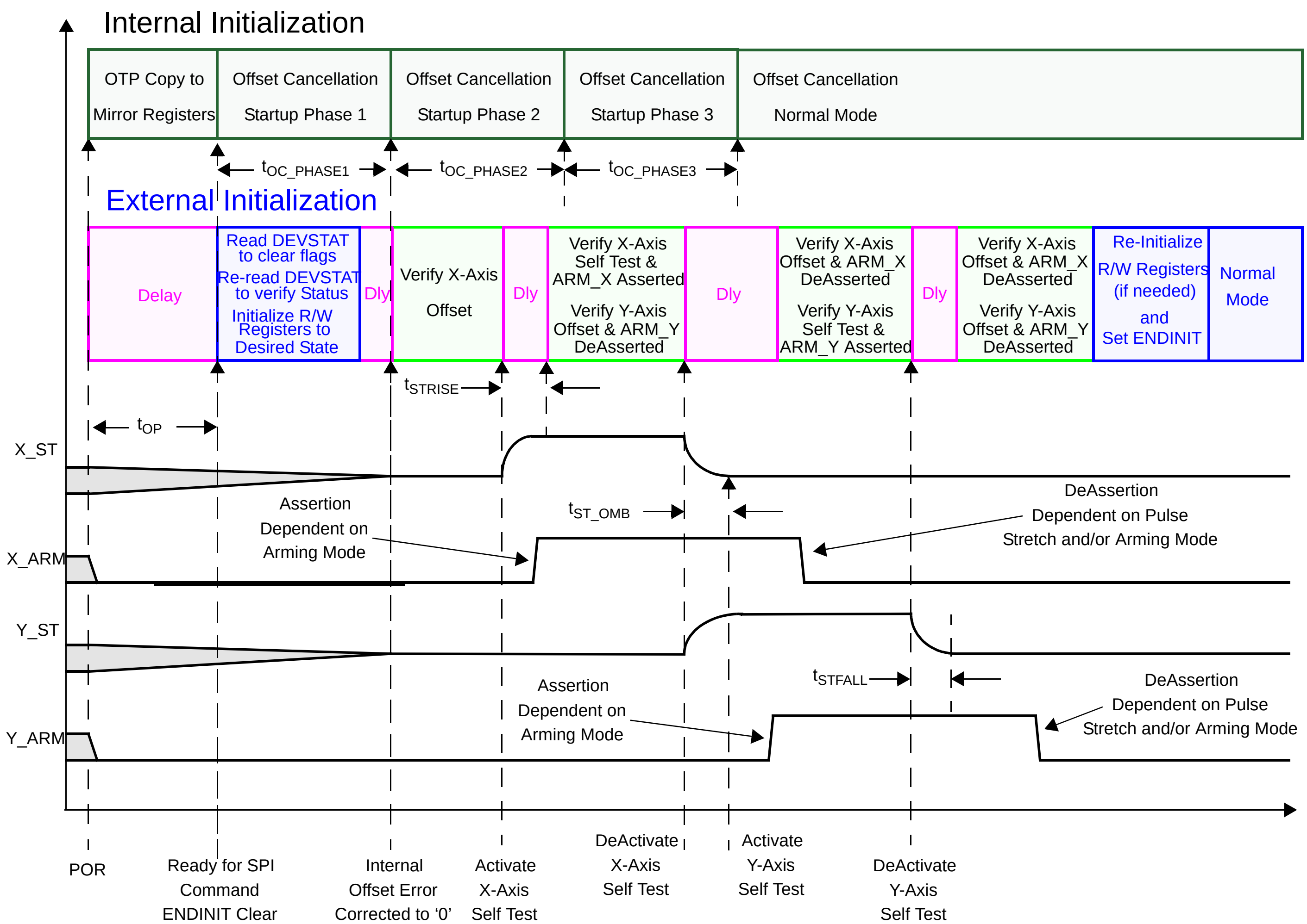


Figure 33. SPI Diagram

3.10 Device Initialization

Following power-up, under-voltage reset, or a SPI reset command sequence, the device proceeds through an internal initialization process as shown below. Figure 34 also shows the device performance for an example external system level initialization procedure.



Notes:1) X-Axis and Y-Axis Self Test can be enabled and evaluated simultaneously to reduce test time.
For failure mode coverage of the arming pins and of potential common axis failures, NXP recommends independent self test activation.
2) t_{STRISE} and t_{STFALL} are dependent on the selected LPF group delay.

Figure 34. Initialization Process

3.11 Overload Response

3.11.1 Overload Performance

The device is designed to operate within a specified range. Acceleration beyond that range (overload) impacts the output of the sensor. Acceleration beyond the range of the device can generate a DC shift at the output of the device that is dependent upon the overload frequency and amplitude. The *g*-cell is overdamped, providing the optimal design for overload performance. However, the performance of the device during an overload condition is affected by many other parameters, including:

- *g*-cell damping
- Non-linearity
- Clipping limits
- Symmetry

Figure 35 shows the *g*-cell, ADC and output clipping of the device over frequency. The relevant parameters are specified in Section 2.1, and Section 2.7.

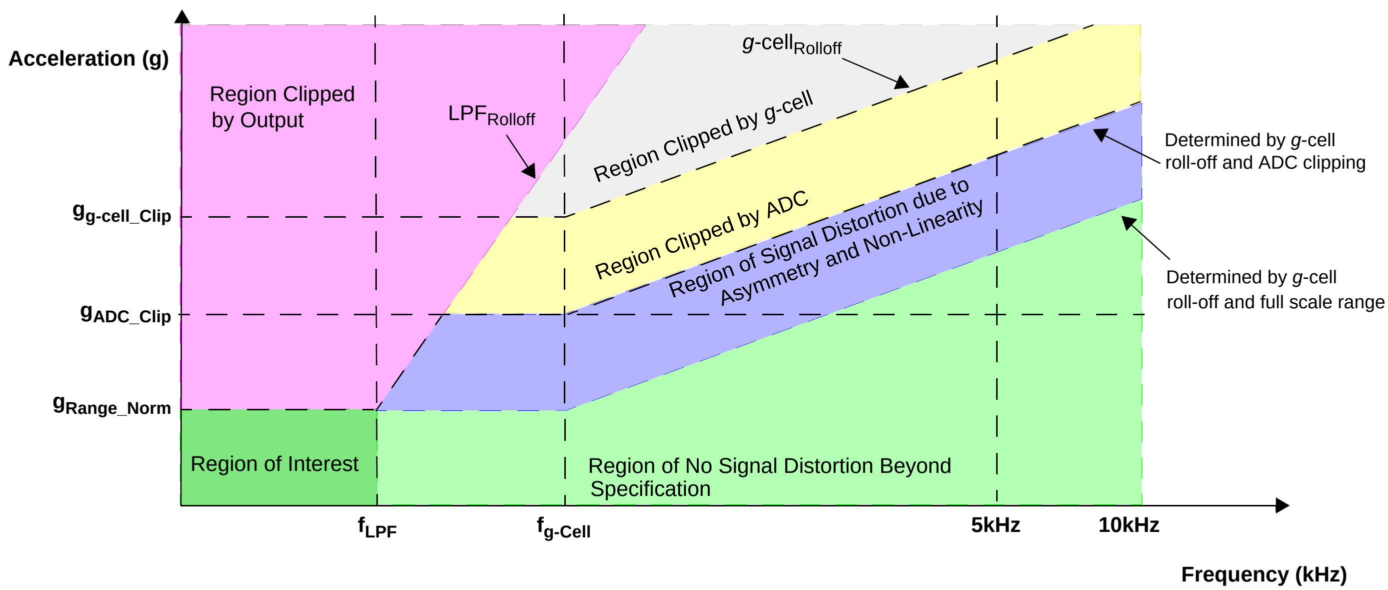


Figure 35. Output Clipping Vs. Frequency

3.11.2 Sigma Delta Over Range Response

Over range conditions exist when the signal level is beyond the full-scale range of the device but within the computational limits of the DSP. The ΣΔ converter can saturate at levels above those specified in Section 2.1 (G_{ADC_CLIP}). The DSP operates predictably under all cases of over range, although the signal may include residual high frequency components for some time after returning to the normal range of operation due to non-linear effects of the sensor.

4 SPI Communications

Communication with the device is completed through synchronous serial transfers via SPI. The device is a slave device configured for CPOL = 0, CPHA = 0, MSB first. SPI transfers are completed through a sequence of two phases. During the first phase, the type of transfer and associated control information is transmitted from the SPI master to the device. Data from the device is transmitted during the second phase. Any activity on MOSI or SCLK is ignored when $\overline{CS}$ is negated. Consequently, intermediate transfers involving other SPI devices may occur between phase one and phase two. Reference Figure 36.

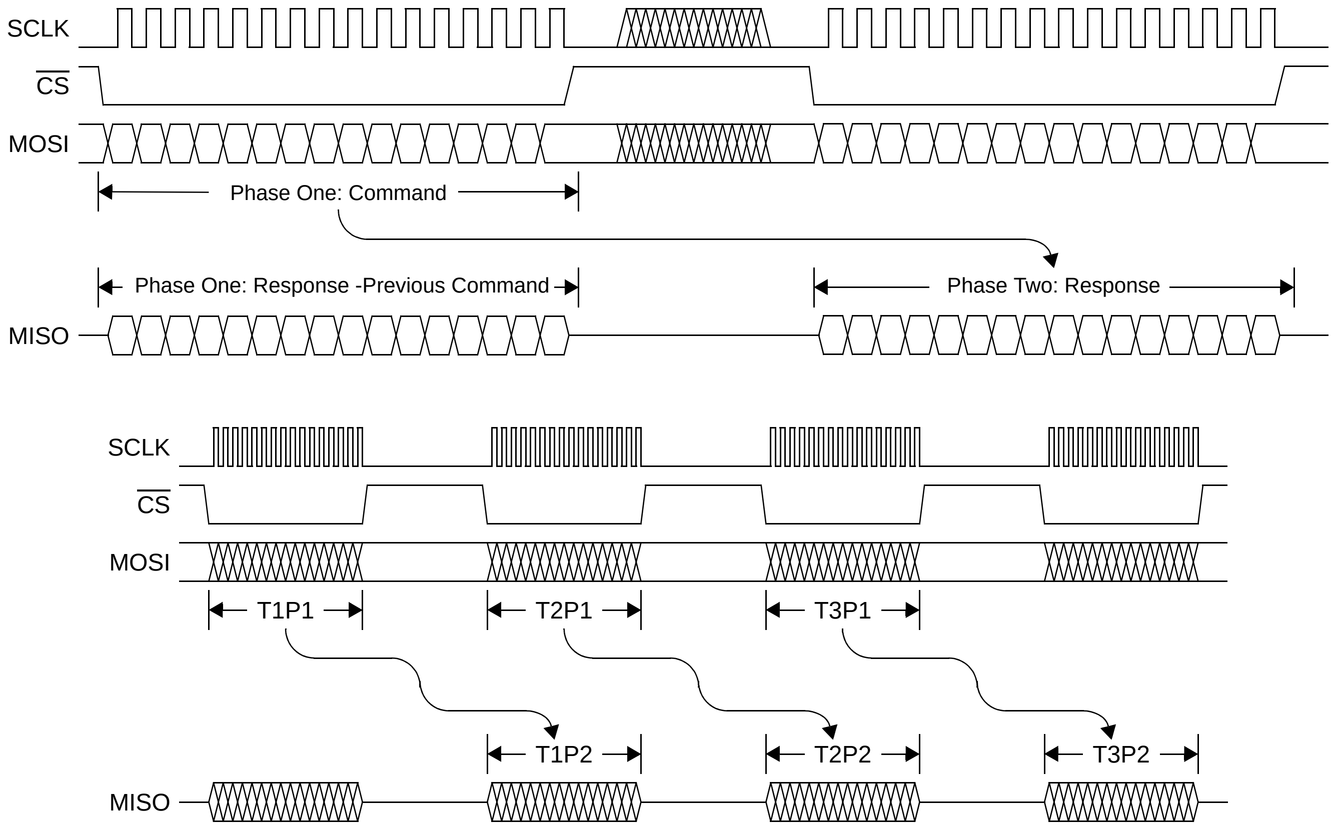


Figure 36. SPI Transfer Detail

4.1 SPI Command Format

Commands are transferred from the SPI master to the device. Valid commands fall into two categories: register operations, and acceleration data requests.

Table 29. SPI Command Message Summary

15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)	Command Type	Reference
0	AX	A	$\overline{OC}$	0	0	0	0	0	0	0	0	1	$\overline{SD}$	ARM	P		

AX = Axis Selection	
0	X-Axis Acceleration Data
1	Y-Axis Acceleration Data

A = Acceleration Data Request	
0	Register Operation
1	Acceleration Data Request

$\overline{OC}$ = Offset Cancelled Data Confirmation	
0	Offset Cancelled Data Enabled
1	Raw Acceleration Data Enabled

$\overline{SD}$ = Signed Data Confirmation	
Signed Data Enabled	0
Unsigned Data Enabled	1

ARM = ARM Function Status Confirmation	
Disabled / PCM Output Enabled	0
Arming Function Enabled	1

P = Odd Parity

0	AX	A	$\overline{OC}$	0	0	0	0	0	0	0	0	0	$\overline{SD}$	ARM	P	Accel Data
0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	X-Axis OC, Signed, Disabled/PCM
0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	X-Axis OC, Signed, ARM Enabled
0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	X-Axis OC, Unsigned, Disabled/PCM
0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	X-Axis OC, Unsigned, ARM Enabled
0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	X-Axis Raw, Signed, Disabled/PCM
0	0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	X-Axis Raw, Signed, ARM Enabled
0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	1	X-Axis Raw, Unsigned, Disabled/PCM
0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	X-Axis Raw, Unsigned, ARM Enabled
0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	Y-Axis OC, Signed, Disabled/PCM
0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	1	Y-Axis OC, Signed, ARM Enabled
0	1	1	0	0	0	0	0	0	0	0	0	1	1	0	1	Y-Axis OC, Unsigned, Disabled/PCM
0	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	Y-Axis OC, Unsigned, ARM Enabled
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	1	Y-Axis Raw, Signed, Disabled/PCM
0	1	1	1	0	0	0	0	0	0	0	0	1	0	1	0	Y-Axis Raw, Signed, ARM Enabled
0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	Y-Axis Raw, Unsigned, Disabled/PCM
0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	Y-Axis Raw, Unsigned, ARM Enabled

P	AX	A	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command Type	Reference
P	0	0	A4	A3	A2	A1	A0	0	0	0	0	0	0	0	0	Register Read	Section 4.4
			Register Address														
P	1	0	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Register Write	Section 4.4
			Register Address					Data to be Written to Register									

P = Odd Parity

4.2 SPI Response Format

Table 30. SPI Response Message Summary

			MSB															LSB	
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CMD	A	AX	Response to Valid Acceleration Request																Reference
			D15	D14	AX	P	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
			D1	D0	Acceleration				D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	

AX = Axis Requested	
0	X-Axis Acceleration Response
1	Y-Axis Acceleration Response

P = Odd Parity

S[1:0] = Device Status		
0	0	In Initialization (ENDINIT = '0')
0	1	Normal Request
1	0	ST Active
1	1	Internal Error Present / SPI Error

CMD	A	AX	D1	D0	AX	P	S1	S0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	Reference
Valid Accel Request	1	0	Accel Data		0	P	0	1	X- Axis Acceleration Data										Section 4.3
	1	0	Accel Data		0	P	1	0	X- Axis Self Test Active Acceleration Data										
	1	0	Accel Data		0	P	0	0	X- Axis Acceleration Data, Initialization in Process (ENDINIT='0')										
	1	1	Accel Data		1	P	0	1	Y-Axis Acceleration Data										
	1	1	Accel Data		1	P	1	0	Y-Axis Self Test Active Acceleration Data										
	1	1	Accel Data		1	P	0	0	Y- Axis Acceleration Data, Initialization in Process (ENDINIT='0')										

			MSB															LSB	
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CMD	A	AX	Response to Valid Register Access																Reference
			D15	D14	AX	P	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Register Write	0	1	0	0	1	P	1	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Section 4.4.1
											New Contents of Register								
Register Read	0	0	0	1	0	P	1	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Section 4.4.2
											Contents of Register								

			MSB															LSB	
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CMD	A	AX	Error Responses																Reference
			D15	D14	AX	P	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Invalid Accel Request	x	x	0	0	AX	P	1	1	0	0	0	0	0	0	0	0	0	0	Section 4.3
Internal Error Present	x	x																	Section 4.5.5
MISO Error	x	x	0	0	0	P	1	1	0	0	0	0	0	0	0	0	0	0	Section 4.5.2
SPI Error	x	x																	Section 4.5.1
Invalid Register Request	0	x	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	Section 4.4
Self Test Error	0	x	0	0	AX	P	1	1	0	0	0	0	0	0	0	0	0	0	Section 4.5.5

4.3 Acceleration Data Transfers

Twelve bit Acceleration data requests are initiated when the Acceleration bit of the SPI command message (A) is set to a logic '1', and bit D[3] of the SPI command message is set to a logic '1'. The Axis Selection bit (AX) selects the type of acceleration data requested, as shown in Table 31.

Table 31. Acceleration Data Request

Axis Selection Bit (AX)	Data Type
0	X-Axis Acceleration Data
1	Y-Axis Acceleration Data

To verify that the device is configured as expected, each acceleration data request includes the configuration information which impacts the output data. The requested configuration is compared against the data programmed in the writable register block. Details are shown in Table 32.

Table 32. Acceleration Data Request Configuration Information

Programmable Option	Command Message Bit	Writable Register Information
Raw or Offset Cancelled Data	$\overline{OC}$	DEVCFG[7] ($\overline{OC}$)
Signed or Unsigned Data	$\overline{SD}$	DEVCFG[4] ($\overline{SD}$)
Arming Function or PCM Output	ARM	DEVCFG[2] || DEVCFG[1] (A_CFG[2] || A_CFG[1])

If the data listed in Table 32 does not does not match, an Acceleration Data Request Mismatch failure is detected and no acceleration data is transmitted. Reference Section 4.5.3.1.

Acceleration data request commands include a parity bit (P). Odd parity is employed. The number of logic '1' bits in the acceleration data request command must be an odd number.

Acceleration data is transmitted on the next SPI message if and only if all of the following conditions are met:

- The DEVINIT bit in the DEVSTAT register is not set
- The DEVRES bit in the DEVSTAT register is not set
- The IDE bit in the DEVSTAT register is not set (Reference Section 4.5.5)
- No SPI Error is detected (Reference Section 4.5.1)
- No MISO Error is detected (Reference Section 4.5.2)
- No Acceleration Data Request Mismatch failure is detected (Reference Section 4.5.3.1)
- No Self Test Error is present (reference Section 4.5.5.2)
- No Offset Monitor Error is present for the requested channel (reference Section 4.5.6)

If the above conditions are met, the device responds with a "valid acceleration data request" response as shown in Table 30. Otherwise, the device responds as specified in Section 4.5.

4.4 Register Access Operations

Two types of register access operations are supported; register write, and register read. Register access operations are initiated when the acceleration bit (A) of the command message is set to a logic ‘0’. The operation to be performed is indicated by the Access Selection bit (AX) of the command message.

Access Selection Bit (AX)	Operation
0	Register Read
1	Register Write

Register Access operations include a parity bit (P). Odd parity is employed. The number of logic ‘1’ bits in the Register Access operation must be an odd number.

4.4.1 Register Write Request

During a register write request, bits 12 through 8 contain a five-bit address, and bits 7 through 0 contain the data value to be written. Writable registers are defined in Table 3.

The response to a register write operation is shown in Table 30. The response is transmitted on the next SPI message if and only if all of the following conditions are met:

- No SPI Error is detected (Reference Section 4.5.1)
- No MISO Error is detected (Reference Section 4.5.2)
- The ENDINIT bit is cleared (Reference Section 3.1.6.3)
  - This applies to all registers with the exception of the DEVCTL register (Only Bits 6 and 7 can be modified)
- No Invalid Register Request is detected (Reference Section 4.5.3.2)

If the above conditions are met, the device responds to the register write request as shown in Table 30. Otherwise, the device Responds as specified in Section 4.5.

Register write operations do not occur internally until the transfer during which they are requested has been completed. In the event that a SPI Error is detected during a register write transfer, the write operation is not completed.

4.4.2 Register Read Request

During a register read request, bits 12 through 8 contain the five-bit address for the register to be read. Bits 7 through 0 must be logic ‘0’. Readable registers are defined in Table 3.

The response to a register read operation is shown in Table 30. The response is transmitted on the next SPI message if and only if all of the following conditions are met:

- No SPI Error is detected (Reference Section 4.5.1)
- No MISO Error is detected (Reference Section 4.5.2)
- No Invalid Register Request is detected (Reference Section 4.5.3.2)

If the above conditions are met, the device responds to the register read request as shown in Table 30. Otherwise, the device responds as specified in Section 4.5.

4.5 Exception Handling

The following sections describe the conditions and the device response for each detectable exception. In the event that multiple exceptions exist, the exception response is determined by the priority listed in Table 33.

Table 33. SPI Error Response Priority

Error Priority	Exception	Effect on Data		
		SPI Data	Arming Output	PCM Output
1	SPI Error	Error Response	No Update	No Effect
2	SPI MISO Error	Error Response	No Update	No Effect
3	Invalid Request	Error Response	No Update	No Effect
4	DEVINIT Bit Set	Error Response	No Update	Disabled
5	DEVRES Error	Error Response	No Update	Disabled
6	CRC Error	Error Response	No Update	No Effect
7	Self Test Error	Error Response	No Update	No Effect
8	Offset Monitor Error	Error Response	No Update	No Effect

4.5.1 SPI Error

The following SPI conditions result in a SPI error:

- SCLK is high when $\overline{CS}$ is asserted
- The number of SCLK rising edges detected while $\overline{CS}$ is asserted is not equal to 16
- SCLK is high when $\overline{CS}$ is negated
- Command message parity error (MOSI)
- Bit 15 of Acceleration Data Request is not equal to ‘0’
- Bits 4 through 11 of an Acceleration Request are not equal to ‘0’
- Bits 3 of an Acceleration Request is not equal to ‘1’
- Bits 0 through 7 of a Register Read Request are not equal to ‘0’

The device responds to a SPI error with a “SPI Error” response as shown in Table 30. This applies to both acceleration data request SPI errors, and Register Access SPI errors.

The arming function will not be updated if a SPI Error is detected. The PCM output is not affected by a SPI Error.

4.5.2 SPI Data Output Verification Error

The device includes a function to verify the integrity of the data output to the MISO pin. The function reads the data transmitted on the MISO pin and compares it against the data intended to be transmitted. If any one bit doesn't match, a SPI MISO Mismatch Fault is detected and the MISOERR flag in the DEVSTAT register is set.

If a valid SPI acceleration request message is received during the SPI transfer with the MISO mismatch failure, the SPI acceleration request message is ignored and the device responds with a “MISO Error” response during the subsequent SPI message (reference Table 30). The Arming function is not updated if a MISO mismatch failure occurs. The PCM function is not affected by the MISO mismatch failure.

If a valid SPI register write request message is received during the SPI transfer with the MISO mismatch failure, the register write is completed as requested, but the device responds with a “MISO Error” response as shown in Table 30, during the subsequent SPI message.

If a valid SPI register read request message is received during the SPI transfer with the MISO mismatch failure, the register read is ignored and the device responds with a “MISO Error” response as shown in Table 30, during the subsequent SPI message. If the register read request is for the DEVSTAT register, the DEVSTAT register will not be cleared.

In all cases, the MISOERR flag in the DEVSTAT register will remain set until a successful SPI Register Read Request of the DEVSTAT register is completed.

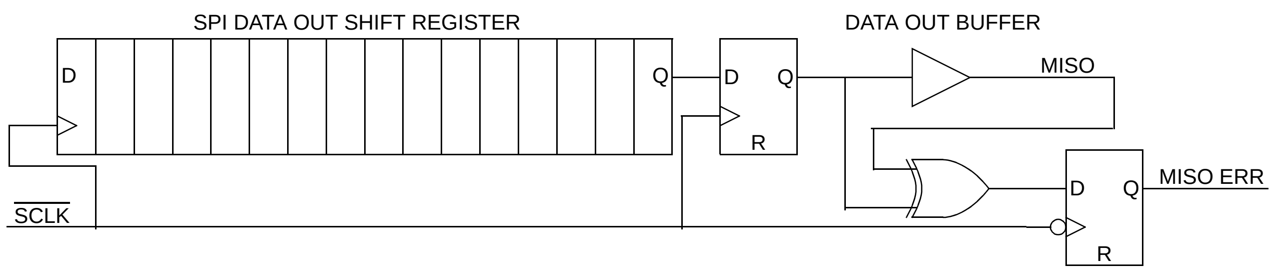


Figure 37. SPI Data Output Verification

4.5.3 Invalid Requests

4.5.3.1 Acceleration Data Request Mismatch Failure

The device detects an “Acceleration Data Request Mismatch” error if the SPI “Acceleration Data Request” Command data listed in Table 32 does not match the internal register settings. The device responds to an “Acceleration Data Request Mismatch” error with an “Invalid Accel Request” response as specified in Table 30 on the subsequent SPI message only. No internal fault is recorded. The arming function will not be updated if an “Acceleration Data Request Mismatch” Error is detected. The PCM output is not affected by the “Acceleration Data Request Mismatch” error.

Register operations will be executed as specified in Section 4.4.

4.5.3.2 Invalid Register Request

The following conditions result in an “Invalid Register Request” error:

- An attempt is made to write to an un-writable register (Writable registers are defined in Section 3.1, Table 3). Attempts to write to registers \$09, \$18, \$19, \$1A and \$1B will result in an error.
- An attempt is made to write to a register while the ENDINIT bit in the DEVCFG register is set
  - This applies to all registers with the exception of the DEVCTL register (Only Bits 6 and 7 can be modified)
- An attempt is made to read an un-readable register (Readable registers are defined in Section 3.1, Table 3). Attempts to read registers \$09, \$18, \$19, \$1A and \$1B will result in an error.

The device responds to an Invalid Register Request” error with an “Invalid Register Request” response as shown in Table 30.

4.5.4 Device Reset Indications

If the DEVINIT, or DEVRES bit is set in the DEVSTAT register as described in Section 3.1.11, the device will respond to acceleration data requests with an “Internal Error Present” response until the bits are cleared in the DEVSTAT register. The DEVINIT bit is cleared automatically when device initialization is complete (Reference t_{OP} in Section 2.7). The DEVRES bit is cleared on a read of the DEVSTAT register. The arming function will not be updated on Acceleration Data Request commands if the DEVINIT or DEVRES bit is set in the DEVSTAT register. The PCM output is disabled if the DEVINIT or DEVRES bit is set.

4.5.5 Internal Error

The following errors will result in an internal error, and set the IDE bit in the DEVSTAT register:

- OTP CRC Failure
- Writable Register CRC Failure
- Self Test Error
- Invalid internal logic states

4.5.5.1 CRC Error

If the IDE bit is set in the DEVSTAT register due to one or more of the following errors, the device will respond to acceleration data requests with an “Internal Error Present” response until the IDE bit is cleared in the DEVSTAT register.

- An OTP Shadow Register CRC failure as described in Section 3.2
- A Writable Register CRC failure as described in Section 3.2
- A clock monitor CRC failure as described in Section 3.4.2

The arming function will not be updated on Acceleration Data Request commands if a CRC Error is detected. The PCM output is not affected by the CRC error.

If the CRC error is in the writable register array, and the ENDINIT bit in the DEVCFG register has been set, the error can only be cleared by a device reset. The IDE bit will not be cleared on a read of the DEVSTAT register.

If the CRC error is in the OTP shadow register array, the error cannot be cleared.

Register operations will be executed as specified in Section 4.4.

4.5.5.2 Self Test Error

If the IDE bit is set in the DEVSTAT register due to a Self Test activation failure, the device will respond to acceleration data requests with a “Self Test Error” response until the IDE bit is cleared in the DEVSTAT register. The arming function will not be updated on Acceleration Data Request commands if a Self Test Error is detected. The PCM output is not affected by the Self Test Error. The IDE bit in the DEVSTAT register will remain set until a read of the DEVSTAT register occurs, even if the internal failure is removed. If the internal error is still present when the DEVSTAT register is read, the IDE bit will remain set.

Register operations will be executed as specified in Section 4.4.

4.5.6 Offset Monitor Error

If an offset monitor error is present as described in Section 3.8.5, the OFFSET_X or OFFSET_Y bit in the DEVSTAT register will be set. The device will respond to an acceleration request for the corresponding axis with an “Internal Error Present” response until the OFFSET_X or OFFSET_Y bit is cleared in the DEVSTAT register. The arming function will not be updated. Once the error condition is removed, the OFFSET_X or OFFSET_Y bit in the DEVSTAT register will remain set until a read of the DEVSTAT register occurs.

The PCM output is not affected by the offset monitor over range condition.

Register operations will be executed as specified in Section 4.4.

4.6 Initialization SPI Response

The first data transmitted by the device following reset is the SPI Error response shown in Table 30. This ensures that an unexpected reset will always be detectable. The device will respond to all acceleration data requests with the “Invalid Acceleration Data Request” response until the DEVRES bit in the DEVSTAT register is cleared via a read of the DEVSTAT register. The arming function will not be updated on Acceleration Data Request commands until the DEVRES bit in the DEVSTAT register is cleared.

4.7 Acceleration Data Representation

Acceleration values are determined from the 12-bit digital output (DV) using the following equations:

$$Acceleration = Sensitivity_{LSB} \times DV \qquad \text{For Signed Data}$$

$$Acceleration = Sensitivity_{LSB} \times (DV - 2048) \qquad \text{For Unsigned Data}$$

The linear range of digital values for signed data is -1920 to +1920, and for unsigned data is 128 to 3968. Resulting ranges and some nominal acceleration values are shown in the following table.

Table 34. Nominal Acceleration Data Values

Unsigned Digital Value	Signed Digital Value	Nominal Acceleration					
		105g		105g		120g	
3969 - 4095	1921 - 2047	Unused		Unused		Unused	
3968	1920	80.000	g	105.49	g	120.00	g
3967	1919	79.958	g	105.44	g	119.94	g
• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
2050	2	0.083333	g	0.1099	g	0.1250	g
2049	1	0.041667	g	0.0545	g	0.0625	g
2048	0	0	g	0	g	0	g
2047	-1	-0.041667	g	-0.0545	g	-0.0625	g
2046	-2	-0.083333	g	-0.1099	g	-0.1250	g
• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
129	-1919	-79.958	g	-105.44	g	-119.94	g
128	-1920	-80.000	g	-105.49	g	-120.00	g
1 - 127	-1921 - 2048	Unused		Unused		Unused	
0	0	Fault		Fault		Fault	

Figure 38 shows the how the possible output data codes are determined from the input data and the error sources. The relevant parameters are specified in Section 2.4.

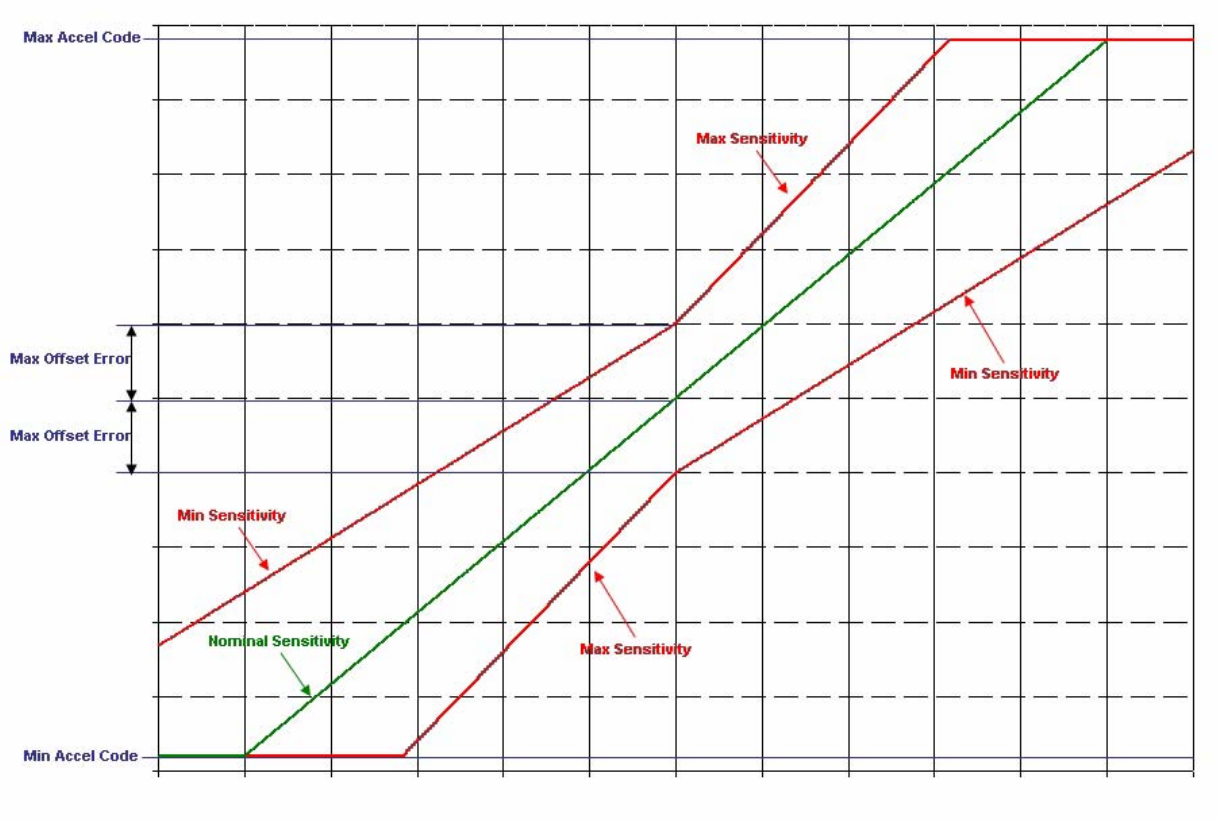


Figure 38. Acceleration Data Output Vs. Acceleration Input

5 Package

5.1 Case Outline Drawing

Reference NXP case outline document 98ASA00690D.

http://cache.nxp.com/assets/documents/data/en/package-information/98ASA00690D.pdf

5.2 Recommended Footprint

Reference NXP application note AN1902, latest revision:

http://www.nxp.com/assets/documents/data/en/application-notes/AN1902.pdf

6 Revision History

Table 35. Revision History

Revision number	Revision date	Description of changes
9.0	01/2017	• Deleted part numbers MMA6519KGTW, MMA6525KGTW, and MMA6527KGTW. • Updated part marking diagram to reflect deletions.
8.0	11/2016	—
7.0	10/2016	—
6.0	04/2016	—
5.0	12/2015	—
3	03/2012	—
4	10/2014	—

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