

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low $r_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Drain current (DC)	$-I_D$	max.	275 mA
Drain-source ON-resistance $-I_D = 200 \text{ mA}; -V_{GS} = 10 \text{ V}$	$r_{DS(on)}$	max.	10Ω
Gate threshold voltage	$-V_{GS(th)}$	max.	3.5 V

MECHANICAL DATA

Dimensions in mm

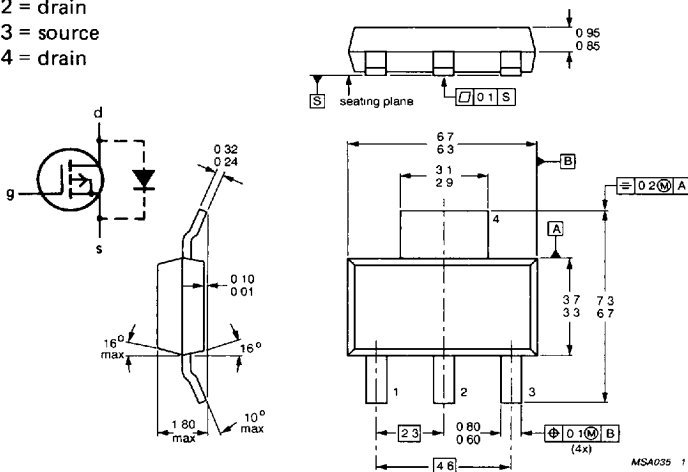
Marking code

Fig.1 SOT223.

BSP205

Pinning:

- 1 = gate
- 2 = drain
- 3 = source
- 4 = drain



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	275 mA
Drain current (peak)	$-I_{DM}$	max.	550 mA
Total power dissipation up to $T_{amb} = 25^\circ\text{C}$ (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}		-65 to $+150^\circ\text{C}$
Junction temperature	T_j	max.	150°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	83.3 K/W
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CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

Drain-source breakdown voltage $-I_D = 10\ \mu\text{A}; V_{GS} = 0$	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS} = 48\ \text{V}; V_{GS} = 0$	$-I_{DSS}$	max.	$1.0\ \mu\text{A}$
Gate-source leakage current $\pm V_{GS} = 20\ \text{V}; V_{DS} = 0$	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D = 1\ \text{mA}; V_{DS} = V_{GS}$	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D = 200\ \text{mA}; -V_{GS} = 10\ \text{V}$	$r_{DS(on)}$	typ. max.	$7.5\ \Omega$ $10\ \Omega$
Transfer admittance $-I_D = 200\ \text{mA}; -V_{DS} = 15\ \text{V}$	$ Y_{fs} $	min. typ.	60 mS 125 mS
Input capacitance at $f = 1\ \text{MHz};$ $-V_{DS} = 10\ \text{V}; V_{GS} = 0$	C_{iss}	typ. max.	30 pF 45 pF
Output capacitance at $f = 1\ \text{MHz};$ $-V_{DS} = 10\ \text{V}; V_{GS} = 0$	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at $f = 1\ \text{MHz};$ $-V_{DS} = 10\ \text{V}; V_{GS} = 0$	C_{rss}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D = 200\ \text{mA}; -V_{DD} = 50\ \text{V};$ $-V_{GS} = 0$ to $10\ \text{V}$	t_{on}	typ. max.	3 ns 6 ns
	t_{off}	typ. max.	10 ns 15 ns

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. $6\ \text{cm}^2$.

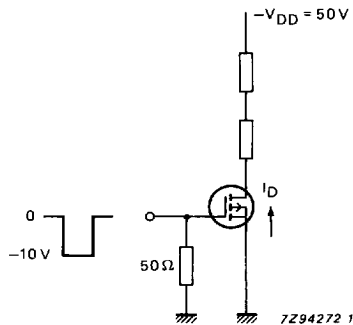


Fig.2 Switching time test circuit.

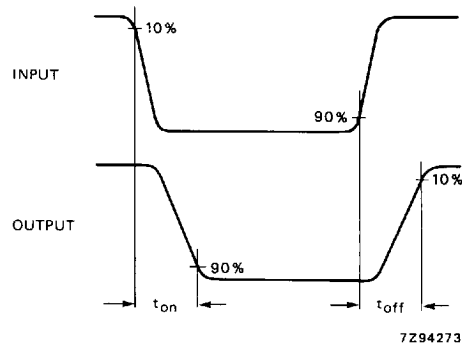


Fig.3 Input and output waveforms.

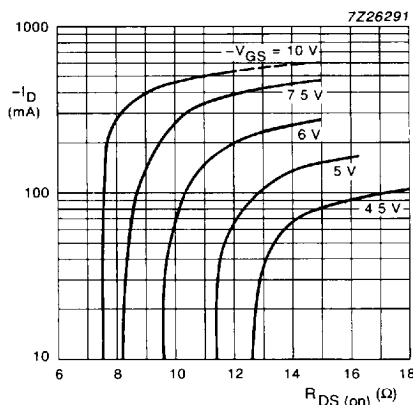


Fig.4 ON-resistance as a function of drain current; $T_j = 25^\circ\text{C}$; typical values.

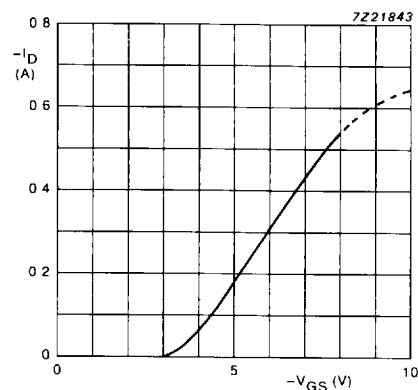


Fig.5 Transfer characteristics; $-V_{DS} = 10\text{ V}$; $T_j = 25^\circ\text{C}$; typical values.

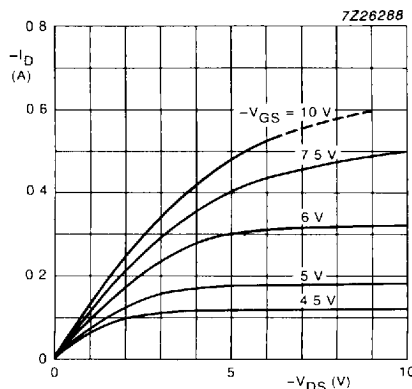


Fig.6 Output characteristics; $T_j = 25^\circ\text{C}$; typical values.

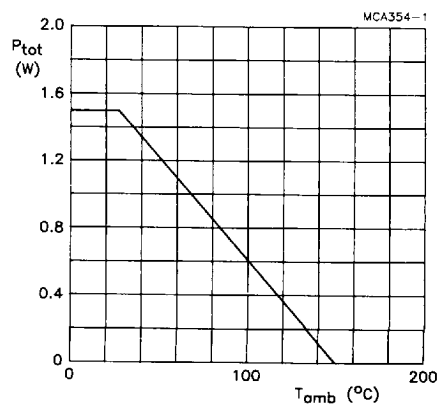


Fig.7 Power derating curve.

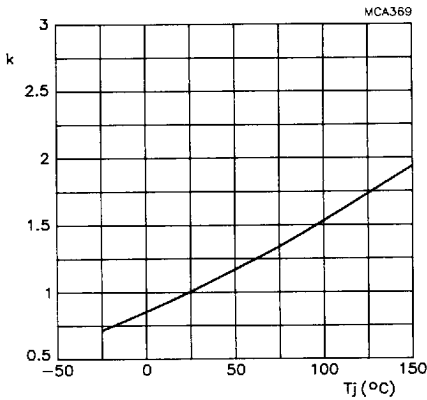


Fig. 8 $k = \frac{r_{DS(on)} \text{ at } T_j}{r_{DS(on)} \text{ at } 25^\circ\text{C}}$; at $-200 \text{ mA}/-10 \text{ V}$;

typical values.

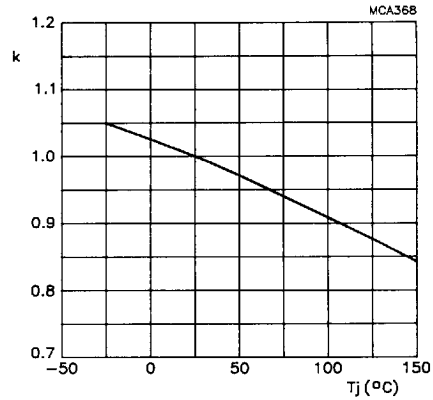


Fig. 9 $k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25^\circ\text{C}}$;

$-V_{GS(th)}$ at -1 mA ; typical values.

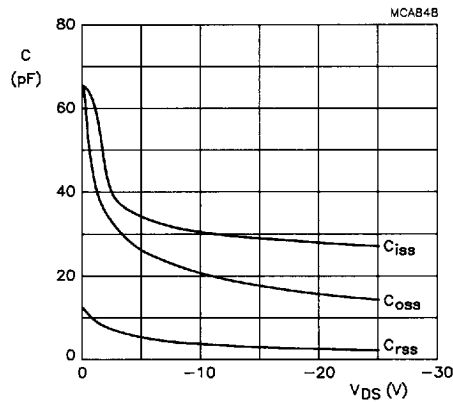


Fig. 10 $T_j = 25^\circ\text{C}$; $V_{GS} = 0$; $f = 1 \text{ MHz}$; typical values.