

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

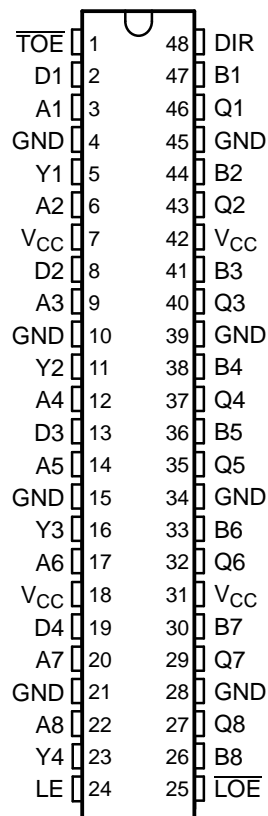
## DESCRIPTION/ORDERING INFORMATION

This device contains four independent noninverting buffers and an 8-bit noninverting bus transceiver and D-type latch, designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH16973 is particularly suitable for demultiplexing an address/data bus into a dedicated address bus and dedicated data bus. The device is used where there is asynchronous bidirectional communication between the A and B data bus, and the address signals are latched and buffered on the Q bus. The control-function implementation minimizes external timing requirements.

This device can be used as one 4-bit buffer, one 8-bit transceiver, or one 8-bit latch. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The transceiver output-enable ( $\overline{TOE}$ ) input can be used to disable the transceivers so that the A and B buses effectively are isolated.

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DL	Tube	SN74ALVCH16973DL	ALVCH16973
		Tape and reel	SN74ALVCH16973DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCH16973DGGR	ALVCH16973
	TVSOP - DGV	Tape and reel	SN74ALVCH16973DGVR	VH973

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

# SN74ALVCH16973

## 8-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH FOUR INDEPENDENT BUFFERS

SCES435B–APRIL 2003–REVISED SEPTEMBER 2004

### DESCRIPTION/ORDERING INFORMATION (CONTINUED)

When the latch-enable (LE) input is high, the Q outputs follow the data (A) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the A inputs. The latch output-enable ( $\overline{\text{LOE}}$ ) input can be used to place the nine Q outputs in either a normal logic state (high or low logic level) or the high-impedance state. In the high-impedance state, the Q outputs neither drive nor load the bus lines significantly.  $\overline{\text{LOE}}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the Q outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{\text{LOE}}$  and  $\overline{\text{TOE}}$  should be tied to  $V_{\text{CC}}$  through pullup resistors; the minimum values of the resistors are determined by the current-sinking capability of the drivers.

The four independent noninverting buffers perform the Boolean function  $Y = D$  and are independent of the state of DIR,  $\overline{\text{TOE}}$ , LE, and  $\overline{\text{LOE}}$ .

The A and B I/Os and D inputs have bus-hold circuitry. Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

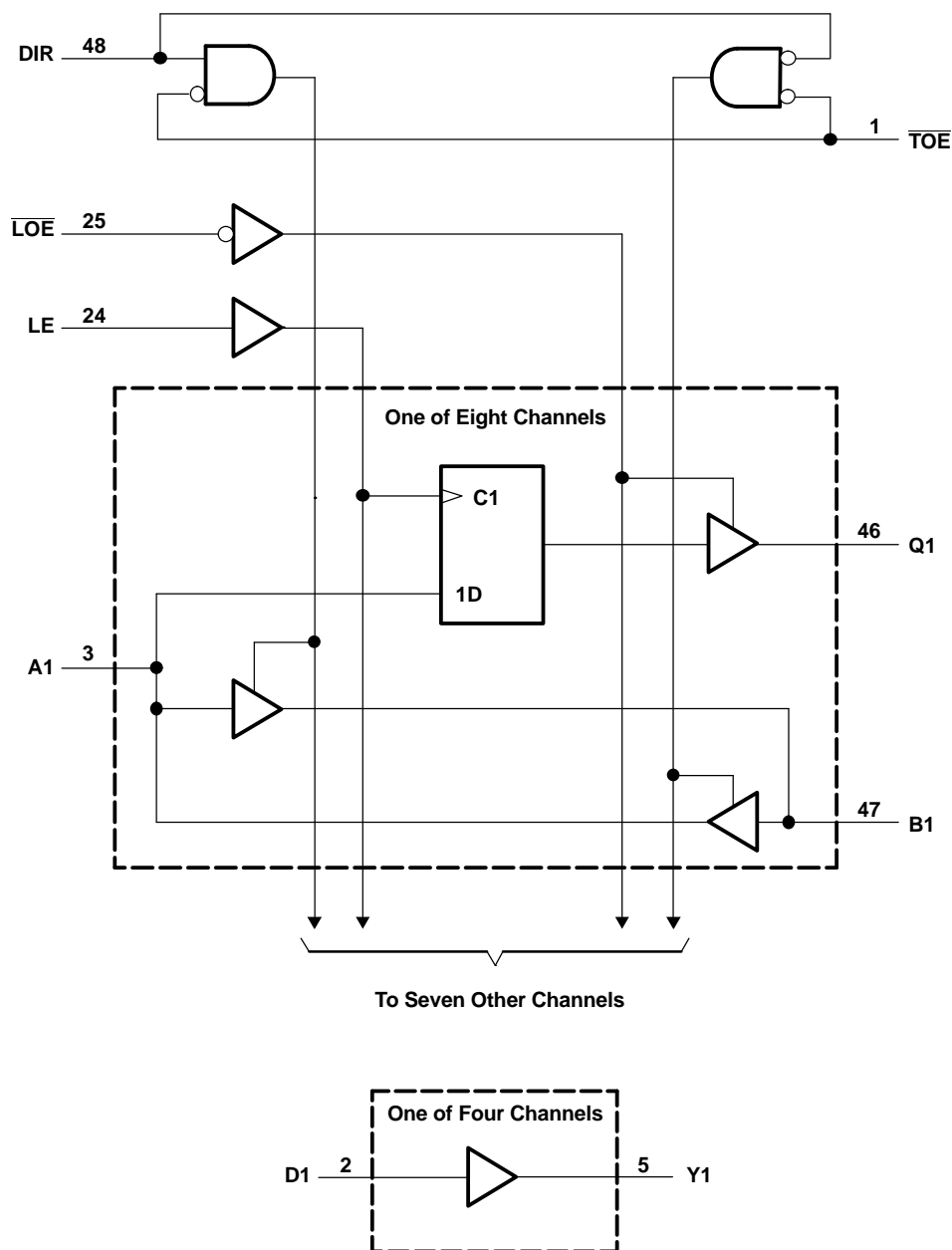
**FUNCTION TABLES**

INPUTS		OPERATION
$\overline{\text{TOE}}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	A bus and B bus isolation

INPUTS			OUTPUT Q
$\overline{\text{LOE}}$	LE	A	
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

INPUT D	OUTPUT Y
L	L
H	H

LOGIC DIAGRAM (POSITIVE LOGIC)



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## 8-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH FOUR INDEPENDENT BUFFERS

SCES435B–APRIL 2003–REVISED SEPTEMBER 2004

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	4.6	V
V <sub>I</sub>	Input voltage range	Except I/O and D input ports <sup>(2)</sup>	-0.5	4.6	V
		I/O and D input ports <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	
V <sub>O</sub>	Output voltage range <sup>(2)(3)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current			±50	mA
	Continuous current through each V <sub>CC</sub> or GND			±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DGG package		70	°C/W
		DGV package		58	
		DL package		63	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JEDEC 51-7.

### RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		1.65	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
		V <sub>CC</sub> = 3 V to 3.6 V		0.8	
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		-4	mA
		V <sub>CC</sub> = 2.3 V		-12	
		V <sub>CC</sub> = 2.7 V		-12	
		V <sub>CC</sub> = 3 V		-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4	mA
		V <sub>CC</sub> = 2.3 V		12	
		V <sub>CC</sub> = 2.7 V		12	
		V <sub>CC</sub> = 3 V		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN TYP <sup>(1)</sup> MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = -100 µA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	V
		I <sub>OH</sub> = -4 mA	1.65 V	1.2	
		I <sub>OH</sub> = -6 mA	2.3 V	2	
		I <sub>OH</sub> = -12 mA	2.3 V	1.7	
			2.7 V	2.2	
			3 V	2.4	
		I <sub>OH</sub> = -24 mA	3 V	2	
V <sub>OL</sub>		I <sub>OL</sub> = 100 µA	1.65 V to 3.6 V	0.2	V
		I <sub>OL</sub> = 4 mA	1.65 V	0.45	
		I <sub>OL</sub> = 6 mA	2.3 V	0.4	
		I <sub>OL</sub> = 12 mA	2.3 V	0.7	
			2.7 V	0.4	
		I <sub>OL</sub> = 24 mA	3 V	0.55	
I <sub>I</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	±5	µA
I <sub>BHL</sub> <sup>(2)</sup>		V <sub>I</sub> = 0.57 V	1.65 V	25	µA
		V <sub>I</sub> = 0.7 V	2.3 V	45	
		V <sub>I</sub> = 0.8 V	3 V	75	
I <sub>BHH</sub> <sup>(3)</sup>		V <sub>I</sub> = 1.07 V	1.65 V	-25	µA
		V <sub>I</sub> = 1.7 V	2.3 V	-45	
		V <sub>I</sub> = 2 V	3 V	-75	
I <sub>BHLO</sub> <sup>(4)</sup>		V <sub>I</sub> = 0 to V <sub>CC</sub>	1.95 V	200	µA
			2.7 V	300	
			3.6 V	500	
I <sub>BHHO</sub> <sup>(5)</sup>		V <sub>I</sub> = 0 to V <sub>CC</sub>	1.95 V	-200	µA
			2.7 V	-300	
			3.6 V	-500	
I <sub>OZ</sub> <sup>(6)</sup>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V	±10	µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	30	µA
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V	750	µA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	3	pF
	D			4	
C <sub>io</sub>	A ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	4.5	pF
	B ports			4.5	
C <sub>o</sub>	Q	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	3	pF

- (1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.
- (2) The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub> max.
- (3) The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.
- (4) An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.
- (5) An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.
- (6) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

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## 8-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH FOUR INDEPENDENT BUFFERS

SCES435B–APRIL 2003–REVISED SEPTEMBER 2004

### TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, LE high	2		2		2		ns
$t_{su}$	Setup time, data before LE↓	0.9		0.9		0.9		ns
$t_h$	Hold time, data after LE↓	0.9		0.9		0.9		ns

### SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	
$t_{pd}$	D	Y	2.2	0.5	3.2	0.5	3	ns
	A	Q	2.2	0.5	3.2	0.5	3	
	LE		2.8	0.5	3.3	0.5	3	
	A or B	B or A	2.2	0.5	3.2	0.5	3	
$t_{en}$	$\overline{LOE}$	Q	2.9	0.7	4.9	0.7	4.7	ns
	$\overline{TOE}$	A or B	3	0.7	4.6	0.7	4.4	
	DIR		3.4	0.7	4.9	0.7	4.7	
$t_{dis}$	$\overline{LOE}$	Q	2.8	0.5	4.3	0.5	4.1	ns
	$\overline{TOE}$	A or B	3.2	0.5	4.3	0.5	4.1	
	DIR		3.4	0.5	4.9	0.5	4.7	

## OPERATING CHARACTERISTICS<sup>(1)</sup>

$T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	
$C_{pd}^{(2)}$ (each output)	Power dissipation capacitance	A outputs enabled, Q outputs disabled, One A output switching	One $f_A = 10\text{ MHz}$ , One $f_B = 10\text{ MHz}$ , $\overline{TOE} = \text{GND}$ , $\overline{LOE} = V_{CC}$ , $\text{DIR} = \text{GND}$ , $C_L = 0\text{ pF}$	12	14	19	pF
		B outputs enabled, Q outputs disabled, One B output switching	One $f_A = 10\text{ MHz}$ , One $f_B = 10\text{ MHz}$ , $\overline{TOE} = \text{GND}$ , $\overline{LOE} = V_{CC}$ , $\text{DIR} = \text{GND}$ , $C_L = 0\text{ pF}$	12	14	21	
		Q outputs enabled, A and B I/Os isolated, One Q output switching	One $f_A = 10\text{ MHz}$ , One $f_{LE} = 20\text{ MHz}$ , One $f_Q = 10\text{ MHz}$ , $\overline{TOE} = V_{CC}$ , $\overline{LOE} = \text{GND}$ , $C_L = 0\text{ pF}$	11	13	19	
		One Y output switching, A and B I/Os isolated, Q outputs disabled	One $f_D = 10\text{ MHz}$ , One $f_Y = 10\text{ MHz}$ , $\overline{TOE} = V_{CC}$ , $\overline{LOE} = V_{CC}$ , $C_L = 0\text{ pF}$	7	8	12	
$C_{pd}^{(2)}$	Power dissipation capacitance	A and B I/Os isolated, Q outputs disabled, One LE and one A data input switching	One $f_A = 10\text{ MHz}$ , One $f_{LE} = 20\text{ MHz}$ , $f_Q$ not switching, $\overline{TOE} = V_{CC}$ , $\overline{LOE} = V_{CC}$ , $C_L = 0\text{ pF}$	4	5	11	pF
$C_{pd}^{(3)}$ (each LE)	Power dissipation capacitance	A and B I/Os isolated, Q outputs disabled, One LE input switching	$f_A$ not switching, One $f_{LE} = 20\text{ MHz}$ , $f_Q$ not switching, $\overline{TOE} = V_{CC}$ , $\overline{LOE} = V_{CC}$ , $C_L = 0\text{ pF}$	6	7	9	pF

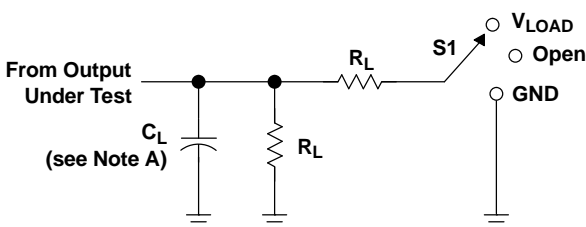
- (1) Total device  $C_{pd}$  for multiple (m) outputs switching and (n) LE inputs switching =  $[m * C_{pd} \text{ (each output)}] + [n * C_{pd} \text{ (each LE)}]$ .  
(2)  $C_{pd}$  (each output) is the  $C_{pd}$  for each data bit (input and output circuitry) when it operates at 10 MHz (Note: the LE is operating at 20 MHz in this test, but its  $I_{CC}$  component has been subtracted).  
(3)  $C_{pd}$  (each LE) is the  $C_{pd}$  for the clock circuitry only when it operates at 20 MHz.

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SCES435B–APRIL 2003–REVISED SEPTEMBER 2004

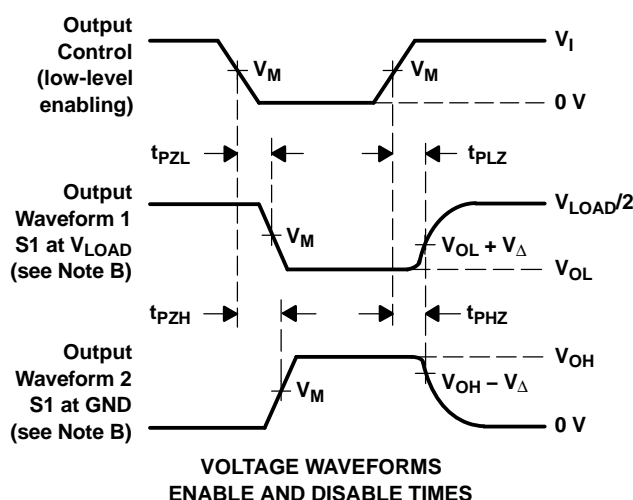
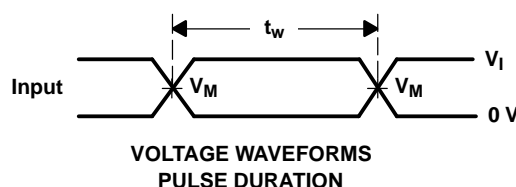
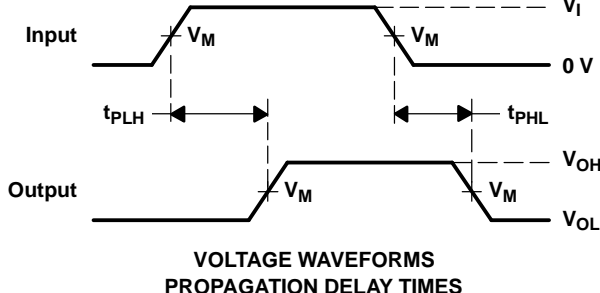
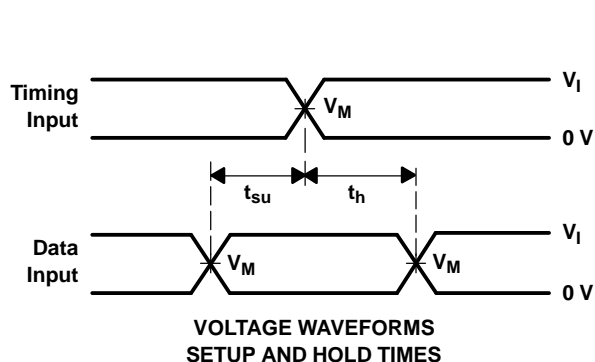
### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUT		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
1.8 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALVCH16973DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16973	<a href="#">Samples</a>
SN74ALVCH16973DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VH973	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16973DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ALVCH16973DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16973DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ALVCH16973DGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

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