National Semiconductor

PRELIMINARY

DM54ALS679/DM74ALS679, DM54ALS680/DM74ALS680 Address Comparators

General Description

The 'ALS679 and 'ALS680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The 'ALS679 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high, regardless of the A and P inputs. The 'ALS680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

Features

- 'ALS679 is a 12-bit to 4-bit comparator with enable
- 'ALS680 is a 12-bit to 4-bit comparator with latch
- Switching specifications at 50 pF
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching specifications guaranteed over full temperature and V_{CC} range

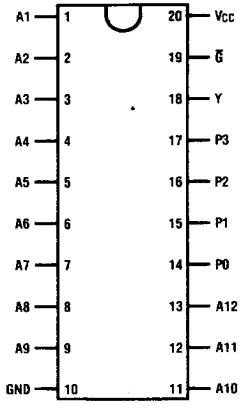
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Packages



TOP VIEW

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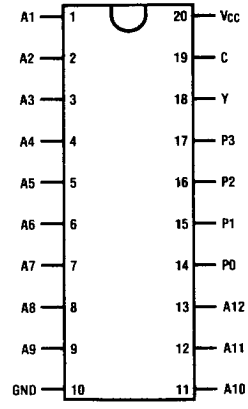
DM54ALS679 (J) **DM74ALS679 (J, N)**



TOP VIEW

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DM54ALS680 (J) **DM74ALS680 (J, N)**

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Recommended Operating Conditions

Symbol	Parameter	DM54ALS679, 680			DM74ALS679, 680			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free Air Temperature Range	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

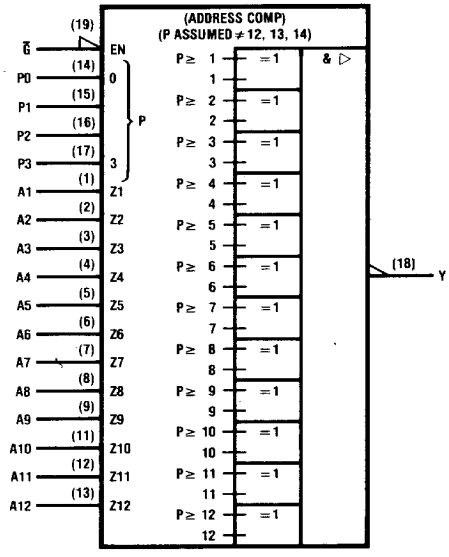
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, I_{OH} = Max		2.4	3.2		V
		$I_{OH} = -400\ \mu A$, $V_{CC} = 4.5$ to 5.5V		$V_{CC}-2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54ALS $I_{OL} = 12mA$		0.25	0.4	V
			74ALS $I_{OL} = 24mA$		0.35	0.5	V
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$, $V_{IN} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$				−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_{OUT} = 2.25V$		−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	ALS679		12.6	28	mA
			ALS680		13.4		

Function Table

'ALS679 $\overline{G}$	'ALS680 C	Inputs Common to 'ALS679 and 'ALS680																Output Y
		P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	H	H	H	L	L*
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	H	H	L	L*
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L*
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	All Other Combinations																H
H		'ALS679: Any Combination																H
	L	'ALS680: Any Combination																Latched

Logic Symbols

'ALS679



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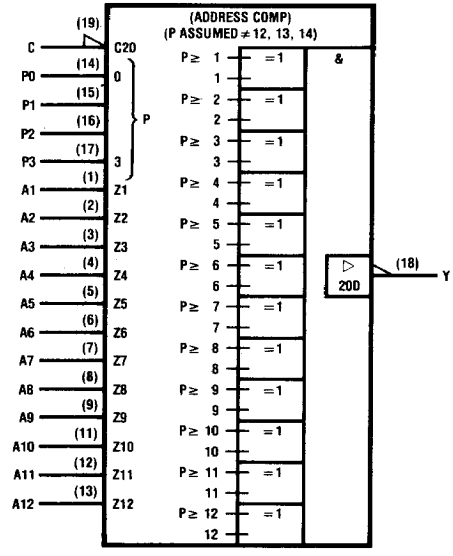
'ALS680



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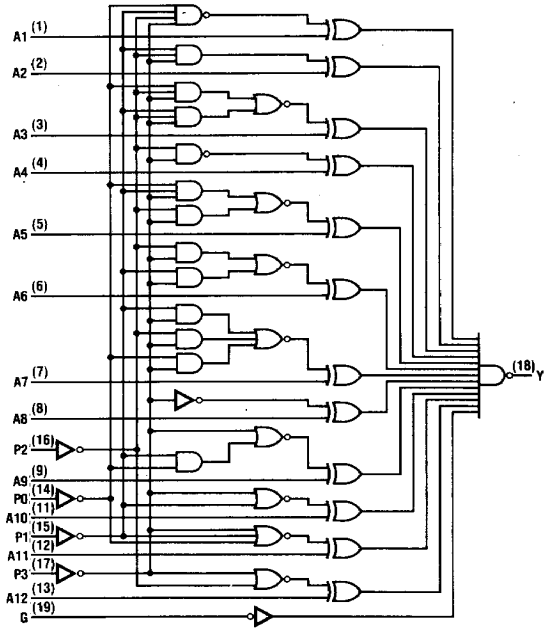
*The three shaded rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for these combinations in which P = 12, 13, and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P ≥ 9 to P = 9...11/13...15, P ≥ 10 to P = 10/11/14/15, and P ≥ 11 to P = 11/15.

Pin numbers shown are for J and N packages.

Logic Diagrams (Positive Logic)

'ALS679



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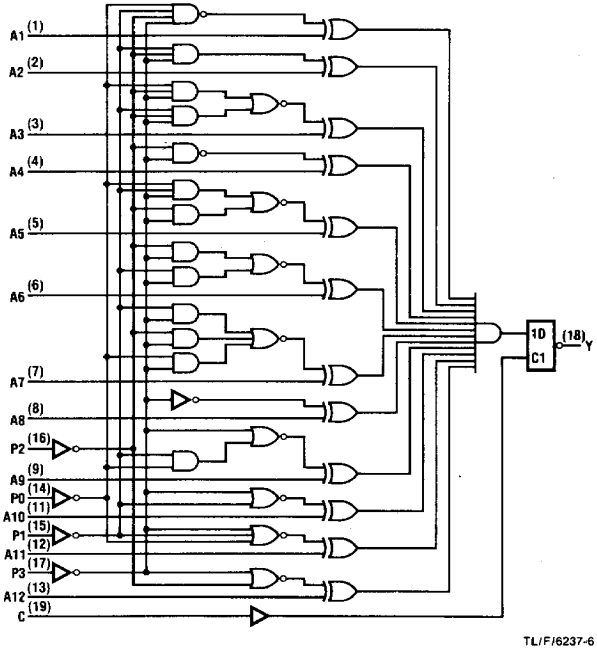
'ALS680



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Pin numbers shown are for J and N packages.

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	From	To	Conditions	DM54ALS679, 680			DM74ALS679, 680			Units
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Any P	Y	$V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, $R_L = 500\Omega$	4	18	28	4	18	25	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				8	18	40	8	18	35	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Any A	Y		5	14	26	5	14	22	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				5	14	35	5	14	30	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	$\overline{G}$ (ALS679)	Y		3	10	15	3	10	13	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				5	10	30	5	10	25	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	C (ALS680)	Y			14			14		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					14			14		ns

Note 1: See Section 1 for test waveforms and output load.

Typical Application Information

The 'ALS679 and 'ALS680 can be wired to recognize any one of 2^{12} addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 12-bit system address is:

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 4 lows and 8 highs, the following connections are made:

P3 to 0V, P2 to V_{CC}, P1 to 0V, and P0 to 0V.

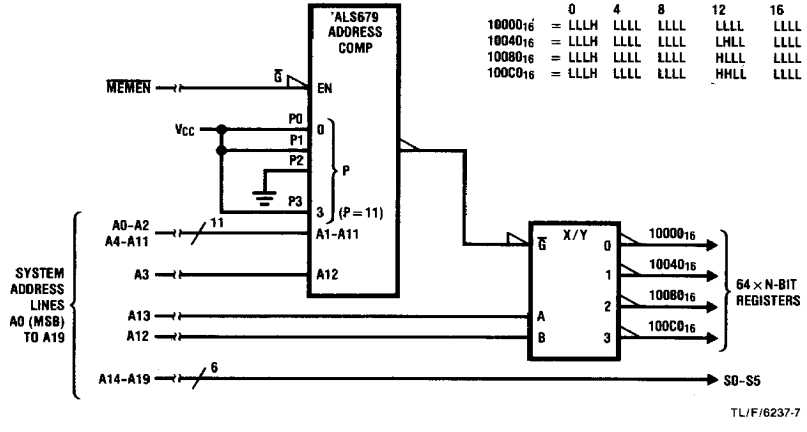
System address lines A9, A8, A5, and A4 to comparator inputs A1 through A4 in any convenient order.

The remaining eight system address lines to comparator inputs A5 through A12 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a register bank decoder that examines the 14 most significant bits (A0 through A13) of a 20-bit address to select banks corresponding to the hex addresses 10000, 10040, 10080, and 100C0.

Register Bank Decoder



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