

Control Integrated POver System (CIPOS™)

IKCS12G60DA

IKCS12G60DC

<http://www.lspst.com>



For Power Management
Application

LS Power Semitech
A joint venture with infineon

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CIPOS™

Control Integrated POver System

Single In-Line Intelligent Power Module

3Φ-bridge 600V / 12A @ 25°C



Features

- TrenchStop® IGBTs with lowest $V_{CE(sat)}$
- Optimal adapted anti parallel diode for low EMI
- Integrated bootstrap diode and capacitor
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Current measurement shunt integrated
- Overcurrent shutdown
- Temperature monitor
- Under voltage lockout at all channels
- Fault-signal
- Matched propagation delay for all channels
- Cross-conduction prevention
- Lead-free terminal plating; RoHS compliant
- Qualified according to JEDEC ¹ (high temperature stress tests for 1000h) for target applications

Target Applications

- Washing machines
- Consumer Fans and Consumer Compressors

Description

The CIPOS™ module family offers the chance for integrating various power and control components to increase reliability, optimize PCB size and system costs.

This SIL-IPM is designed to control AC motors in variable speed drives for applications like air conditioning, compressors and washing machines. The package concept is specially adapted to power applications, which need extremely good thermal conduction and electrical isolation, but also EMI-save control and overload protection. The features of TrenchStop® IGBTs and anti parallel diodes are combined with a new optimized Infineon SOI gate driver for excellent electrical performance. The integrated shunt improves the overall performance of the module.

System Configuration

- 3 half-bridges with TrenchStop® IGBT & FW-diodes
- 3Φ SOI gate driver
- Bootstrap diodes for high side supply
- Integrated 100nF bootstrap capacitance
- Temperature sensor, passive components for adaptations
- Isolated heatsink
- Creepage distance typ 3.2mm

Certification

UL 1577 (UL file E314539)

¹ J-STD-020 and JESD-022

[illegible]

Figure 1: Internal Schematic

Pin Assignment

Pin Number	Pin Name	Pin Description
1	VB3	High side floating IC supply voltage
2	W,VS3	Motor output W, high side floating IC supply offset voltage
3	na	None
4	VB2	High side floating IC supply voltage
5	V,VS2	Motor output V, high side floating IC supply offset voltage
6	na	None
7	VB1	High side floating IC supply voltage
8	U,VS1	Motor output U, high side floating IC supply offset voltage
9	na	None
10	V+	Positive bus input voltage
11	na	None
12	Sh	Closed low side emitter with internal shunt
13	TEMP	Temperature control
14	VDD	IC main supply +15V
15	/HIN1	Input gate driver high side 1/U
16	/HIN2	Input gate driver high side 2/V
17	/HIN3	Input gate driver high side 3/W
18	/LIN1	Input gate driver low side 1/U
19	/LIN2	Input gate driver low side 2/V
20	/LIN3	Input gate driver low side 3/W
21	EN, /FAULT	Input logic enable, Indicates over-current and under-voltage (negative logic, open-drain output)
22	ITRIP	Input over current shutdown
23	VSS	IC negative supply

Pin Description

/HIN1,2,3 and /LIN1,2,3 (Low side and high side control pins, Pin 15 - 20)

These pins are active low and they are

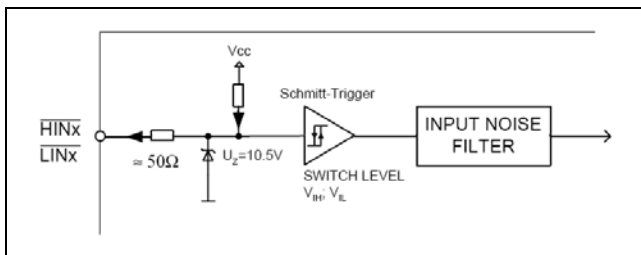


Figure 2: Input pin structure

responsible for the control of the integrated IGBT.

The Schmitt-trigger input threshold of them are such to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs. Pull-up resistor of about 75kΩ is internally provided to pre-bias inputs during supply start-up and a zener clamp is provided for pin protection purposes. Input schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

It is recommended for proper work of CIPOS™ not to provide input pulse-width lower than 1μs.

The integrated gate drive provides additionally a shoot through prevention capability which avoids the simultaneous on-state of two gate drivers of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3).

A minimum deadtime insertion of typ 380ns is also provided, in order to reduce cross-conduction of the external power switches.

EN, /FAULT (Pin 21)

The signal applied to pin EN controls directly the output stages. All outputs are set to LOW, if EN is at LOW logic level. The internal structure of the pin is the same as Figure 2 made exception of the switching levels of the Schmitt-Trigger, which are here $V_{EN,TH+} = 2.1V$ and $V_{EN,TH-} = 1.3V$. The typical propagation delay time is $t_{EN} = 900ns$. A pull down resistor of typ. 75kΩ keeps the system off in case of lack of control signal.

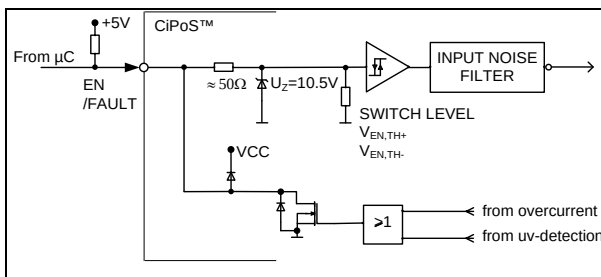


Figure 3: Internal circuit at pin EN

This pin is also used for indication of exceptional conditions, such as over current or under voltage of the control section of the gate drive IC. The on-resistance of the internal open-drain FET is typically 56Ω.

TEMP (Temperature monitor, Pin 13)

The integrated NTC-resistor is given in section Integrated Components.

ITRIP (Over-current detection, Pin 22)

The over current signal is provided by the integrated shunt resistor. CIPOS™ provides an over-current detection function. The integrated ITRIP comparator threshold (typ 0.46V) is referenced to VSS ground. An input noise filter (typ: $t_{TRIPMIN} = 225ns$) prevents the driver to detect false over-current events. The over-current detection generates a hard shut down of all outputs of the gate driver after the propagation delay of typically 900ns.

As soon as the over current detector triggers, the /FAULT signal is activated, which pulls down the enable pin.

VDD, VSS (control side supply and reference, Pin 14, 23)

VDD is the low side supply and it provides power both to input logic and to low side output power stage. Input logic is referenced to VSS ground as well as the under-voltage detection circuit.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of $V_{DDUV+} = 12.1V$ is at least present.

The IC shuts down all the gate drivers power outputs, when the VDD supply voltage is below $V_{DDUV-} = 10.4V$. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

VB1,2,3 and VS1,2,3 (High side supplies, Pin 1, 2, 4, 5, 7, 8)

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter/source voltage.

Due to the low power consumption, the floating driver stage is supplied by an integrated bootstrap circuit connected to VDD. This includes also integrated bootstrap capacitors of 100nF at each floating supply, which are located very close to the gate drive circuit.

The under-voltage detection operates with a rising supply threshold of typical $V_{BSUV+} = 12.1V$ and a falling threshold of $V_{DDUV-} = 10.4V$ according to Figure 4.

VS1,2,3 provide a high robustness against negative voltage in respect of VSS of -50V. This ensures very stable designs even under rough conditions.

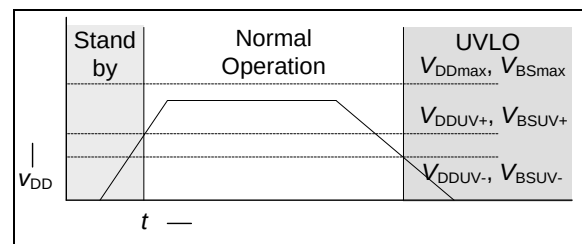


Figure 4: Operation modes

V+ (positive bus input voltage, Pin 10)

The high side IGBT are connected to the bus voltage. It is recommended, that the bus voltage does not exceed 500V.

Sh (shunt negative potential, Pin 12)

This pin is the available terminal of the shunt resistor, which is usually connected to the reference voltage of CIPOS™.

Absolute Maximum Ratings

($T_J = 25^\circ\text{C}$, $V_{DD} = 15\text{V}$ Unless Otherwise Specified):

Module Section

Description	Condition	Symbol	Value		Unit
			Min	max	
Storage temperature range		T_{stg}	-40	125	$^\circ\text{C}$
Operating temperature control PCB ¹		T_{PCB}	-	125	$^\circ\text{C}$
Solder temperature	Wave soldering, 1.6mm (0.063in.) from case for 10s	T_{sol}	-	260	$^\circ\text{C}$
Insulation test voltage	RMS, f=50Hz, t =1min	V_{ISOL}	2500	-	V
Mounting torque	M3 screw and washer	M_S	-	0.6	Nm
Mounting pressure on surface	Package flat on mounting surface	N_{MC}	-	150	N/mm ²
Creepage distance		d_S	3.1	-	mm
Max. peak power of bootstrap resistor	$t_p = 100\mu\text{s}$ $T_c = 100^\circ\text{C}$	P_{BRpeak}		90	W

IGBT and Diode Section

Description	Condition	Symbol	Value		Unit
			min	max	
Max. Blocking Voltage		V_{CES}	600	-	V
DC output current	$T_c = 25^\circ\text{C}, T_{\text{vj}} < 150^\circ\text{C}$ $T_c = 80^\circ\text{C}, T_{\text{vj}} < 150^\circ\text{C}$	I_u, I_v, I_w	-12 -6	12 6	A
Repetitive peak collector current	t_p limited by T_{vjmax}	I_u, I_v, I_w	-18	18	A
Short circuit withstand time ²	$V_{DD} = 15\text{V}, V_{DC} = 400\text{V},$ $T_{\text{vj}} = 150^\circ\text{C}$	t_{sc}	-	5	μs
IGBT reverse bias safe operating area (RBSOA)	$V_{DD} = 15\text{V}, V_{DC} \leq 500\text{V},$ $T_{\text{vj}} = 150^\circ\text{C}, I_c = 6\text{A}$ $V_{\text{CEmax}} = 600\text{V}$		Full Square		
Power dissipation per IGBT	$T_c = 25^\circ\text{C}$	P_{tot}	-	35	W
Operating junction temperature range	IGBT Diode	T_{vjI} T_{vjD}	-40 -40	150 150	$^\circ\text{C}$

¹ Monitored by pin 13

² Allowed number of short circuits: <1000; time between short circuits: >1s.

Description	Condition	Symbol	Value		Unit
			min	max	
Single IGBT thermal resistance, junction-case		R_{thJC}	-	3.0	K/W
Single diode thermal resistance, junction-case		R_{thJCD}	-	4.2	

Control Section

Description	Condition	Symbol	Value		Unit
			min	max	
Module supply voltage		V_{DD}	-1	20	V
High side floating supply voltage (VB vs. VS)		V_{BS}	-1	20	
High side floating IC supply offset voltage	$t_p < 500ns$	$V_{S1,2,3}$	VDD-VBS-6 VDD-VBS-50	600	
Input voltage	/LIN, /HIN, EN, ITRIP	V_{in}	-1	10	
Operating junction temperature ¹		$T_{J,IC}$	-	125	°C
Max. switching frequency		f_{PWM}	-	20	kHz

Recommended Operation Conditions

All voltages are absolute voltages referenced to V_{SS} -Potential unless otherwise specified.

Description	Symbol	Value		Unit
		min	max	
High side floating supply offset voltage	V_S	-3	500	V
High side floating supply voltage (V_B vs. V_S)	V_{BS}	12.5	17.5	
High side output voltage (V_{HO} vs. V_S)	V_{HO}	0	V_{BS}	
Low side power supply	V_{DD}	12.5	17.5	
Logic input voltages LIN,HIN,EN,ITRIP	V_{IN}	0	5	

¹ Monitored by pin 13

Static Characteristics

(T_c = 25°C, V_{DD} = 15V, if not stated otherwise)

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Collector-Emitter breakdown voltage	V _{IN} = 5V, I _C = 0.25 mA	V _{(BR)CES}	600	-	-	V
Collector-Emitter saturation voltage	V _{DD} = 15V, I _{out} = +/- 6A T _{vj} = 25°C T _{vj} = 150°C	V _{CE(sat)}	- -	1.6 1.9	2.1	V
Diode forward voltage	V _{IN} = 5V, I _{out} = +/- 6A T _{vj} = 25°C T _{vj} = 150°C	V _F	- -	1.65 1.6	2.05	V
Zero gate voltage collector current of IGBT	V _{CE} = 600V, V _{IN} = 5V T _{vj} = 25°C T _{vj} = 150°C	I _{CES}	- -	- -	40 1000	μA
Short circuit collector current ¹	V _{DD} = 15V, t _{SC} ≤ 5μs V _{CC} = 400V, T _{vj} = 150°C	I _{C(SC)} ²	-	40	-	A
Logic "0" input voltage (LIN,HIN)		V _{IH}	1.7	2.1	2.4	V
Logic "1" input voltage (LIN,HIN)		V _{IL}	0.7	0.9	1.1	V
EN positive going threshold		V _{EN,TH+}	1.9	2.1	2.3	V
EN negative going threshold		V _{EN,TH-}	1.1	1.3	1.5	V
ITRIP positive going threshold		V _{IT,TH+} ²	360	460	540	mV
ITRIP input hysteresis		V _{IT,HYS} ²	45	75	-	mV
V _{DD} and V _{BS} supply under voltage positive going threshold		V _{DDUV+} ² V _{BSUV+} ²	11.0	12.1	12.8	V
V _{DD} and V _{BS} supply under voltage negative going threshold		V _{DDUV-} ² V _{BSUV-} ²	9.5	10.4	11.0	V
V _{CC} and V _{BS} supply under voltage lockout hysteresis		V _{DDUVH} ² V _{BSUVH} ²	1.2	1.7	-	V
Input clamp voltage (/HIN, /LIN, EN, ITRIP)	I _{IN} = 4 mA	V _{INCLAMP}	9.0	10.1	13.0	V
Quiescent V _{Bx} supply current (V _{Bx} only)	V _{HIN} = low	I _{QB}	-	360	550	μA
Quiescent V _{DD} supply current (V _{DD} only)	V _{IN} = float	I _{QDD}	-	2.0	3.0	mA
Input bias current	V _{IN} = 5V	I _{IN+}	-	55	100	μA
Input bias current	V _{IN} = 0V	I _{IN-}	-	110	200	μA
EN Input bias current	V _{EN} = 5V	I _{EN+}	-	62	120	μA
Leakage current of high side	T _{j,IC} = 125°C	I _{LVS} ²	-	30	-	μA

¹ Allowed number of short circuits: <1000; time between short circuits: >1s.

² Test is not subject of product test, verified by characterisation

Dynamic Characteristics

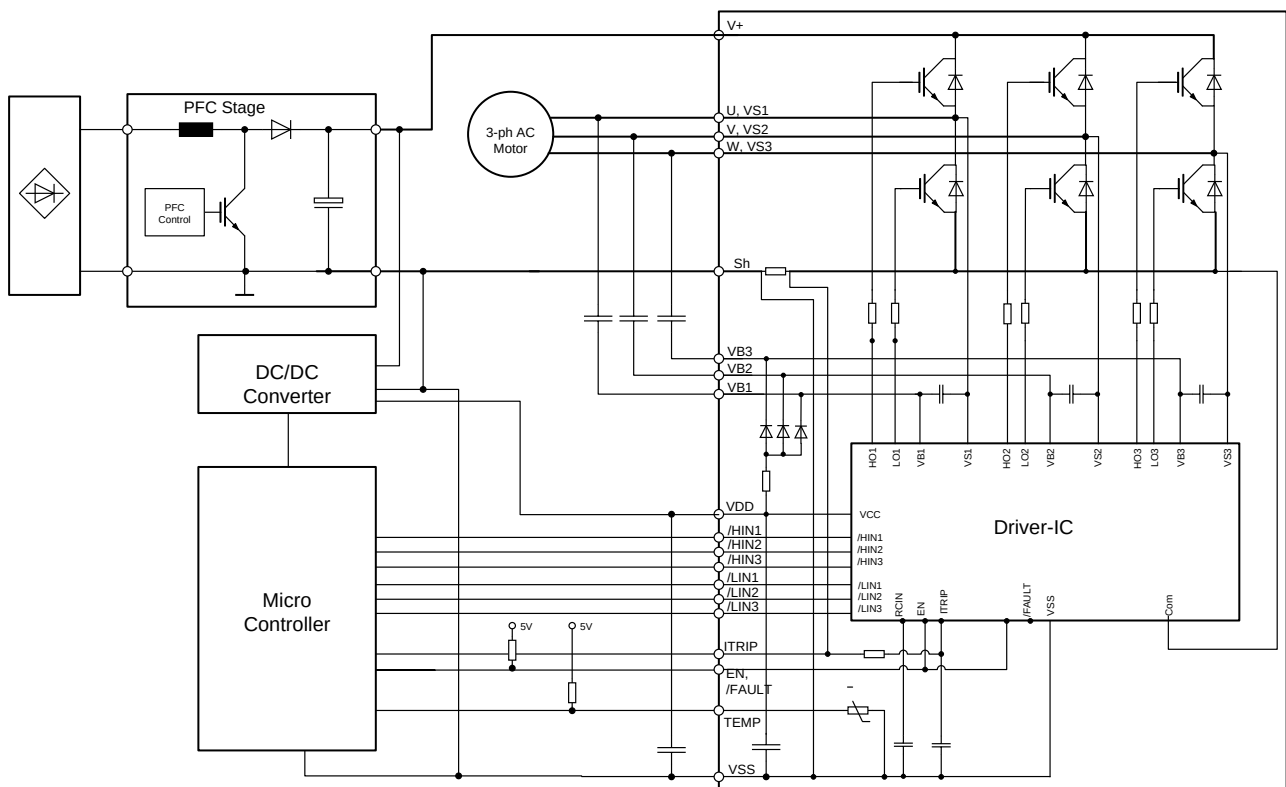
($T_c = 25^\circ\text{C}$, $V_{DD} = 15\text{V}$, if not stated otherwise)

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Turn-on propagation delay High side or low side	$V_{LIN,HIN} = 0\text{V}$; $I_{out} = 6\text{A}$, $V_{DC} = 300\text{V}$	$t_{d(on)}$	-	638	-	ns
Turn-on rise time High side or low side	$I_{out} = 6\text{A}$, $V_{DC} = 300\text{V}$ $V_{LIN,HIN} = 5\text{V}$	t_r	-	22	-	ns
Turn-off propagation delay High side or low side	$V_{LIN,HIN} = 5\text{V}$; $I_{out} = 6\text{A}$, $V_{DC} = 300\text{V}$	$t_{d(off)}$	-	812	-	ns
Turn-off fall time High side or low side	$I_{out} = 6\text{A}$, $V_{DC} = 300\text{V}$ $V_{LIN,HIN} = 0\text{V}$	t_f	-	30	-	ns
Shutdown propagation delay ENABLE	$V_{EN} = 0\text{V}$, I_u , I_v , $I_w = 6\text{A}$	t_{EN}	-	900	-	ns
Shutdown propagation delay ITRIP	$V_{ITRIP} = 1\text{V}$, I_u , I_v , $I_w = 6\text{A}$	t_{ITRIP}	-	900	-	ns
Input filter time ITRIP	$V_{ITRIP} = 1\text{V}$	$t_{ITRIPmin}$	155	210	380	ns
Input filter time at LIN for turn on and off and input filter time at HIN for turn on only	$V_{LIN,HIN} = 0\text{V} \text{ \& } 5\text{V}$	t_{FILIN}	120	270	-	ns
Input filter time at HIN for turn off	$V_{HIN} = 5\text{V}$	t_{FILIN1}	-	220	-	ns
Input filter time at HIN for turn off	$V_{HIN} = 5\text{V}$	t_{FILIN2}	-	400	-	ns
Input filter time EN		t_{FILEN}	300	430	-	ns
Fault clear time after ITRIP-fault	$V_{LIN,HIN} = 0\text{V} \text{ \& } 5\text{V}$ $V_{ITRIP} = 0\text{V}$	t_{FLTCLR}	-	4.7	-	ms
Min. deadtime between low side and high side		DT_{PWM}	-	1	-	μs
Deadtime of gate drive circuit		DT_{IC}	-	380	-	ns
IGBT Turn-on Energy (includes reverse recovery of diode)	$I_{out} = 6\text{A}$, $V_{DC} = 300\text{V}$ $T_{vj} = 25^\circ\text{C}$ $T_{vj} = 150^\circ\text{C}$	E_{on}	- -	89 141	- -	μJ
IGBT Turn-off Energy	$I_{out} = 6\text{A}$, $V_{DC} = 300\text{V}$ $T_{vj} = 25^\circ\text{C}$ $T_{vj} = 150^\circ\text{C}$	E_{off}	- -	123 163	- -	μJ
Diode recovery Energy	$I_{out} = 6\text{A}$, $V_{DC} = 300\text{V}$ $T_{vj} = 25^\circ\text{C}$ $T_{vj} = 150^\circ\text{C}$	E_{rec}	- -	22 59	- -	μJ

Integrated Components

Description	Condition	Symbol ¹	Value			Unit
			min	typ	max	
Resistor (0.25 W)		Rbs	-	10	-	Ω
Shunt-Resistor		Rsh	-	20	-	mΩ
Resistor		R2	-	0.47		kΩ
Resistor	$T_{NTC} = 25^{\circ}\text{C}$	RTS	-	100	-	kΩ
B-Constant of NTC (Negative Temperature Coefficient)	$T_{NTC} = 25^{\circ}\text{C}$	B25	-	4250	-	K
Bootstrap diode forward voltage	$I_{FDBS} = 1\text{A}, T_J = 25^{\circ}\text{C}$	V_{FDBS}	-	1.3	-	V
Capacitor		C1	-	100	-	nF
Capacitor		C2	-	2.2	-	
Capacitor		C3		2.2		
Bootstrap Capacitor		C_{bsH_x}	-	100	-	
Capacitor		Cgex		390		pF

Circuit of a Typical Application



¹ Symbols according to Figure 1

Characteristics

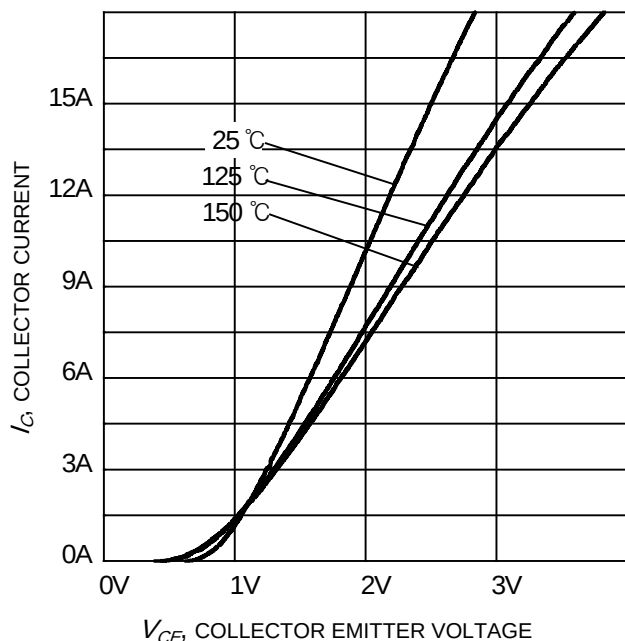


Figure 4. Typical IGBT output characteristic
($V_{DD} = 15V$)

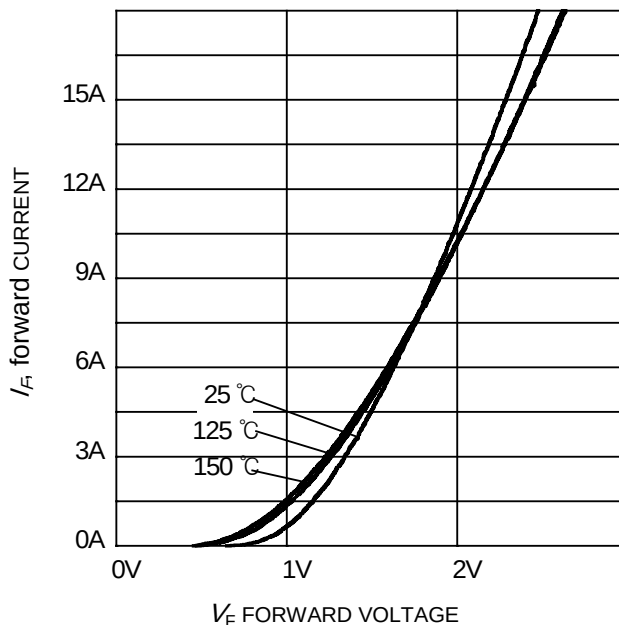


Figure 5. Typical diode forward current as a function of forward voltage

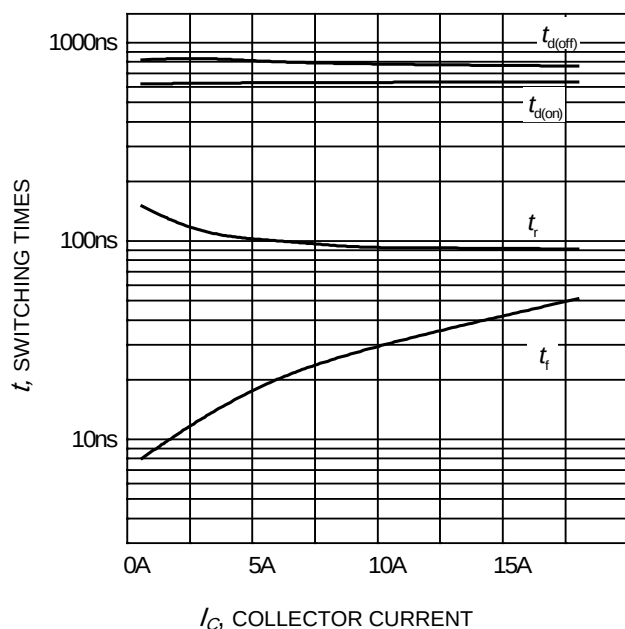


Figure 6. Typical switching times as a function of collector current
(inductive load, $T_J = 150^\circ C$,
 $V_{CE} = 300V$, $V_{DD} = 15V$
Dynamic test circuit in Figure A)

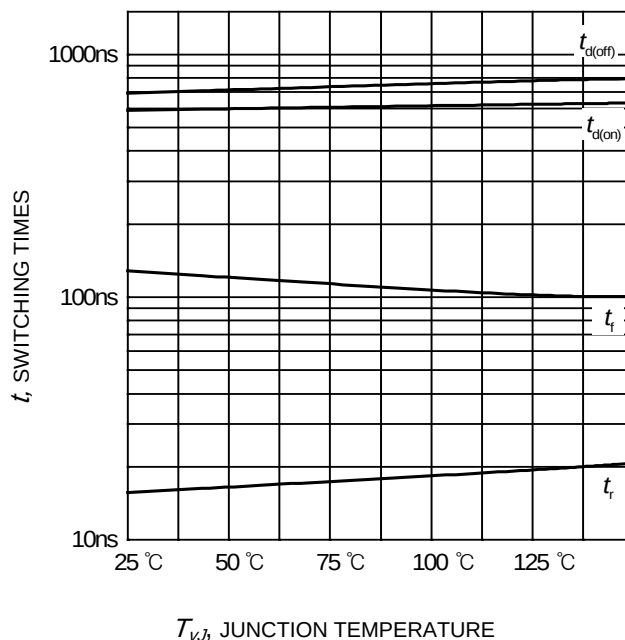


Figure 7. Typical switching times as a function of junction temperature
(inductive load, $V_{CE} = 300V$,
 $V_{DD} = 15V$, $I_C = 6A$
Dynamic test circuit in Figure A)

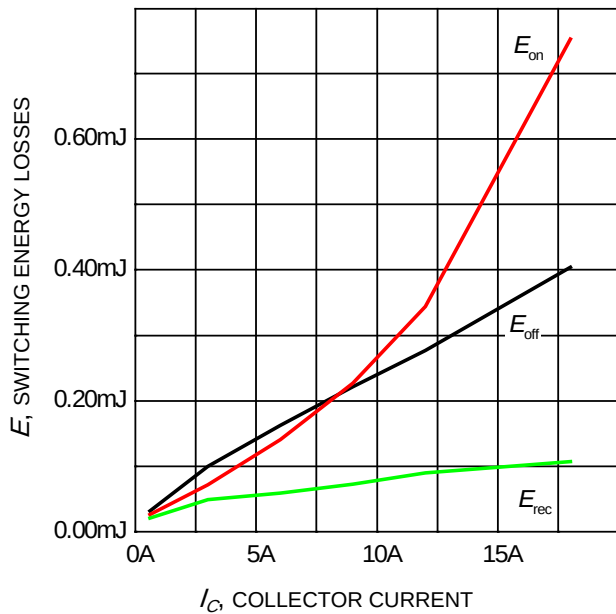


Figure 8. Typical switching energy losses as a function of collector current
(inductive load, $T_J = 150^\circ\text{C}$,
 $V_{CE} = 300\text{V}$, $V_{DD} = 15\text{V}$
Dynamic test circuit in Figure A)

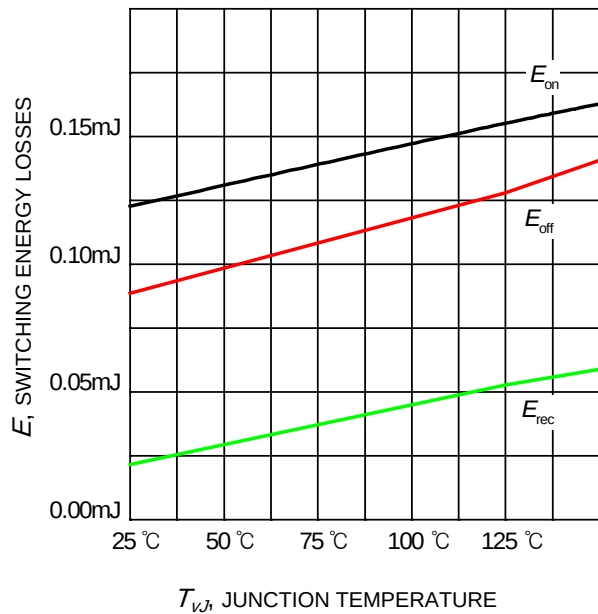


Figure 9. Typical switching energy losses as a function of junction temperature
(inductive load, $V_{CE} = 300\text{V}$,
 $V_{DD} = 15\text{V}$, $I_C = 6\text{A}$
Dynamic test circuit in Figure A)

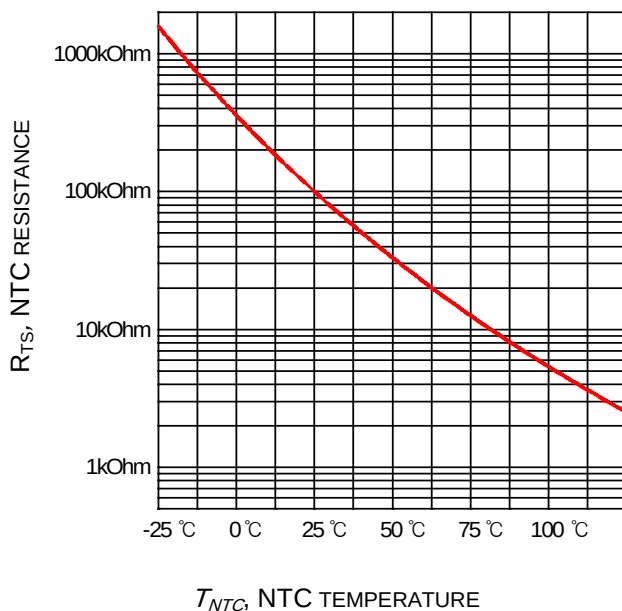


Figure 10. Typical Resistance of NTC as a function of NTC temperature

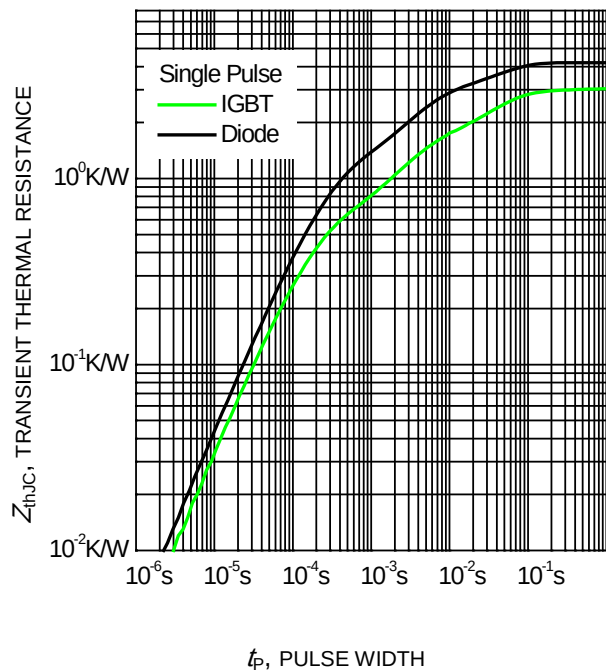


Figure 12. IGBT and Diode transient thermal impedance as a function of pulse width

Test Circuits and Parameter Definition

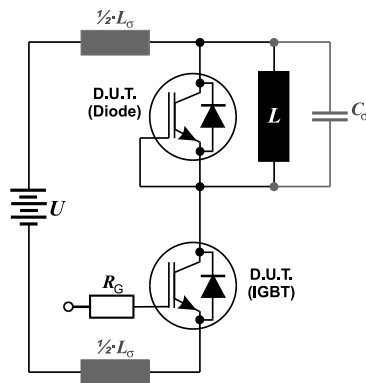


Figure A: Dynamic test circuit
Leakage inductance $L_\sigma = 180\text{nH}$
Stray capacitance $C_\sigma = 39\text{pF}$

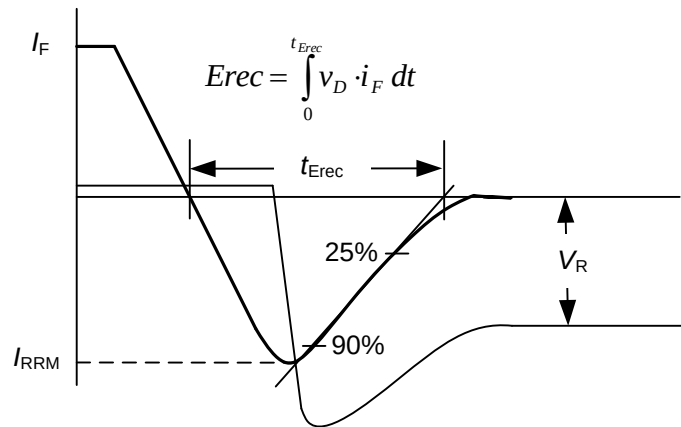


Figure B: Definition of diodes switching characteristics

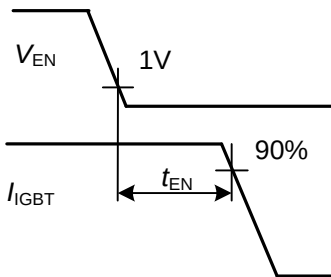


Figure C: Definition of Enable propagation delay

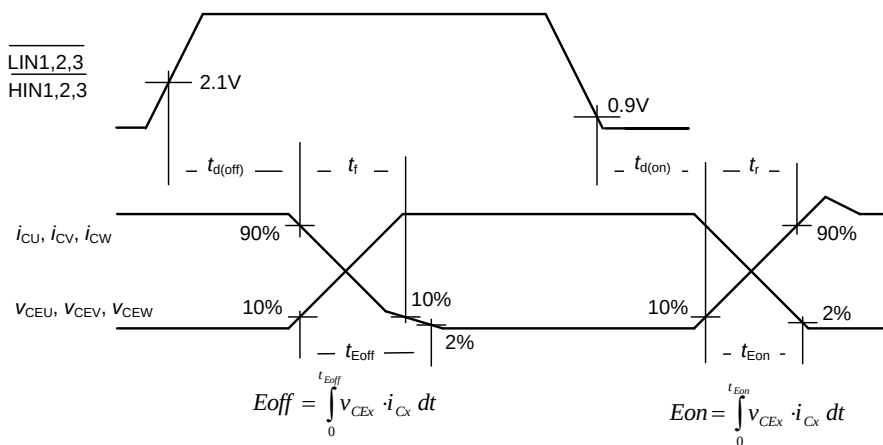


Figure D: Switching times definition and switching energy definition

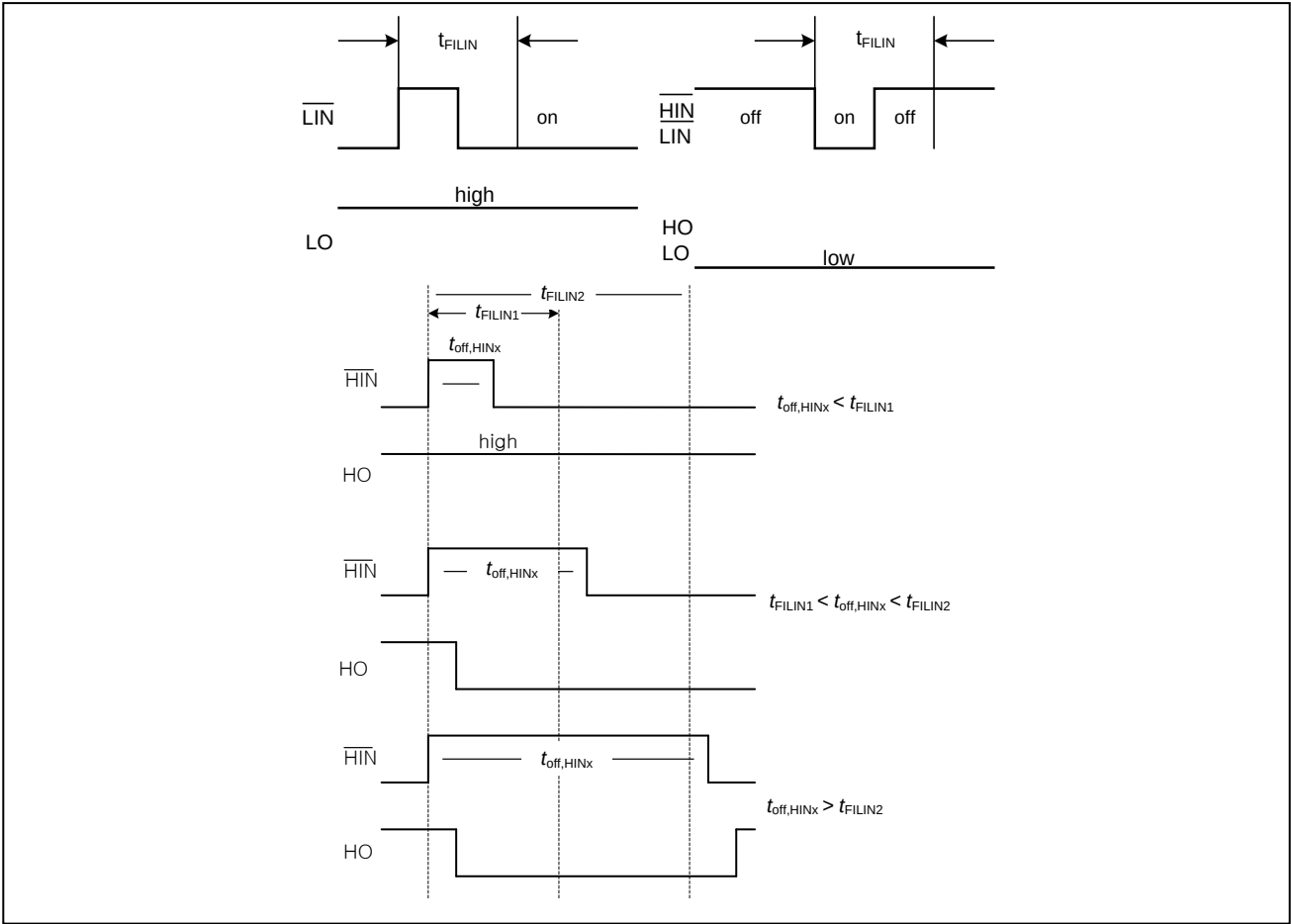
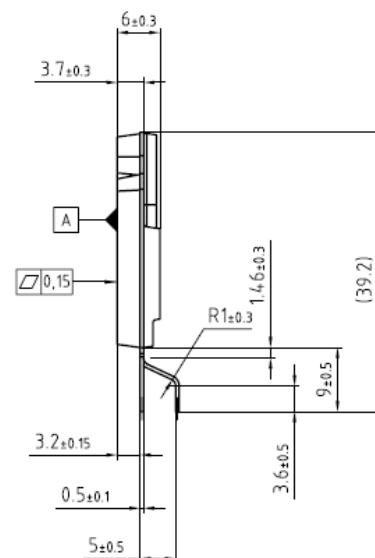


Figure E: Short Pulse suppression



Jun. 2010

Technical drawing of a mold assembly, showing three views: top, front, and side.

Top View:

- Overall width: 50.4 ± 0.3
- Overall height: 38 ± 0.3
- Feature B: 0.25 B
- Feature 2: 0.4 (M) B
- Feature 23x2=46: $23 \times 2 = 46$

Front View:

- Overall width: 30.2 ± 0.3
- Overall height: 30.5 ± 0.4
- Feature 8x4.5°: $8 \times 4.5^\circ$
- Feature 45°: 45°
- Feature 3.5±0.15: 3.5 ± 0.15
- Feature 0.8±0.1: 0.8 ± 0.1
- Feature 2: 2
- Feature 0.4(M)B: 0.4 (M) B
- Feature 23x2=46: $23 \times 2 = 46$
- Feature max.0.12 per side: $\text{max. } 0.12 \text{ per side}$

Side View:

- Overall width: 31 ± 0.3
- Overall height: 1.8 ± 0.5
- Feature 0.5B: 0.5 B
- Feature 10.9±0.3: 10.9 ± 0.3
- Feature 1.8±0.5: 1.8 ± 0.5

Annotations:

- PIN 1 Laser Marking - $\phi 1$
- ejector marks 10 pieces
- punched-mold along this equator side
- mold flash along side of leads

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Weight		m_P	-	17	-	g

Data Sheet