

# HD74LV166A

## Parallel-Load 8-bit Shift Register

REJ03D0321-0300Z  
(Previous ADE-205-268A (Z))  
Rev.3.00  
Jun. 04, 2004

### Description

The HD74LV166A is 8-bit shift register with an output from the last stage. Data may be loaded into the register either in parallel or in serial form. When the Shift/Load input is low, the data is loaded asynchronously in parallel. When the Shift/Load input is high, the data is loaded serially on the rising edge of either clock inhibit or Clock. Clear is asynchronous and active-low.

The 2-input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

### Features

- $V_{CC} = 2.0\text{ V}$  to  $5.5\text{ V}$  operation
- All inputs  $V_{IH}(\text{Max.}) = 5.5\text{ V}$  ( $@V_{CC} = 0\text{ V}$  to  $5.5\text{ V}$ )
- All outputs  $V_O(\text{Max.}) = 5.5\text{ V}$  ( $@V_{CC} = 0\text{ V}$ )
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V}$  ( $@V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot  $> 2.3\text{ V}$  ( $@V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Output current  $\pm 6\text{ mA}$  ( $@V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ),  $\pm 12\text{ mA}$  ( $@V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ )
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV166AFPEL	SOP-16 pin(JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74LV166ARPEL	SOP-16 pin(JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)
HD74LV166ATELL	TSSOP-16 pin	TTP-16DAV	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

## Function Table

Inputs						Internal outputs		Output
$\overline{\text{CLR}}$	$\text{SH}/\overline{\text{LD}}$	CLK INH	CLK	SER	A ... H	QA	QB	QH
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$
H	L	L	$\uparrow$	X	a ... h	a	b	h
H	H	L	$\uparrow$	H	X	H	$Q_{An}$	$Q_{Gn}$
H	H	L	$\uparrow$	L	X	L	$Q_{An}$	$Q_{Gn}$
H	X	H	$\uparrow$	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$

Note: H: High level

L: Low level

$\uparrow$ : Low to high transition

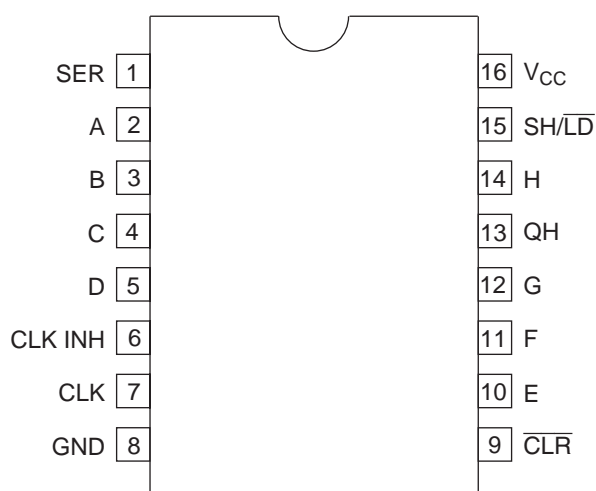
X: Immaterial

a ... h: Parallel data

$Q_{A0} \dots Q_{H0}$ : Outputs remain unchanged.

$Q_{An} \dots Q_{Gn}$ : Data shifted from the previous stage on a positive edge at the clock input.

## Pin Arrangement



(Top view)

### Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V	
Input voltage range* <sup>1</sup>	$V_I$	-0.5 to 7.0	V	
Output voltage range* <sup>1, 2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L $V_{CC}$ : OFF
Input clamp current	$I_{IK}$	-20	mA	$V_I < 0$
Output clamp current	$I_{OK}$	$\pm 50$	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	$\pm 25$	mA	$V_O = 0$ to $V_{CC}$
Continuous current through $V_{CC}$ or GND	$I_{CC}$ or $I_{GND}$	$\pm 50$	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* <sup>3</sup>	$P_T$	785 500	mW	SOP TSSOP
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

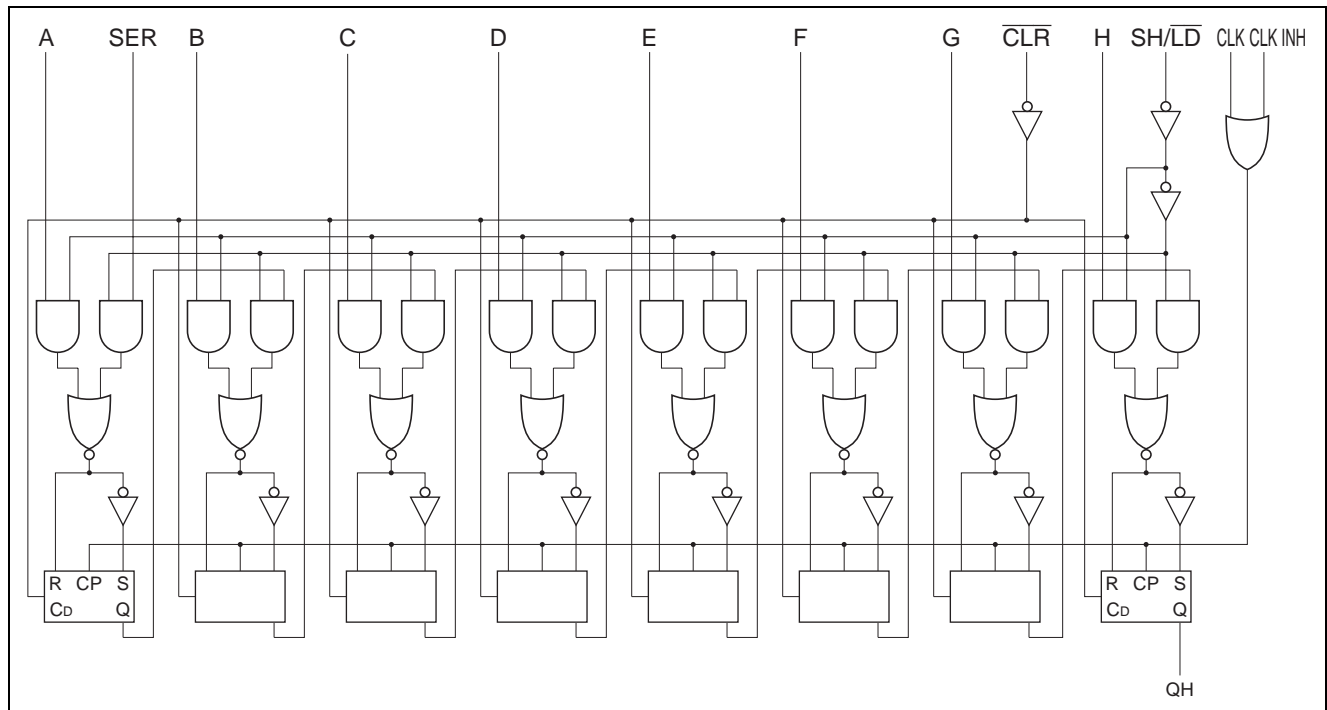
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of  $150^\circ\text{C}$ .

### Recommended Operating Conditions

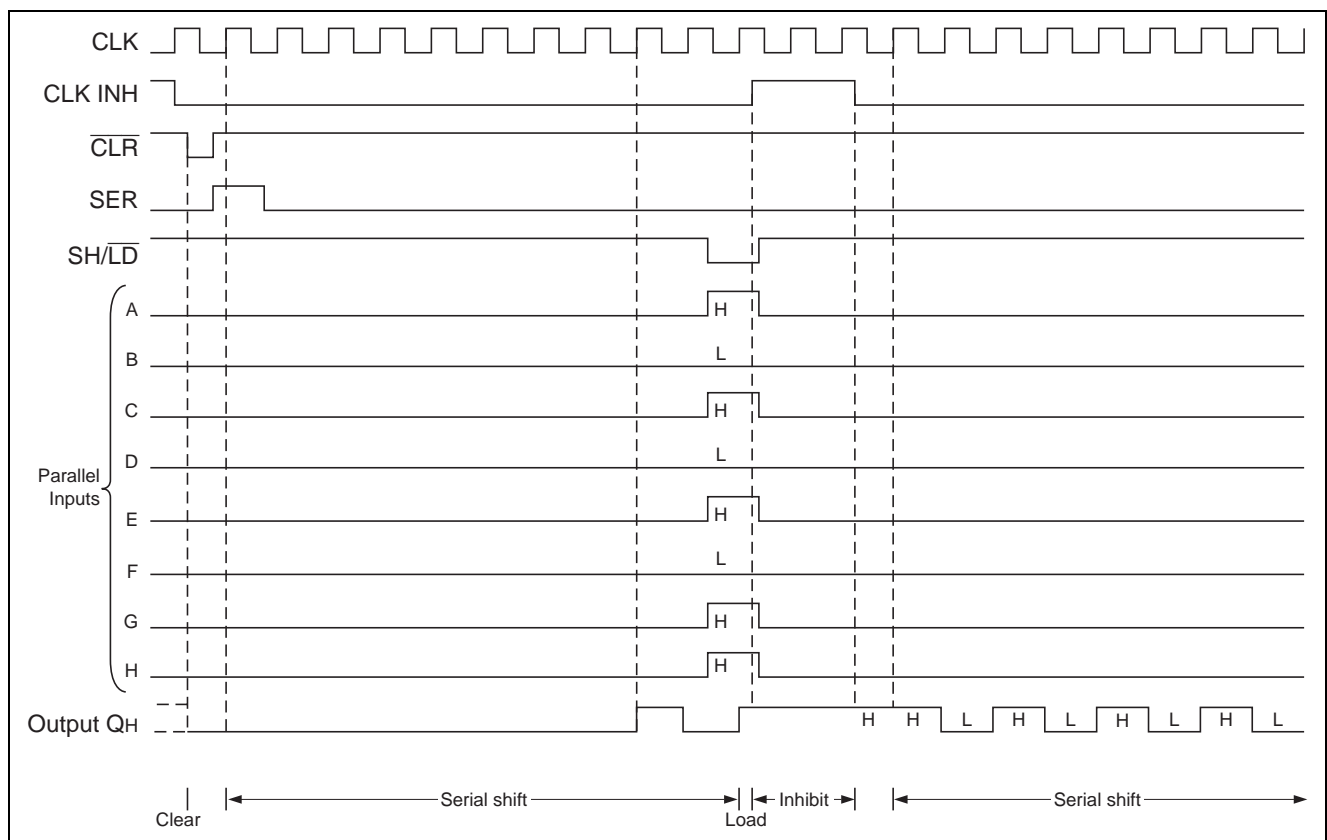
Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	$V_{CC}$	2.0	5.5	V	
Input voltage range	$V_I$	0	5.5	V	
Output voltage range	$V_O$	0	$V_{CC}$	V	H or L
Output current	$I_{OH}$	—	-50	$\mu\text{A}$	$V_{CC} = 2.0\text{ V}$
		—	-2	mA	$V_{CC} = 2.3$ to $2.7\text{ V}$
		—	-6		$V_{CC} = 3.0$ to $3.6\text{ V}$
		—	-12		$V_{CC} = 4.5$ to $5.5\text{ V}$
	$I_{OL}$	—	50	$\mu\text{A}$	$V_{CC} = 2.0\text{ V}$
		—	2	mA	$V_{CC} = 2.3$ to $2.7\text{ V}$
		—	6		$V_{CC} = 3.0$ to $3.6\text{ V}$
		—	12		$V_{CC} = 4.5$ to $5.5\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3$ to $2.7\text{ V}$
		0	100		$V_{CC} = 3.0$ to $3.6\text{ V}$
		0	20		$V_{CC} = 4.5$ to $5.5\text{ V}$
Operating free-air temperature	$T_a$	-40	85	$^\circ\text{C}$	

Note: Unused or floating inputs must be held high or low.

## Logic Diagram



## Timing Diagram



## DC Electrical Characteristics

Ta = -40 to 85°C

Item	Symbol	V <sub>CC</sub> (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>	2.0	1.5	—	—	V	
		2.3 to 2.7	V <sub>CC</sub> × 0.7	—	—		
		3.0 to 3.6	V <sub>CC</sub> × 0.7	—	—		
		4.5 to 5.5	V <sub>CC</sub> × 0.7	—	—		
	V <sub>IL</sub>	2.0	—	—	0.5		
		2.3 to 2.7	—	—	V <sub>CC</sub> × 0.3		
		3.0 to 3.6	—	—	V <sub>CC</sub> × 0.3		
		4.5 to 5.5	—	—	V <sub>CC</sub> × 0.3		
Output voltage	V <sub>OH</sub>	Min to Max	V <sub>CC</sub> - 0.1	—	—	V	I <sub>OL</sub> = -50 μA
		2.3	2.0	—	—		I <sub>OL</sub> = -2 mA
		3.0	2.48	—	—		I <sub>OL</sub> = -6 mA
		4.5	3.8	—	—		I <sub>OL</sub> = -12 mA
	V <sub>OL</sub>	Min to Max	—	—	0.1		I <sub>OL</sub> = 50 μA
		2.3	—	—	0.4		I <sub>OL</sub> = 2 mA
		3.0	—	—	0.44		I <sub>OL</sub> = 6 mA
		4.5	—	—	0.55		I <sub>OL</sub> = 12 mA
Input current	I <sub>IN</sub>	0 to 5.5	—	—	±1	μA	V <sub>I</sub> = 5.5 V or GND
Quiescent supply current	I <sub>CC</sub>	5.5	—	—	20	μA	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0
Output leakage current	I <sub>OFF</sub>	0	—	—	5	μA	V <sub>I</sub> or V <sub>O</sub> = 0 V to 5.5 V
Input capacitance	C <sub>IN</sub>	3.3	—	1.7	—	pF	V <sub>I</sub> = V <sub>CC</sub> or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

## Switching Characteristics

$$V_{CC} = 2.5 \pm 0.2 \text{ V}$$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f <sub>max</sub>	50	80	—	45	—	MHz	C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		
Propagation delay time	t <sub>PLH</sub> /t <sub>PHL</sub>	—	12.2	19.8	1.0	22.0	ns	C <sub>L</sub> = 15 pF	CLK	Q <sub>H</sub>
		—	15.3	23.3	1.0	26.0		C <sub>L</sub> = 50 pF		
	t <sub>PHL</sub>	—	10.8	16.0	1.0	18.0		C <sub>L</sub> = 15 pF	CLR	
		—	14.2	19.5	1.0	22.0		C <sub>L</sub> = 50 pF		
Setup time	t <sub>su</sub>	6.0	—	—	7.0	—	ns		CLR inactive before CLK ↑	
		7.0	—	—	7.0	—			CLK INH before CLK ↑	
		6.5	—	—	8.5	—			Data before CLK ↑	
		7.0	—	—	8.5	—			SH/LD high before CLK ↑	
		8.5	—	—	9.5	—			SER before CLK ↑	
Hold time	t <sub>h</sub>	-0.5	—	—	0.0	—	ns		PAR data after SH/LD ↑	
		-0.5	—	—	0.0	—			SER data after CLK ↑	
		-0.5	—	—	0.0	—			SH/LD high after CLK ↑	
Pulse width	t <sub>w</sub>	8.0	—	—	9.0	—	ns		CLR low	
		8.5	—	—	9.0	—			CLK H or L	

$$V_{CC} = 3.3 \pm 0.3 \text{ V}$$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f <sub>max</sub>	65	115	—	55	—	MHz	C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		
Propagation delay time	t <sub>PLH</sub> /t <sub>PHL</sub>	—	8.6	15.4	1.0	18.0	ns	C <sub>L</sub> = 15 pF	CLK	Q <sub>H</sub>
		—	10.9	18.9	1.0	21.5		C <sub>L</sub> = 50 pF		
	t <sub>PHL</sub>	—	7.9	12.5	1.0	15.0		C <sub>L</sub> = 15 pF	CLR	
		—	10.4	16.3	1.0	18.5		C <sub>L</sub> = 50 pF		
Setup time	t <sub>su</sub>	4.0	—	—	4.0	—	ns		CLR inactive before CLK ↑	
		5.0	—	—	5.0	—			CLK INH before CLK ↑	
		5.0	—	—	6.0	—			Data before CLK ↑	
		5.0	—	—	6.0	—			SH/LD high before CLK ↑	
		5.0	—	—	6.0	—			SER before CLK ↑	
Hold time	t <sub>h</sub>	0.0	—	—	0.0	—	ns		PAR data after SH/LD ↑	
		0.0	—	—	0.0	—			SER data after CLK ↑	
		0.0	—	—	0.0	—			SH/LD high after CLK ↑	
Pulse width	t <sub>w</sub>	6.0	—	—	7.0	—	ns		CLR low	
		6.0	—	—	7.0	—			CLK H or L	

## Switching Characteristics (cont)

$V_{CC} = 5.0 \pm 0.5 \text{ V}$

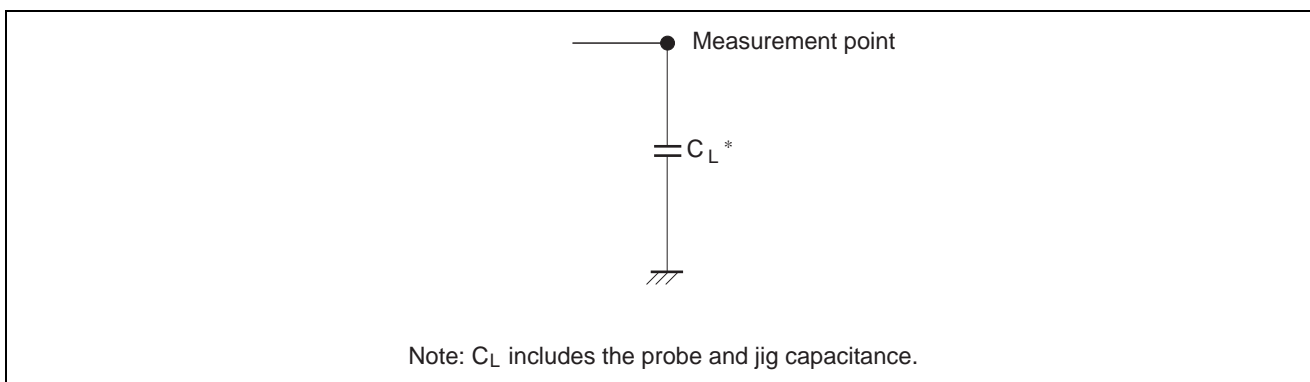
Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f <sub>max</sub>	110	165	—	90	—	MHz	C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		
Propagation delay time	t <sub>PLH</sub> /t <sub>PHL</sub>	—	6.0	9.9	1.0	11.5	ns	C <sub>L</sub> = 15 pF	CLK	Q <sub>H</sub>
		—	7.7	11.9	1.0	13.5		C <sub>L</sub> = 50 pF		
	t <sub>PHL</sub>	—	5.4	8.6	1.0	10.0		C <sub>L</sub> = 15 pF	CLR	
		—	6.9	10.6	1.0	12.0		C <sub>L</sub> = 50 pF		
Setup time	t <sub>su</sub>	3.5	—	—	3.5	—	ns		CLR inactive before CLK ↑	
		3.5	—	—	3.5	—			CLK INH before CLK ↑	
		4.5	—	—	4.5	—			Data before CLK ↑	
		4.0	—	—	4.0	—			SH/LD high before CLK ↑	
		4.0	—	—	4.0	—			SER before CLK ↑	
Hold time	t <sub>h</sub>	1.0	—	—	1.0	—	ns		PAR data after SH/LD ↑	
		1.0	—	—	1.0	—			SER data after CLK ↑	
		1.0	—	—	1.0	—			SH/LD high after CLK ↑	
Pulse width	t <sub>w</sub>	5.0	—	—	5.0	—	ns		CLR low	
		4.0	—	—	4.0	—			CLK H or L	

## Operating Characteristics

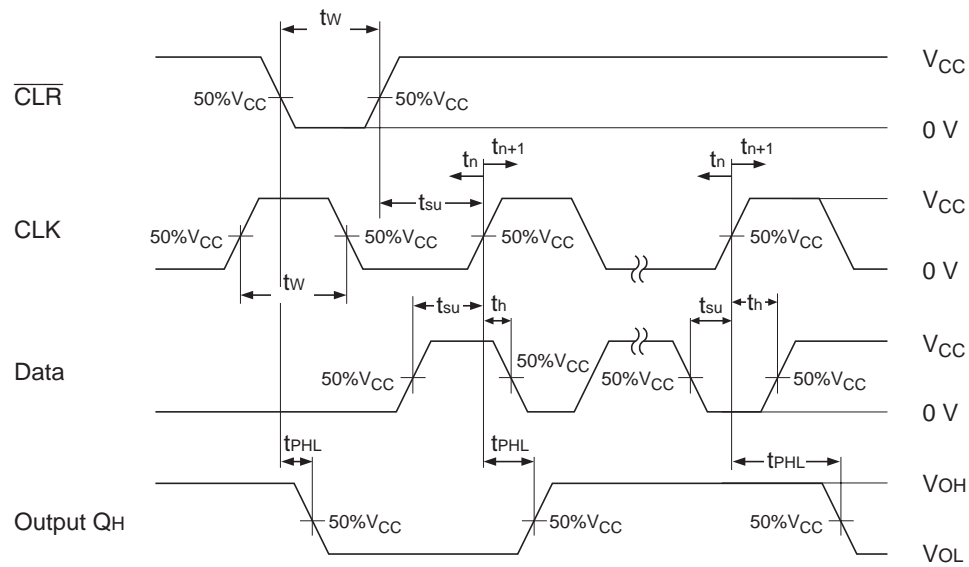
C<sub>L</sub> = 50 pF

Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C <sub>PD</sub>	3.3	—	36.1	—	pF	f = 10 MHz
		5.0	—	37.5	—		

## Test Circuit

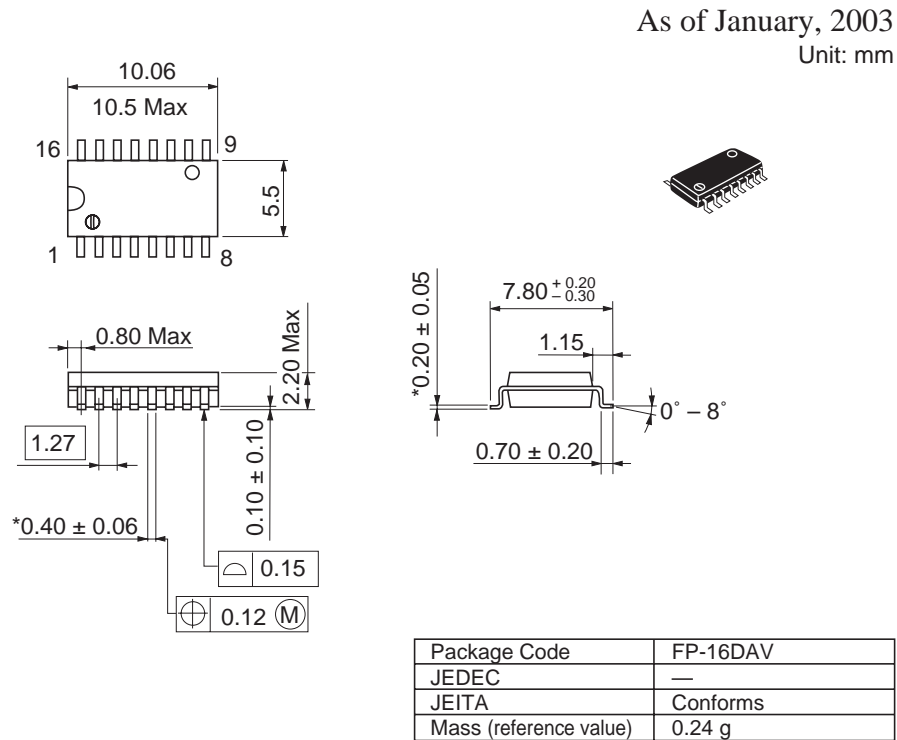


Waveforms



Notes: 1. Input waveform:  $PRR \leq 1 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$   
2. The output are measured one at a time with one transition per measurement.

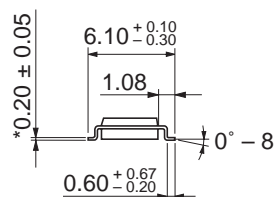
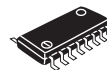
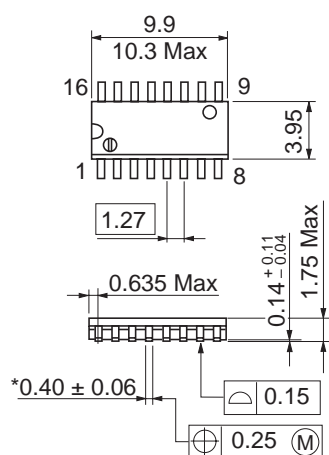
Package Dimensions





As of January, 2003

Unit: mm

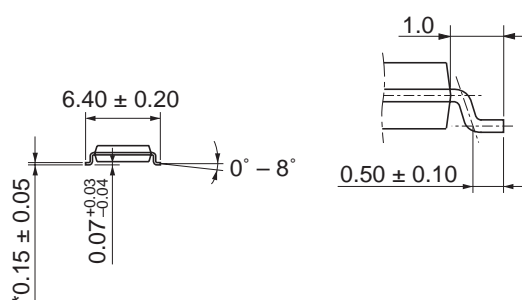
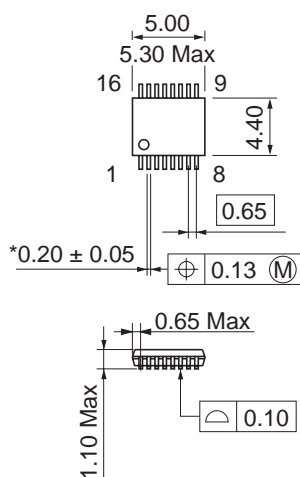


\*Ni/Pd/Au plating

Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

As of January, 2003

Unit: mm



\*Ni/Pd/Au plating

Package Code	TTP-16DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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