TEXAS INSTRUMENTS

TL1451AEVM-166

3.3-V/1.8-V Dual Buck EVM Using the TL1451A

User's Guide

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Power Management Products

SLVU043

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Preface

About This Manual

This user's guide describes the TL1451AEVM–166 buck converter evaluation module.

How to Use This Manual

- ❑ Chapter 1—Introduction
- ❑ Chapter 2—Schematic
- ❑ Chapter 3—Test Results
- ❑ Chapter 4—Bill of Materials

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

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This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

- ❑ TL1451A datasheet (literature number SLVS024)
- ❑ TL5001C application report (literature number SLVA034)

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Figures

Tables

Chapter 1

Introduction

This user's guide describes the TL1451AEVM-166 buck converter evaluation module (SLVP166). The SLVP166 provides a convenient method for evaluating the performance of a dual buck converter using the TL1451A PWM regulator controller. A complete designed and tested power supply is presented. The power supply is a dual step-down dc-dc converter that can deliver up to 1.5 A of continuous output current at 3.3-V output and up to 1 A of continuous output current at 1.8-V output with an input range of 4.5 V to 5.5 V.

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1.1 Performance Specification Summary

This section summarizes the performance specifications of the SLVP166 converter. Table 1–1 gives the performance specifications of the converters.

Table 1–1. Performance Specification Summary

Specifications	Test Conditions		Min	Typ	Max	Unit
Input voltage range			4.5		5.5	V
Output voltage, set point	I_O1 = 0 A		3.178	3.31	3.442	V
	I_O2 = 0 A		1.730	1.802	1.874	V
Line regulation	V_O1 with V_I = 4.5 V to 5.5 V, I_O1 = 1.5 A			0.01%	0.02%	
	V_O2 with V_I = 4.5 V to 5.5 V, I_O2 = 1 A			0.01%	0.02%	
Load regulation	V_O1 with V_I =5 V, I_O1 = 0 – 1.5 A			0.5%	0.7%	
	V_O2 with V_I =5 V, I_O1 = 0 – 1 A			0.4%	0.6%	
Transient response	I_O1 = 150 mA to 1.5 A, $T_{(rise)}$ = 30 µs			10		mV_{PK}
				150		µs
	I_O2 = 100 mA to 1 A, $T_{(rise)}$ = 30 µs			10		mV_{PK}
				150		µs
Output current range	V_I = 4.5 V to 5.5 V	I_O1	0		1.5	A
		I_O2	0		1	
Output ripple	V_I = 5 V, I_O1 = 1.5 A			30	60	mV_{PP}
	V_I = 5 V, I_O2 = 1 A			30	50	
Soft-start rise time	V_I = 5 V, I_O1 = 1.5 A, I_O2 = 1 A			0.6	1	ms
Operating frequency	V_I = 5 V, I_O1 = 1.5 A, I_O2 = 1 A		255	300	345	kHz
Efficiency, full load	V_I = 5 V, I_O1 = 1.5 A, I_O2 = 1 A		80%	85%		

Chapter 2

Schematic

This chapter contains the schematic diagram for the SLVP166 EVM.

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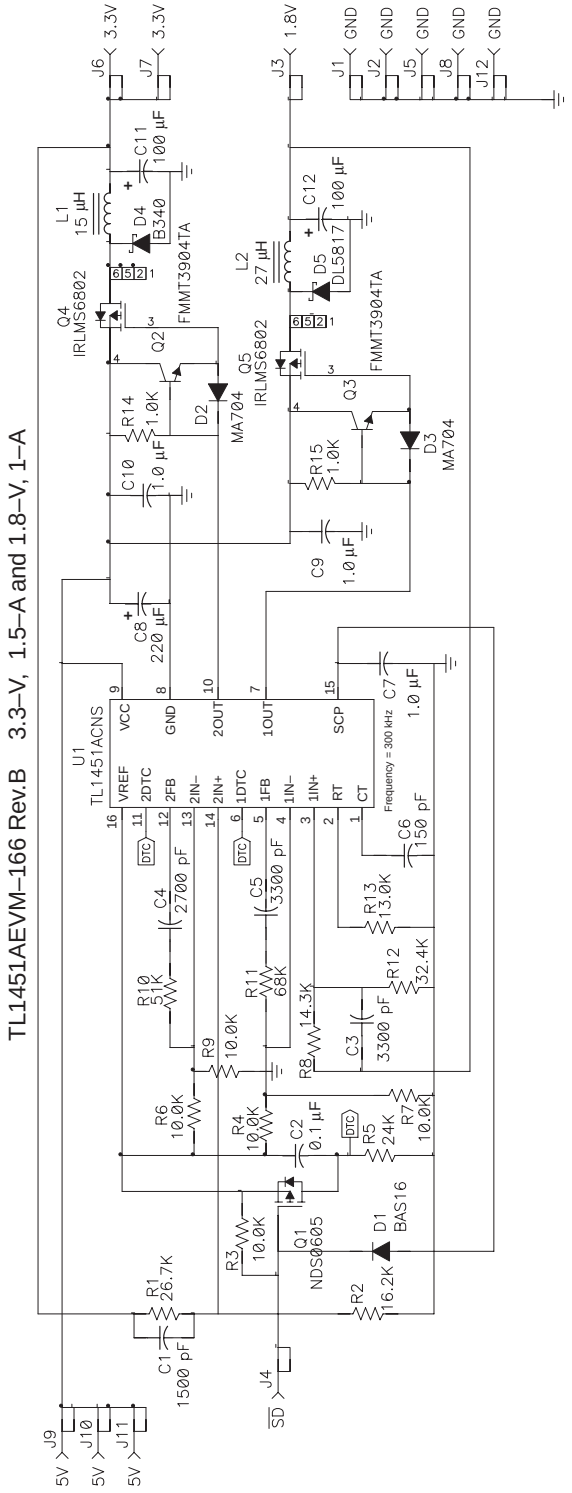
2.1 Schematic

Figure 2–1. SLVP166 Schematic Diagram



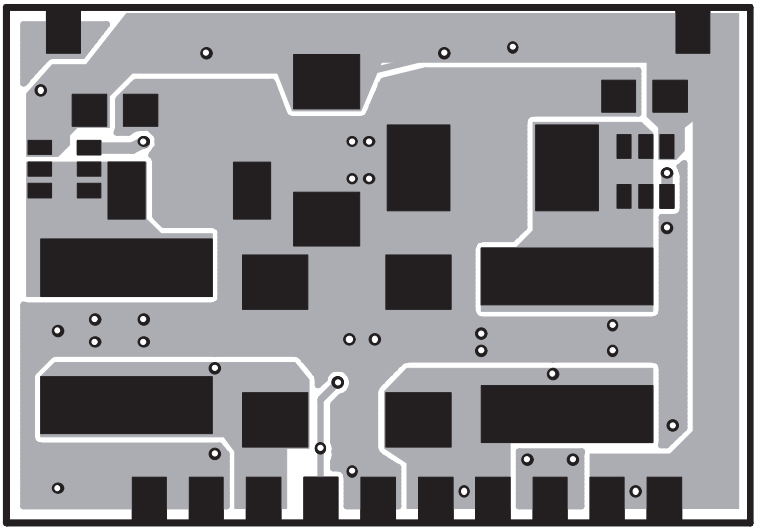
Notes: 1) A low signal on J4 will shut down the power supply.

2) When a change in the output voltage is required, R2 and/or R12 should be changed instead of R1 and or R8 due to the compensation networks.

2.2 Board Layout

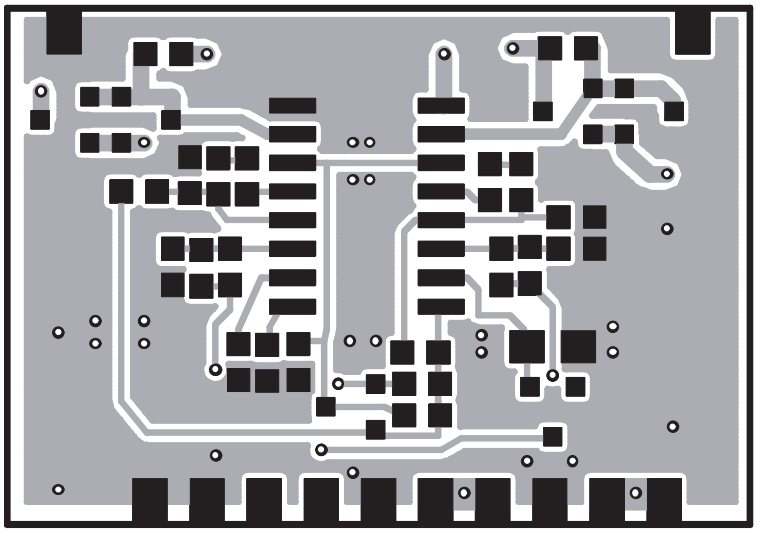
The power supply module consists of one PWB. Figure 2–2 shows the top layer (front view) of the SLVP166 PWB. Figure 2–3 shows the bottom layer (top view) of the SLVP166 PWB. Figure 2–4 shows the SLVP166 top and bottom assembly views.

Figure 2–2. SLVP166 Board Layout Top Layer



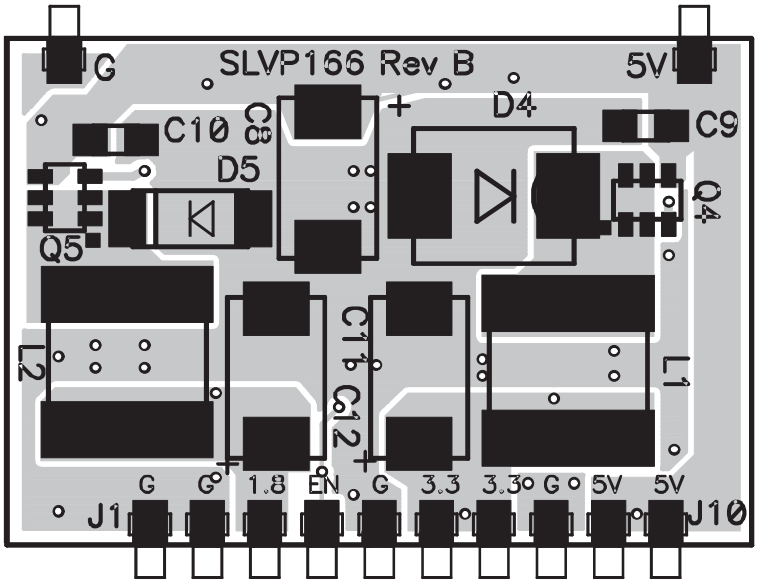
Top Layer

Figure 2–3. SLVP166 Board Layout Bottom Layer

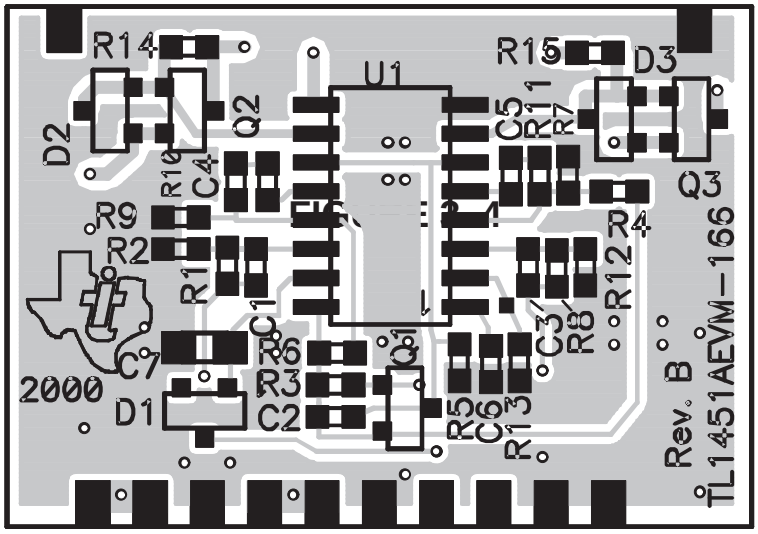


Bottom Layer (Top View)

Figure 2–4. SLVP166 Top and Bottom Assembly Views



Top Assembly



Bottom Assembly (Bottom View)

Chapter 3

Test Results

This chapter shows the test setups used, and the test results obtained, in designing the SLVP166 EVM.

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3.1 Test Summary

The detailed test results are presented in Figures 3–2 to 3–6 for the SLVP166. The following are summarized results.

3.1.1 Static Line and Load Regulation

The load regulation from no load to full load current does not exceed 0.6%. The line regulation is less than 0.015% for the input voltage range from 4.5 V to 5.5 V. Line and load regulation curves are shown in Figures 3–1 and 3–2. The set point tolerance is approximately 4%.

Figure 3–1. SLVP166 Measured Line Regulation

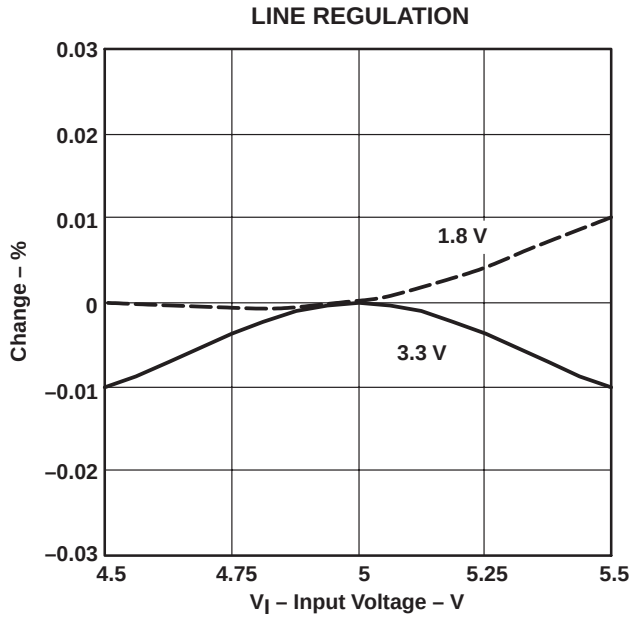
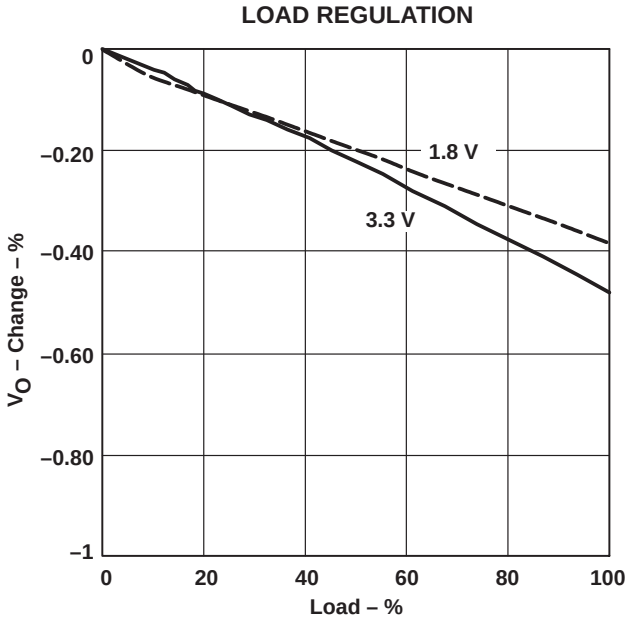


Figure 3–2. SLVP166 Measured Load Regulation



3.1.2 Output Voltage Ripple

The output voltage peak to peak ripple is approximately 30 mV on both outputs. This is a typical value but the converter can be optimized for lower ripple applications.

Figure 3–3. 3.3-V Ripple Voltage

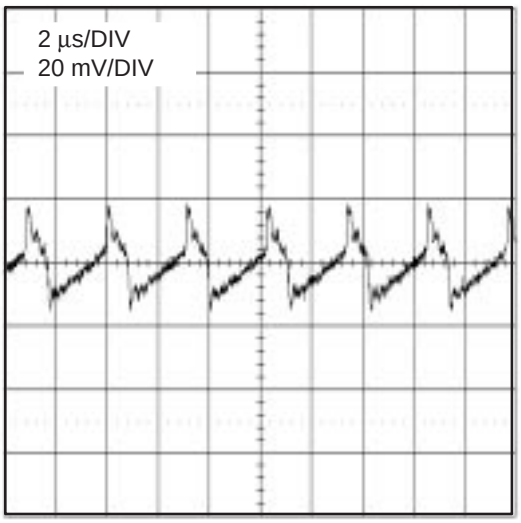
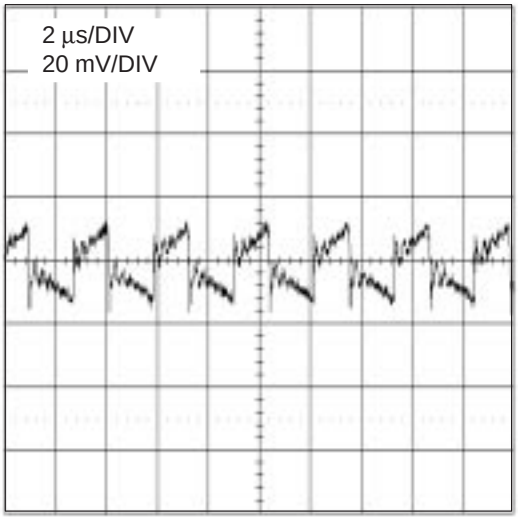


Figure 3–4. 1.8-V Ripple Voltage



3.1.3 Efficiency and Power Losses

Efficiency and power losses for 5-V input voltage and maximum output current on both outputs gives an efficiency of 85.6% resulting in an onboard power loss of 1.12 W maximum.

Figure 3–5. SLVP166 Measured Load Regulation

Low power loss in each component decreases their temperature rise and improves long term reliability. The EVM does not require forced air cooling at room temperature with good margin.

3.1.4 Output Start-Up and Overshoot

Output voltage rise time does not depend on the load current and ramps up in a linear fashion. There is no discernable overshoot in the waveform. In this application, output voltage rise time is set to approximately 600 μs with an external capacitor.

3.1.5 Transient Response

Although this controller was not designed for high-speed transient response, it does do a good job at low power levels such as with this design. A transient load that varied from 10% to 100% of full load was applied to each output of the EVM. Results are shown in Figure 3–6 and Figure 3–7.

Figure 3–6. 3.3-V Transient Response

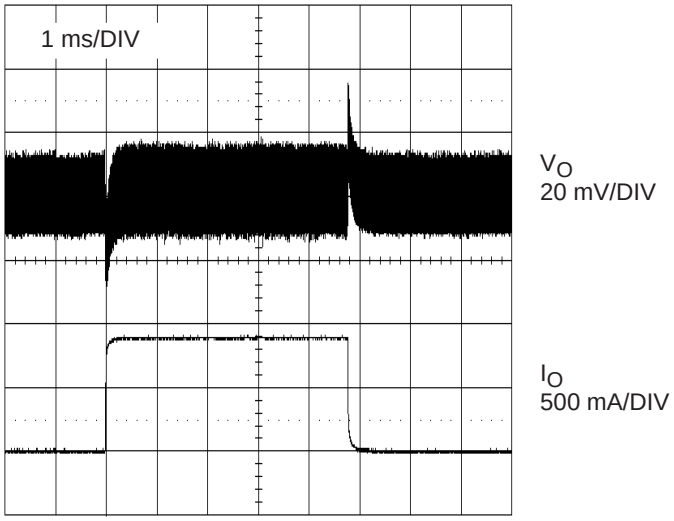
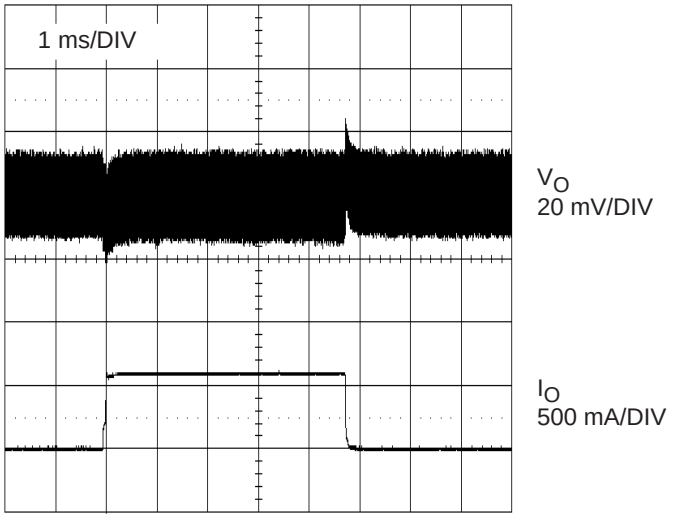


Figure 3–7. 1.8-V Transient Response



3.1.6 Frequency Variation

The onboard oscillator is set by two external components, R13 and C6. The nominal frequency is set to 300 kHz but has a tolerance of ±15%.

3.1.7 Conclusion

The test results of the SLVP166 EVM demonstrate the advantages of the TL1451A controller to meet dual-output supply requirements to power supplies. The power system designer has a good solution to optimize the system for his particular application. Detailed information on how to design a dc-dc buck converter is available in the application report, *Designing with the TL5001C PWM Controller, SLVA034.*

3.2 Test Setup

Follow these steps for initial power up of the SLVP166:

Step 1: Connect an electronic load from 1.8 V to G (J3 to J2) adjusted to draw approximately 1 A at 1.8 V. Connect an electronic load from 3.3 V to G (J6 to J8) adjusted to draw approximately 1.5 A at 3.3 V. The exact current is not critical; any nominal current is sufficient. A fixed resistor can also be used in place of the electronic loads. The output current drawn by the resistors is $I_L = \frac{V_O}{R}$ where R is the value of the load resistor. The resistor power rating, P_R should be at least $\frac{2 \times V_O^2}{R}$ watts.

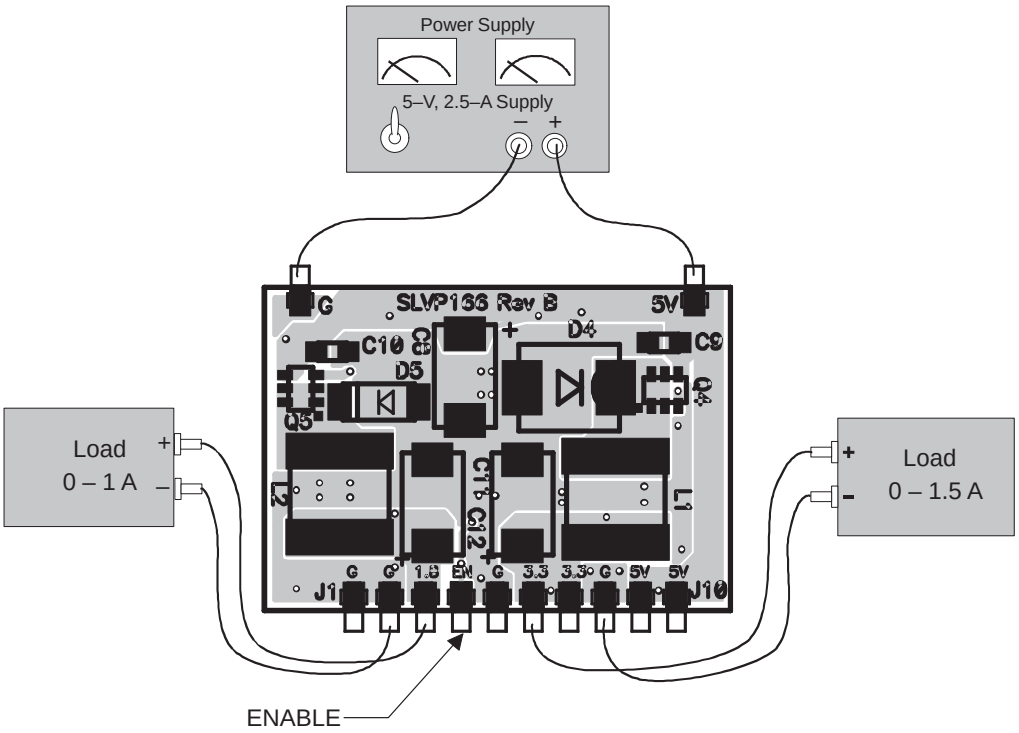
Step 2: Connect a 5-V lab power supply to the 5-V input (J11 referenced to GND, J12) of the SLVP166. Adjust the current limit to approximately 2 A.

Step 3: Turn on the 5-V power supply and ramp the input voltage up to 5 V.

Step 4: Verify that the SLVP166 output voltages (measured at the module output pins) are within the output voltage tolerances.

Step 5: Refer to the test results for selected typical waveforms and operating conditions for verification of proper module operation.

Figure 3–8. SLVP166 Test Setup



Chapter 4

Bill of Materials

This chapter contains the bill of materials for the SLVP166 EVM.

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4.1 Bill of Materials

Table 4–1 lists materials required for the SLVP166 EVM.

Table 4–1. SLVP166 Bill of Materials

Qty	RefDes	Part Number	Description	MFR	Size
1	C1	GRM39X7R152K50	Capacitor, ceramic, 1500 pF, 50 V, 10%, X7R	Murata	603
1	C2	GRM39X7R104K16	Capacitor, ceramic, 0.1 μF, 16 V, 10% X7R	Murata	603
2	C3,C5	GRM39X7R332K50	Capacitor, ceramic, 3300 pF, 50 V, 10%, X7R	Murata	603
1	C4	GRM39X7R272K50	Capacitor, ceramic, 2700 pF, 50 V, 10%, X7R	Murata	603
1	C6	GRM39COG151J50	Capacitor, ceramic, 150 pF, 50 V, 5%, COG	Murata	603
3	C7,C9, C10	ECJ-JVF1C105Z	Capacitor, ceramic, 1 μF, 16 V, +80%–20%, Y5V	Panasonic	805
1	C8	10TPB220M	Capacitor, POSCAP, 220 μF, 10 V, 40-mΩ, 20%	Sanyo	D Case
2	C11,C12	TPSD107M010R100	Capacitor, Tantalum, 100 μF, 10 V, 10-mΩ, 20%	AVX	D Case
1	D1	BAS16	Diode, switching, 10-mA, 75-V, 350-mW	Vishay-Liteon	TO-236
2	D2,D3	MA704	Diode, Schottky, 30-mA, 15-V	Panasonic	TO-236
1	D4	B340	Diode, Schottky, 3-A, 40-V	Vishay-Liteon	SMC
1	D5	DL5817	Diode, Schottky, 1-A, 20-V	Vishay-Liteon	DL41
12	J1-J12	CA26DA-D36W-0FC	Clip, surface-mount, 0.040 board, 0.090 stand-off	NAS Interplex	
1	L1	CTGS75-150K	Inductor, SMT, 15 μH, 1.8-A, 90-mΩ	Central Tech	CD75
1	L2	CTGS75-270K	Inductor, SMT, 27 μH, 1.3-A, 120-mΩ	Central Tech	CD75
1	R1	STD	Resistor, chip, 26.7 kΩ, 1/16 W, 1%		603
1	R2	STD	Resistor, chip, 16.2 kΩ, 1/16 W, 1%		603
5	R3,R4, R6,R7, R9	STD	Resistor, chip, 10.0 kΩ, 1/16 W, 1%		603
1	R5	STD	Resistor, chip 24 kΩ, 1/16 W, 5%		603
1	R8	STD	Resistor, chip, 14.3 kΩ, 1/16 W, 1%		603
1	R10	STD	Resistor, chip, 51 kΩ, 1/16 W, 5%		603
1	R11	STD	Resistor, chip, 68 kΩ, 1/16 W, 5%		603
1	R12	STD	Resistor, chip, 32.4 kΩ, 1/16 W, 1%		603
1	R13	STD	Resistor, chip, 13.0 kΩ, 1/16 W, 1%		603
2	R14,R15	STD	Resistor, chip, 1.0 kΩ, 1/16 W, 5%		603

Table 4–1. SLVP166 Bill of Materials (Continued)

Qty	RefDes	Part Number	Description	MFR	Size
1	Q1	NDS0605	MOSFET, P-ch, 60-V, 180-mA, 5 Ω	Fairchild	SOT-23
2	Q2, Q3	FMMT3904TA	Bipolar, NPN, 40-V, 200-mA, 300-mW	Zetex	SOT-23
w	Q4,Q5	IRLMS6802	MOSFET, P-ch, 20-V, 5.6-A, 50-mΩ	IR	MICRO6
1	U1	TL1451ACNS	IC, Dual channel PWM controller with open-collector outputs	TI	SOP-16
1	NA	SLVP166	PCB, TL1451AEVM-166B, 2 layers, 2 ounce copper		1.30 × 0.900