

## Dual Channel USB3.0 Redriver/Equalizer

Check for Samples: [SN65LVPE502CP](#)

### FEATURES

- Single Lane USB 3.0 Equalizer/Redriver
- Selectable Equalization, De-Emphasis and Output Swing Control
- Integrated Termination
- Hot-Plug Capable
- Low Active Power (U0 state)
  - 315 mW (TYP),  $V_{CC} = 3.3V$
- USB 3.0 Low Power Support
  - 7 mW (TYP) When no Connection Detected
  - 70 mW (TYP) When Link in U2/U3 Mode
- Excellent Jitter and Loss Compensation Capability:
  - >40" of Total 4 mil Stripline on FR4
- Small Foot Print – 24 Pin (4mm x 4mm) QFN Package

- High Protection Against ESD Transient
  - HBM: 5,000 V
  - CDM: 1,500 V
  - MM: 200 V

### APPLICATIONS

- Notebooks, Desktops, Docking Stations, Active Cable, Backplane and Active Cable

### DESCRIPTION

The SN65LVPE502CP is a dual channel, single lane USB 3.0 redriver and signal conditioner supporting data rates of 5.0Gbps. The device complies with USB 3.0 spec revision 1.0, supporting electrical idle condition and low frequency periodic signals (LFPS) for USB 3.0 power management modes.

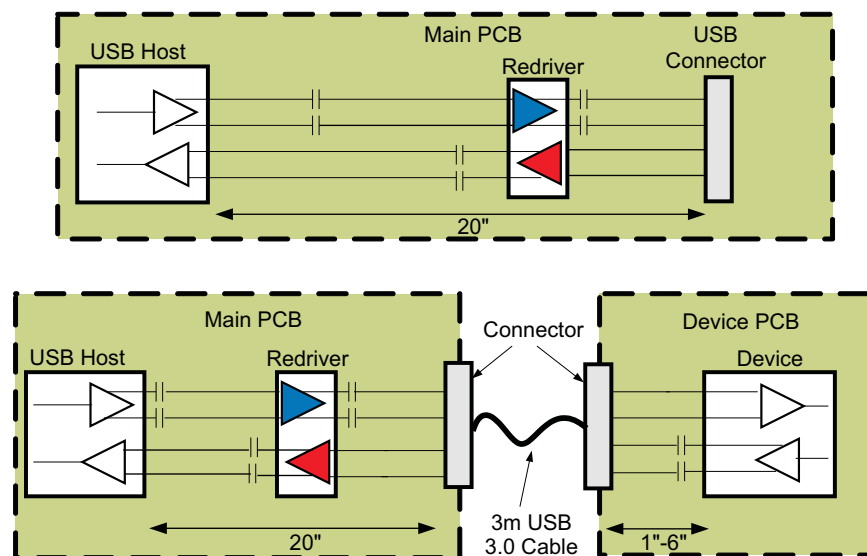


Figure 1. Typical Application



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

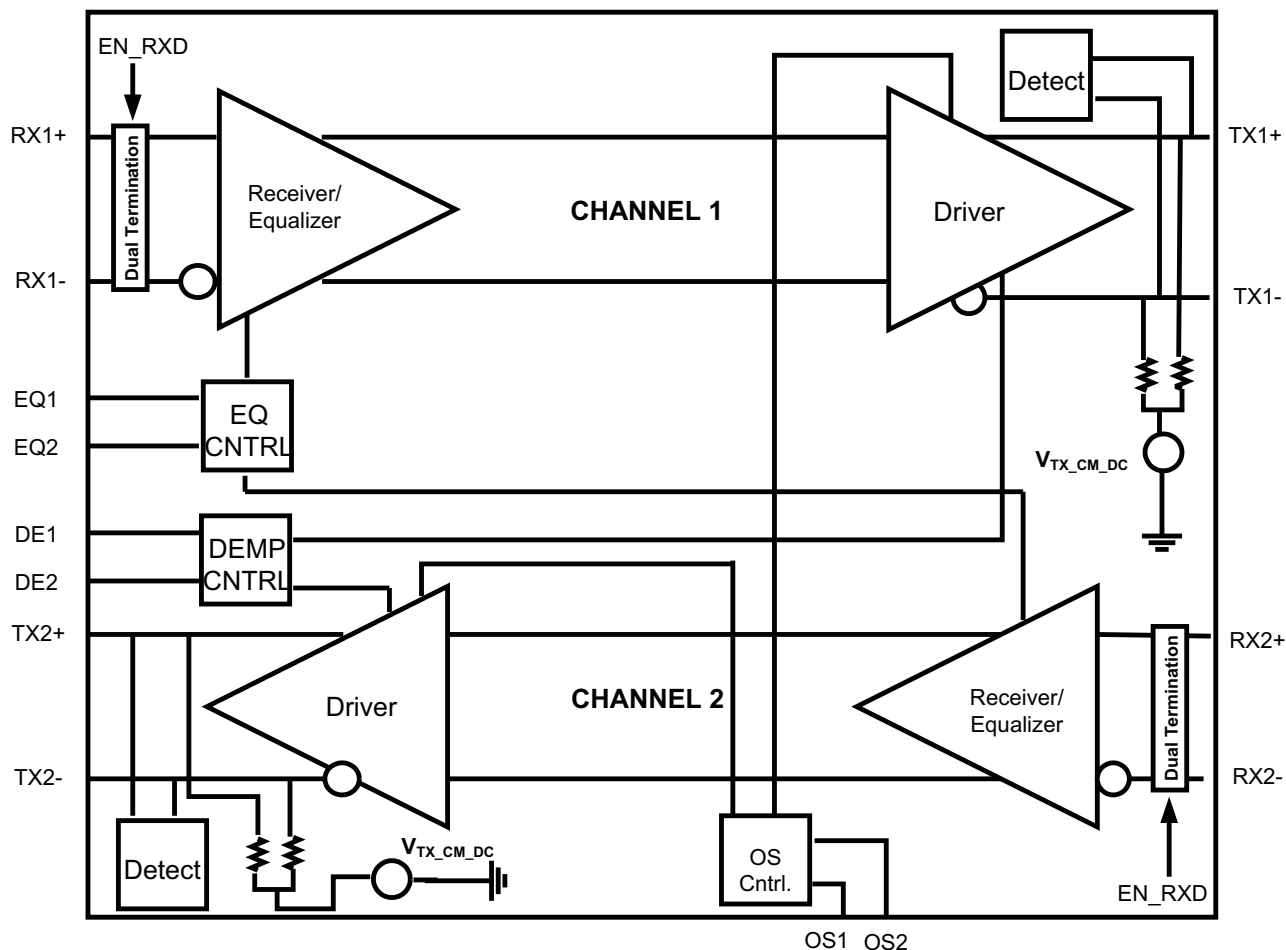


Figure 2. Data Flow Block Diagram

### ORDERING INFORMATION<sup>(1)</sup>

PART NUMBER	PART MARKING	PACKAGE
SN65LVPE502CPRGER	502CP	24-pin RGE Reel (Large)
SN65LVPE502CPRGET	502CP	24-pin RGE Reel (Small)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range <sup>(2)</sup>	V <sub>CC</sub>	–0.5	4	V
Voltage range	Differential I/O	–0.5	4	V
	Control I/O	–0.5	V <sub>CC</sub> + 0.5	V
Electrostatic discharge	Human body model <sup>(3)</sup>	±5000		V
	Charged-device model <sup>(4)</sup>	±1500		V
	Machine model <sup>(5)</sup>	±200		V
Continuous power dissipation		See Thermal Table		

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
- (5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		SN65LVPE502CP	UNITS
		RGE PACKAGE	
		24 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	46	°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance	42	
$\theta_{JB}$	Junction-to-board thermal resistance	13	
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance	4	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## THERMAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX <sup>(1)</sup>	UNIT
P <sub>D</sub>	Device power dissipation RSVD, EN_RXD, EQ cntrl pins = NC, K28.5 pattern at 5 Gbps, V <sub>ID</sub> = 1000mV <sub>p-p</sub>		330	450	mW
P <sub>Slp</sub>	Device power dissipation in sleep mode EN_RXD= GND		0.3	1	mW

- (1) The maximum rating is simulated under 3.6V VCC.

### Device Power

The SN65LVPE502CP is designed to operate from a single 3.3V supply.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V <sub>CC</sub>	Supply voltage		3	3.3	3.6	V
C <sub>COUPLING</sub>	AC Coupling capacitor		75		200	nF
	Operating free-air temperature		0		85	°C
<b>DEVICE PARAMETERS</b>						
I <sub>CC</sub>	Supply current	EN_RXD, RSVD, EQ cntrl = NC, K28.5 pattern at 5 Gbps, VID = 1000mVp-p		100	120	mA
I <sub>CC</sub> <sub>Rx.Detect</sub>		In Rx.Detect mode		2	5	
I <sub>CC</sub> <sub>sleep</sub>		EN_RXD = GND		0.01	0.1	
I <sub>CC</sub> <sub>U2-U3</sub>		Link in USB low power state		21		
	Maximum data rate				5	Gbps
t <sub>ENB</sub>	Device enable time	Sleep mode exit time EN_RXD L → H With Rx termination present			100	μs
t <sub>DIS</sub>	Device disable time	Sleep mode entry time EN_RXD H → L			2	μs
T <sub>RX.DETECT</sub>	Rx.Detect start event	Power-up time			100	μs
<b>CONTROL LOGIC</b>						
V <sub>IH</sub>	High level input voltage		1.4		V <sub>CC</sub>	V
V <sub>IL</sub>	Low level input voltage		–0.3		0.5	V
V <sub>HYS</sub>	Input hysteresis			150		mV
I <sub>IH</sub>	High level input current	OSx, EQx, DEx = V <sub>CC</sub>			30	μA
		EN_RXD = V <sub>CC</sub>			1	
		RSVD = V <sub>CC</sub>			30	
I <sub>IL</sub>	Low level input current	OSx, EQx, DEx = GND	–30			μA
		EN_RXD = GND	–30			
		RSVD = GND	–1			

## ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER AC/DC						
V <sub>in_diff_P-P</sub>	RX1, RX2 input voltage swing	AC coupled differential RX peak to peak signal	100		1200	mVp-p
V <sub>CM_RX</sub>	RX1, RX2 common mode voltage			3.3		V
V <sub>inCOM_P</sub>	RX1, RX2 AC peak common mode voltage	Measured at Rx pins with termination enabled			150	mVP
Z <sub>DC_RX</sub>	DC common mode impedance		18	26	30	Ω
Z <sub>diff_RX</sub>	DC differential input impedance		72	80	120	Ω
Z <sub>RX_High_IMP+</sub>	DC Input high impedance	Device in sleep mode Rx termination not powered measured with respect to GND over 500mV max	50	85		kΩ
V <sub>RX-LFPS-DETPp</sub>	Low voltage periodic signaling (LFPS) detect threshold	Measured at receiver pin, below minimum output is squelched, above max input signal is passed to output	100		300	mVpp
RL <sub>RX-DIFF</sub>	Differential return loss	50 MHz – 1.25 GHz	10	11		dB
		1.25 GH – 2.5 GHz	6	7		
RL <sub>RX-CM</sub>	Common mode return loss	50 MHz– 2.5 GHz	11	13		dB
TRANSMITTER AC/DC						
V <sub>TxDIFF_TB_P-P</sub>	Differential peak-to-peak output voltage (VID = 800, 1200 mVpp, 5Gbps)	R <sub>L</sub> = 100 Ω ±1%, DEx, OSx = NC, <b>Transition Bit</b>	800	1042	1200	mV
		R <sub>L</sub> = 100 Ω ±1%, DEx = NC, OSx = GND <b>Transition Bit</b>		908		
		R <sub>L</sub> = 100 Ω ±1%, DEx = NC, OSx = VCC <b>Transition Bit</b>		1127		
V <sub>TxDIFF NTB_P-P</sub>		R <sub>L</sub> = 100 Ω ±1%, DEx=NC, OSx = 0,1,NC <b>Non-Transition Bit</b>		1042		mV
		R <sub>L</sub> = 100 Ω ±1%, DEx=0 OSx = 0,1,NC <b>Non-Transition Bit</b>		661		
		R <sub>L</sub> = 100 Ω ±1%, DEx=1 OSx = 0,1,NC <b>Non-Transition Bit</b>		507		
DE	De-emphasis level OS1,2 = NC (for OS1, 2 = 1 and 0 see <a href="#">Table 2</a> )	DE1/DE2 = NC		0		dB
		DE1/DE2 = 0	–3.0	–3.5	–4.0	
		DE1/DE2 = 1		–6.0		
T <sub>DE</sub>	De-emphasis width			0.85		UI
Z <sub>diff_TX</sub>	DC differential impedance		72	90	120	Ω
Z <sub>CM_TX</sub>	DC common mode impedance	Measured w.r.t to AC ground over 0-500mV	18	23	30	Ω
RL <sub>diff_TX</sub>	Differential return loss	f = 50 MHz – 1.25 GHz	9	10		dB
		f = 1.25 GHz – 2.5 GHz	6	7		
RL <sub>CM_TX</sub>	Common mode return loss	f = 50 MHz – 2.5 GHz	11	12		dB
I <sub>TX_SC</sub>	TX short circuit current	TX± shorted to GND			60	mA
V <sub>TX_CM_DC</sub>	Transmitter DC common-mode voltage		2.0	2.6	3.0	V
V <sub>TX_CM_AC_Active</sub>	TX AC common mode voltage active			30	100	mVpp
V <sub>Tx_idle_diff-AC-pp</sub>	Electrical idle differential peak to peak output voltage	HPF to remove DC	0		10	mVpp
V <sub>TX_CM_DeltaU1-U0</sub>	Absolute delta of DC CM voltage during active and idle states			35	200	mV
V <sub>TX_idle_diff-DC</sub>	DC Electrical idle differential output voltage	Voltage must be low pass filtered to remove any AC component	0		10	mV
V <sub>detect</sub>	Voltage change to allow receiver detect	Positive voltage to sense receiver termination			600	mV
t <sub>R</sub> , t <sub>F</sub>	Output rise/fall time	20%–80% of differential voltage measured 1" from the output pin	30	65		ps
t <sub>RF_MM</sub>	Output rise/fall time mismatch	20%–80% of differential voltage measured 1" from the output pin		1.5	20	ps
T <sub>diff_LH</sub> , T <sub>diff_HL</sub>	Differential propagation delay	De-Emphasis = –3.5 dB (CH 0 and CH 1). Propagation delay between 50% level at input and output		305	370	ps
t <sub>idleEntry</sub> , t <sub>idleExit</sub>	Idle entry and exit times	See <a href="#">Figure 4</a>		4	6	ns
C <sub>TX</sub>	Tx input capacitance to GND	At 2.5 GHz		1.25		pF

## ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>EQUALIZATION</b>					
$T_{TX-EYE}^{(1)(2)}$ <b>Total jitter (Tj) at point A</b>	Device setting: OS1 = L, DE1 = -6 dB, EQ1 = 7 dB		0.23	0.5	UI <sup>(3)</sup> p-p
$DJ_{TX}^{(2)}$ Deterministic jitter (Dj)			0.14	0.3	
$RJ_{TX}^{(2)(4)}$ Random jitter (Rj)			0.08	0.2	
$T_{TX-EYE}^{(1)(2)}$ <b>Total jitter (Tj) at point B</b>	Device setting: OS2 = H, DE2 = -6 dB, EQ2 = 7dB		0.15	0.5	UI <sup>(3)</sup> p-p
$DJ_{TX}^{(2)}$ Deterministic jitter (Dj)			0.07	0.3	
$RJ_{TX}^{(2)(4)}$ Random jitter (Rj)			0.08	0.2	

(1) Includes RJ at  $10^{-12}$  BER

(2) Deterministic jitter measured with K28.5 pattern, Random jitter measured with K28.5 pattern at the ends of reference channel in [Figure 6](#), VID=1000mVpp, 5Gbps, -3.5dB DE from source

(3) UI = 200ps

(4) Rj calculated as 14.069 times the RMS random jitter for  $10^{-12}$  BER

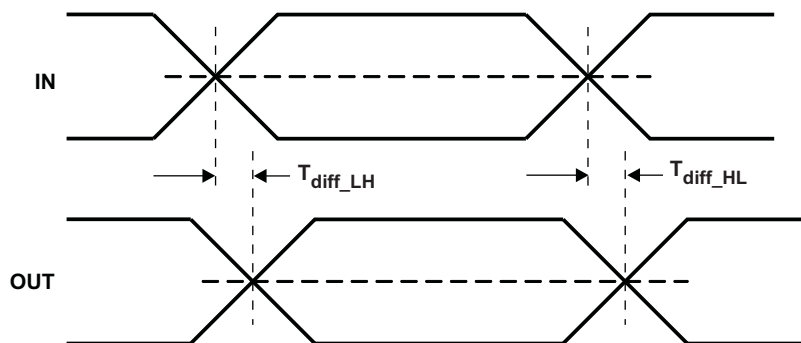


Figure 3. Propagation Delay

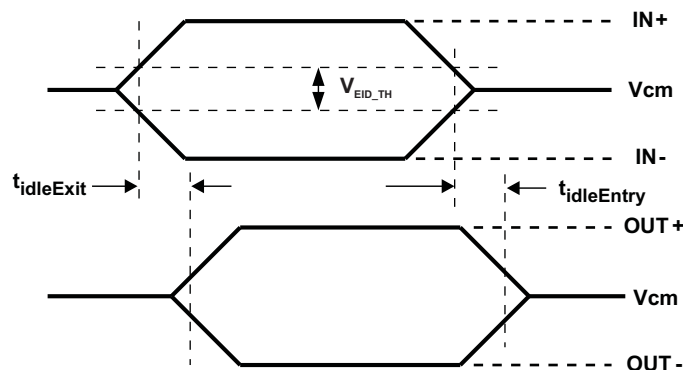


Figure 4. Electrical Idle Mode Exit and Entry Delay

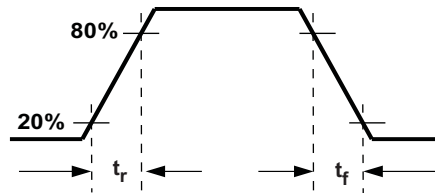


Figure 5. Output Rise and Fall Times

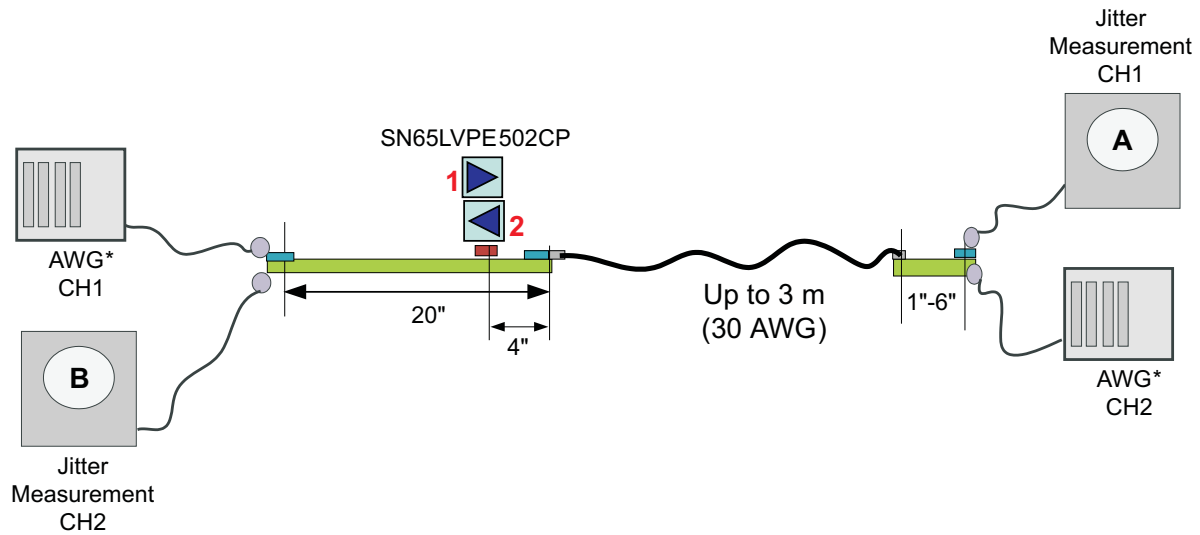


Figure 6. Jitter Measurement Setup

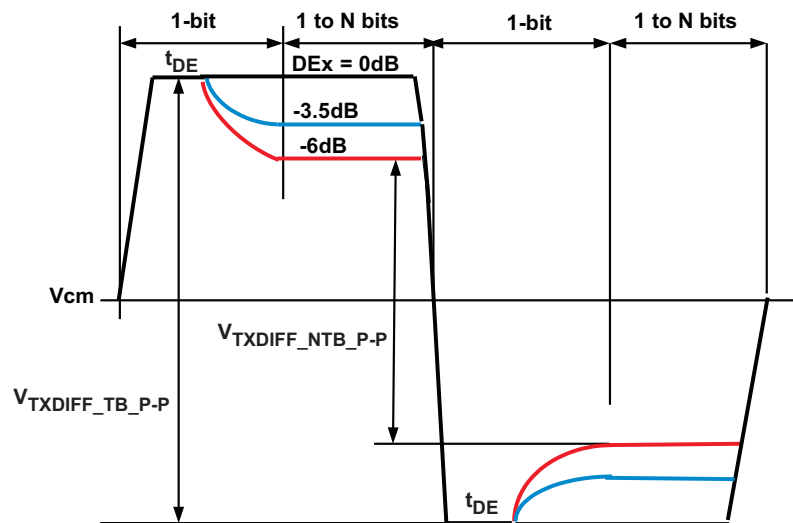
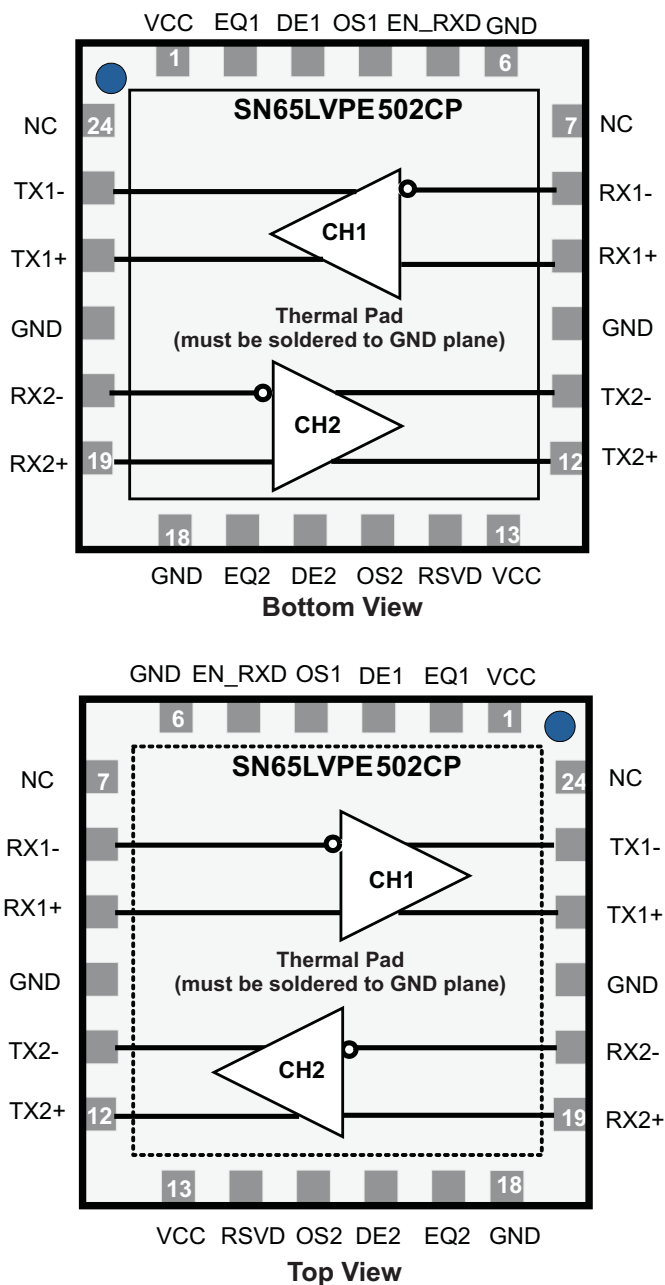


Figure 7. Output De-Emphasis Levels OSx = NC

## DEVICE INFORMATION



**Figure 8. Flow-Through Pin-Out**

**Table 1. Pin Functions**

PIN		I/O Type	Description
Number	Name		
HIGH SPEED DIFFERENTIAL I/O PINS			
8	RX1–	I, CML	Non-inverting and inverting CML differential input for CH 1 and CH 2. These pins are tied to an internal voltage bias by dual termination resistor circuit.
9	RX1+	I, CML	
20	RX2–	I, CML	
19	RX2+	I, CML	



Table 1. Pin Functions (continued)

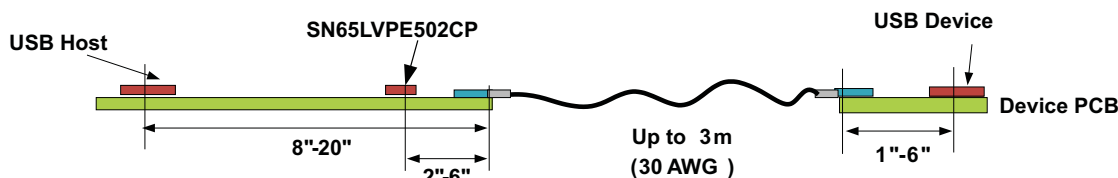
PIN		I/O Type	Description
Number	Name		
23	TX1–	O, VML	Non-inverting and inverting VML differential output for CH 1 and CH 2. These pins are internally tied to voltage bias by termination resistors.
22	TX1+	O, VML	
11	TX2–	O, VML	
12	TX2+	O, VML	
DEVICE CONTROL PIN			
5	EN_RXD	I, LVCMOS	Sets device operation modes per <a href="#">Table 2</a> . Internally pulled to VCC
14	RSVD	I, LVCMOS	RSVD, internally pulled to GND. Can be left as No-connect.
7, 24	NC	No-connect	Pads are not internally connected
EQ CONTROL PINS <sup>(1)</sup>			
3, 16	DE1, DE2	I, LVCMOS	Selects de-emphasis settings for CH 1 and CH 2 per <a href="#">Table 2</a> . Internally tied to Vcc/2
2, 17	EQ1, EQ2	I, LVCMOS	Selects equalization settings for CH 1 and CH 2 per <a href="#">Table 2</a> . Internally tied to Vcc/2
4, 15	OS1, OS2	I, LVCMOS	Selects output amplitude for CH 1 and CH 2 per <a href="#">Table 2</a> . Internally tied to Vcc/2
POWER PINS			
1,13	VCC	Power	Positive supply should be 3.3V ± 10%
6, 10, 18, 21	GND	Power	Supply ground

(1) Internally biased to Vcc/2 with >200kΩ pull-up/pull-down. When pins are left as NC board leakage at this pin pad must be < 1 μA otherwise drive to Vcc/2 to assert mid-level state

Table 2. Signal Control Pin Setting

OUTPUT SWING AND EQ CONTROL (at 2.5 GHz)			
OSx <sup>(1)</sup>	TRANSISTION BIT AMPLITUDE (TYP mVpp)	EQx <sup>(1)</sup>	EQUALIZATION (dB)
NC (default)	1042	NC (default)	0
0	908	0	7
1	1127	1	15
OUTPUT DE CONTROL (at 2.5 GHz)			
DEx <sup>(1)</sup>	OSx <sup>(1)</sup> = NC	OSx <sup>(1)</sup> = 0	OSx <sup>(1)</sup> = 1
NC (default)	0 dB	0 dB	0 dB
0	–3.5 dB	–2.2 dB	–4.4 dB
1	–6.0 dB	–5.2 dB	–6.0 dB
CONTROL PINS SETTINGS			
EN_RXD	DEVICE FUNCTION		
1 (default)	Normal Operation		
0	Sleep Mode		

(1) Where x = Channel 1 or Channel 2



NOTE: For more detailed placement example of redriver see typical eye diagrams and jitter plots at end of data sheet.

Figure 9. Redriver Placement Example

## DETAILED DESCRIPTION

### Programmable EQ, De-Emphasis and Amplitude Swing

The SN65LVPE502CP is designed to minimize signal degradation effects such as crosstalk and inter-symbol interference (ISI) that limits the interconnect distance between two devices. The input stage of each channel offers selectable equalization settings that can be programmed to match loss in the channel. The differential outputs provide selectable de-emphasis to compensate for the anticipated distortion USB 3.0 signal will experience. Level of de-emphasis will depend on the length of interconnect and its characteristics. The SN65LVPE502CP provides a unique way to tailor output de-emphasis on a per channel basis with use of DE and OS pins. All Rx and Tx equalization settings supported by the device are programmed by six 3-state pins as shown in [Table 2](#).

### Low Power Modes

Device supports three low power modes as described below

#### 1. Sleep Mode

Initiated anytime EN\_RXD undergoes a high to low transition and stays low or when device powers up with EN\_RXD set low. In sleep mode both input and output terminations are held at HiZ and device ceases operation to conserve power. Sleep mode max power consumption is 1mW, entry time is 2μs, device exits sleep mode to Rx.Detect mode after EN\_RXD is driven to Vcc, exit time is 100μs max.

#### 2. RX Detect Mode--When no remote device is connected

Anytime LVPE502CP detects a break in link (i.e. when upstream device is disconnected) or after power-up fails to find a remote device, LVPE502CP goes to Rx Detect mode and conserves power by shutting down majority of its internal circuitry. In this mode input termination for both channels are driven to Hi-Z. In Rx Detect mode device power is <10mW (TYP) or less than 5% of its normal operating power. This feature is very useful in saving system power in mobile applications like notebook PC where battery life is critical.

Anytime an upstream device gets reconnected the redriver automatically senses the connection and goes to normal operating mode. This operation requires no setting to the device.

#### 3. U2/U3 Mode

With the help of internal timers the device tracks when link enters USB 3.0 low power modes U2 and U3; in these modes link is in electrical idle state. LVPE502CP will selectively turn-off internal circuitry to save on power. Typical power saving is about 75% lower than normal operating mode. The device will automatically revert to active mode when signal activity (LFPS) is detected.

## Receiver Detection

### At Power Up or Reset

After power-up or anytime EN\_RXD is toggled, RX.Detect cycle is performed by first setting Rx termination for each channel to Hi-Z, device then starts sensing for receiver termination that may be attached at the other end of each TX.

If receiver is detected on both channel

- The TX and RX terminations are switched to  $Z_{DIFF\_TX}$ ,  $Z_{DIFF\_RX}$  respectively.

If no receiver is detected on one or both channels

- The transmitter is pulled to Hi-Z
- The channel is put in low power mode
- Device attempts to detect Rx termination in 12 ms (TYP) interval until termination is found or device is put in sleep mode

### During U2/U3 Link State

Rx detection is also performed periodically when link is in U2/U3 states. However in these states during Rx detection, input termination is not automatically disabled before performing Rx.Detect. If termination is found device goes back to its low power state if termination is not found then device disables its input termination and then jumps to power-up RX.Detect state.

## Electrical Idle Support

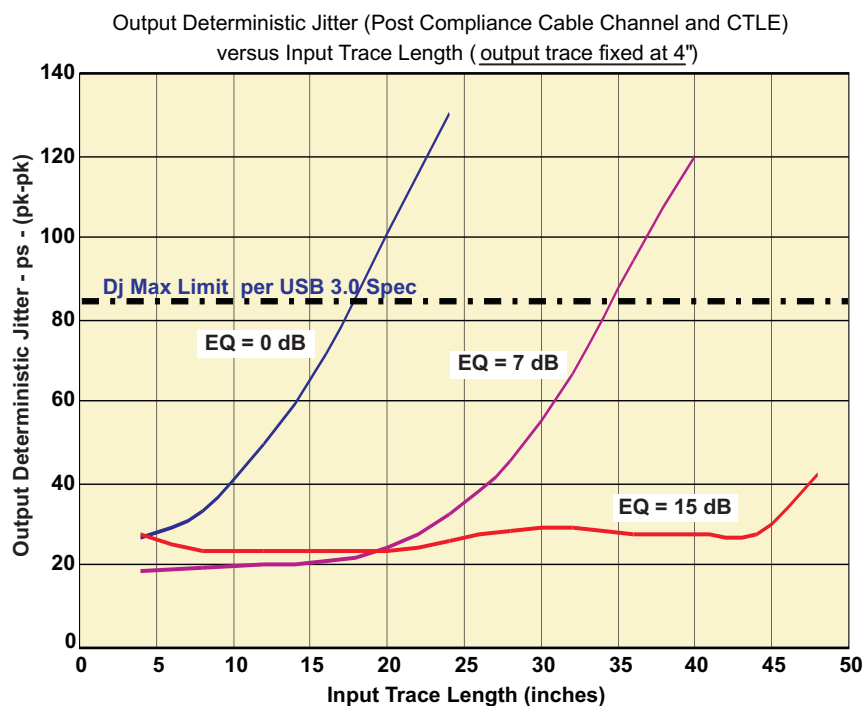
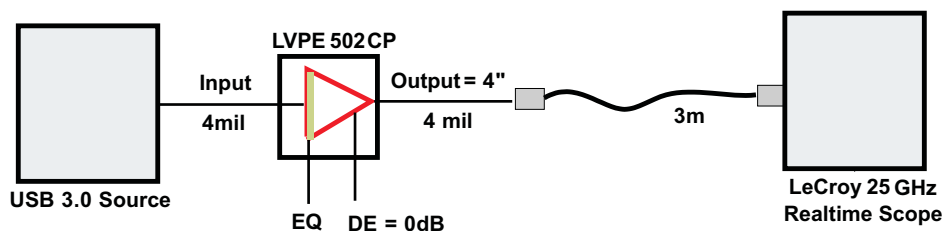
Electrical idle support is needed for low frequency periodic signaling (LFPS) used in USB 3.0 side band communication. A link is in an electrical idle state when the TX± voltage is held at a steady constant value like the common mode voltage. LVPE502CP detects an electrical idle state when RX± voltage at the device pin falls below VRX\_LFPS\_DIFFp-p min. After detection of an idle state in a given channel the device asserts electrical idle state in its corresponding TX. When RX± voltage exceeds VRX\_LFPS\_DIFFp-p max normal operation is restored and output start passing input signal. Electrical idle exit and entry time is speccified at < 6ns.

## TYPICAL EYE DIAGRAM AND PERFORMANCE CURVES

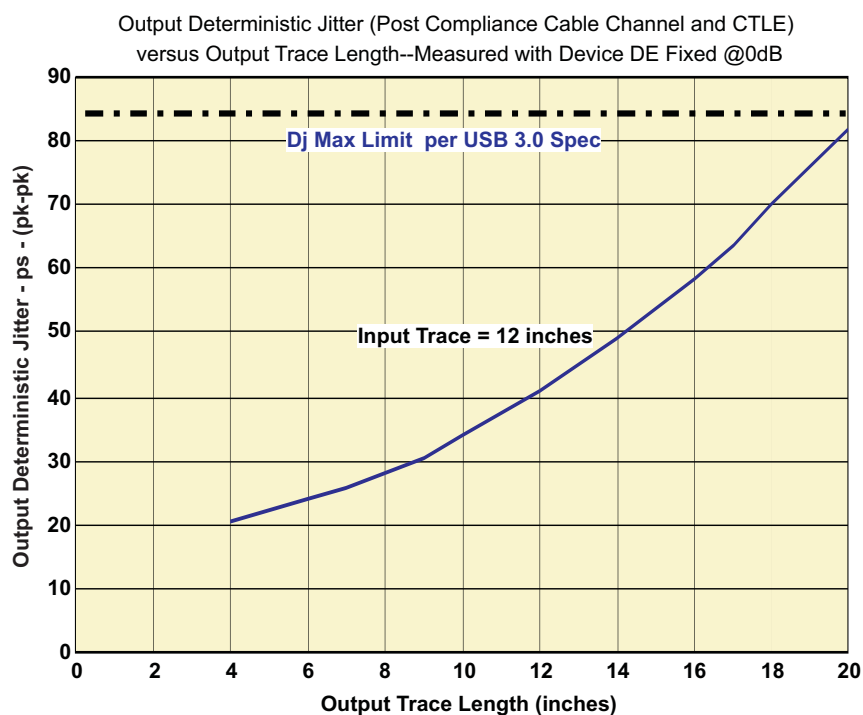
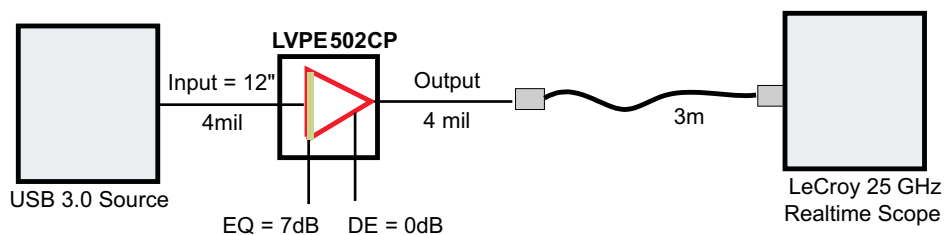
Measurement equipment details:

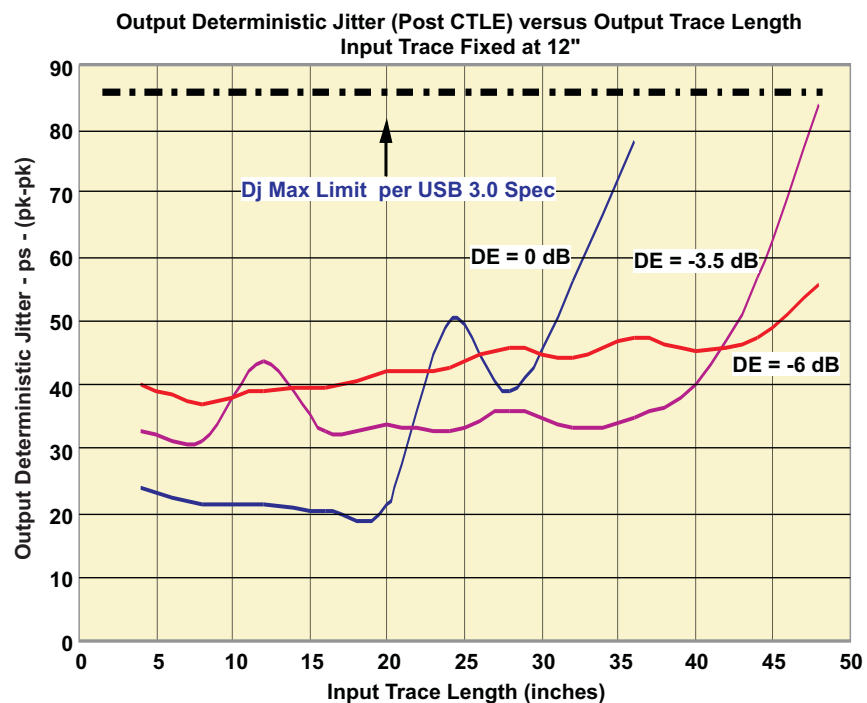
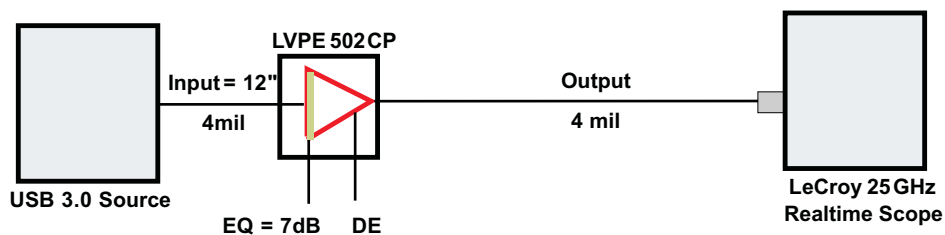
- Generator (source) LeCroy PERT3,
- Signal: 5Gbps, 1000mVp-p, 3.5 dB De-Emphasis
- Tj and Dj measurements based on CP0 (USB 3 compliance pattern) which is D0.0 or logical idle with SKP sequences removed
- Rj measurements based on CP1 or D10.2 symbol containing alternating 0s and 1s at Nyquist frequency
- Oscilloscope (Sink) LeCroy 25GHz Real Time Oscilloscope
- LeCroy QualiPHY software used to measure jitter and collect compliance eye diagrams

**Device Operating Conditions:** VCC = 3.3 V, Temp = 25°C, EQx/DEx/OSx set to their default value when not mentioned

**PLOT #1 FIXED OUTPUT TRACE +3m USB 3 CABLE WITH VARIABLE INPUT TRACE**

## PLOT #2 FIXED INPUT TRACE WITH VARIABLE OUTPUT TRACE and +3m USB 3.0 CABLE

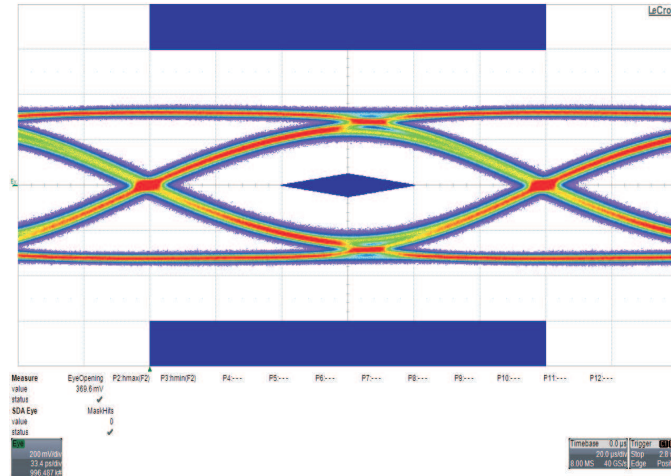


**PLOT #3 FIXED INPUT TRACE WITH VARIABLE OUTPUT TRACE and (No Cable)**

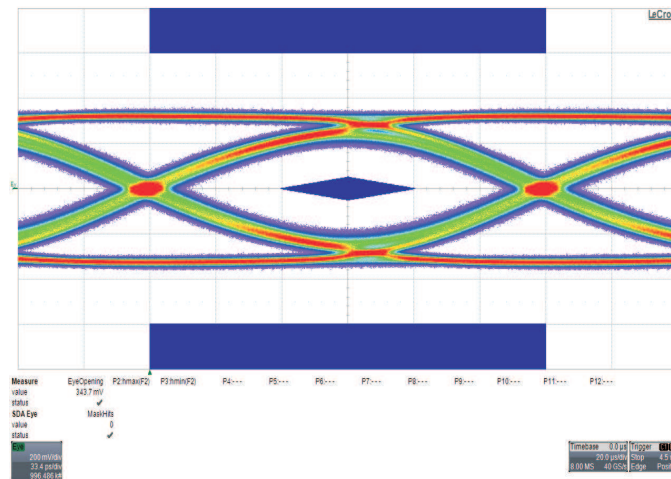
## USB 3.0 MASK EYE DIAGRAM TEST

### CASE I FIXED OUTPUT AND VARIABLE INPUT TRACE

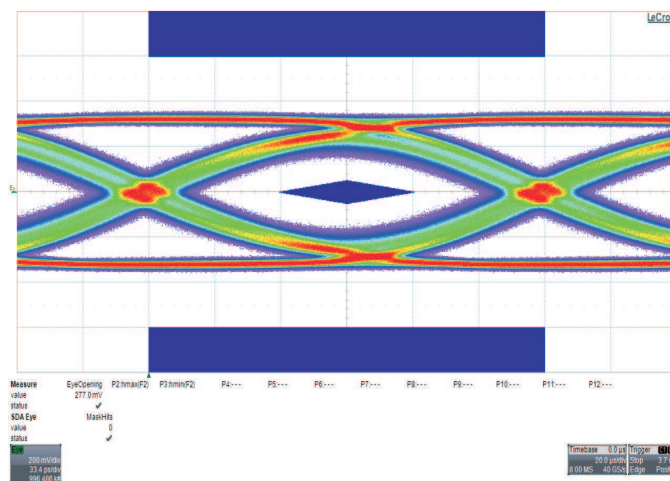
DE= 0dB, EQ = 0dB, Input = 4", Output = 4" + 3m Cable



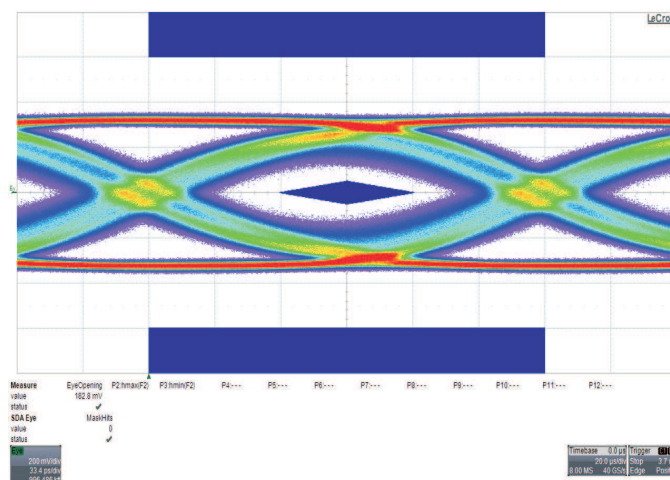
DE= 0dB, EQ = 0dB, Input = 8", Output = 4" + 3m Cable



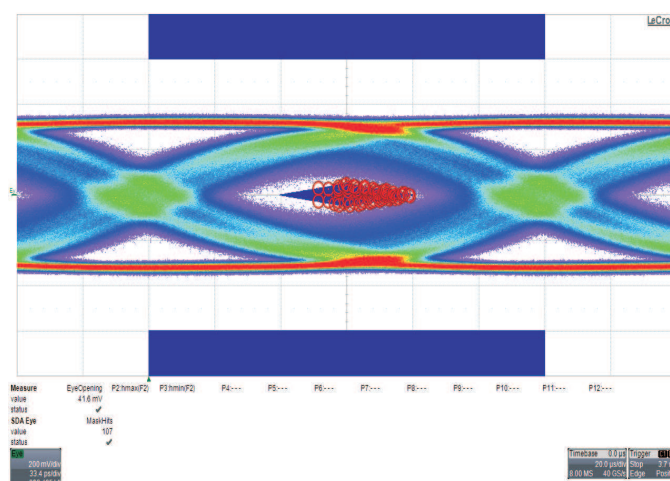
DE= 0dB, EQ = 0dB, Input = 12", Output = 4" + 3m Cable



DE= 0dB, EQ = 0dB, Input = 16", Output = 4" + 3m Cable

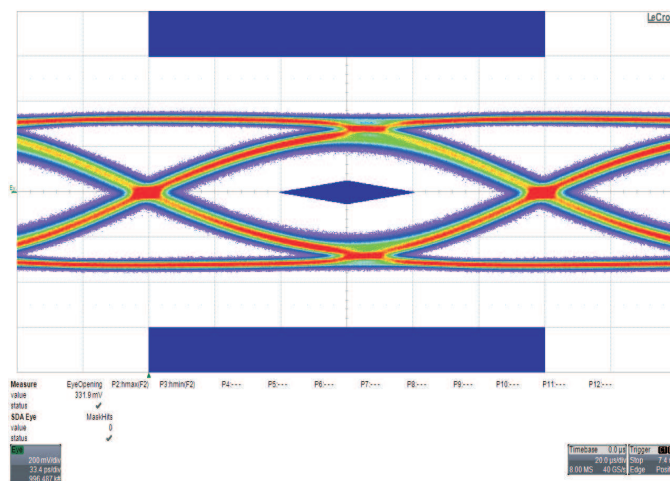


DE= 0dB, EQ = 0dB, Input = 20", Output = 4" + 3m Cable

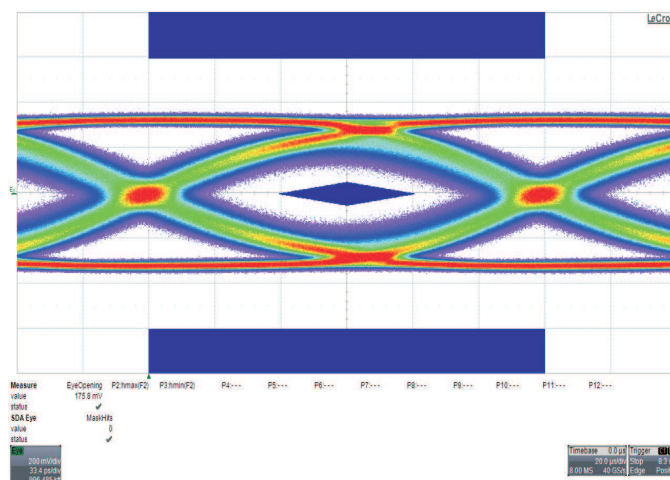




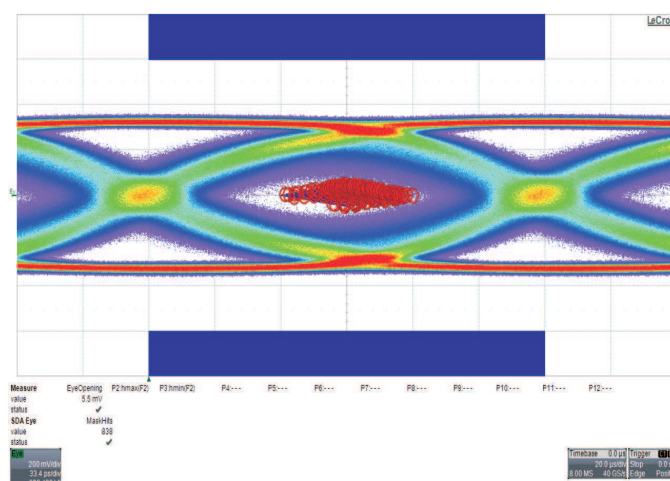
**DE= 0dB, EQ = 7dB, Input = 24", Output = 4" + 3m Cable**



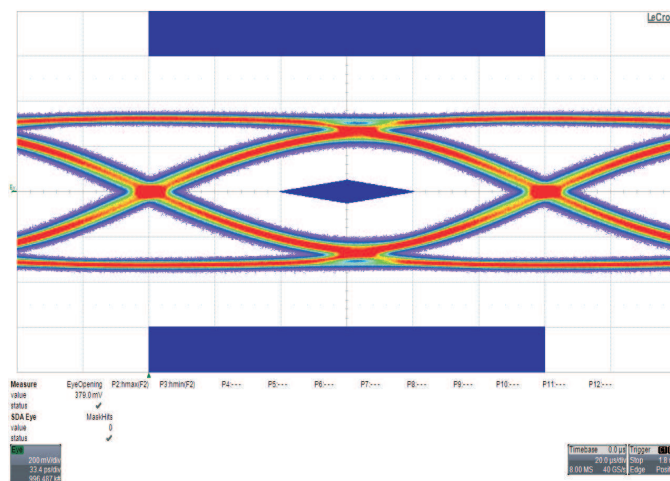
**DE= 0dB, EQ = 7dB, Input = 32", Output = 4" + 3m Cable**



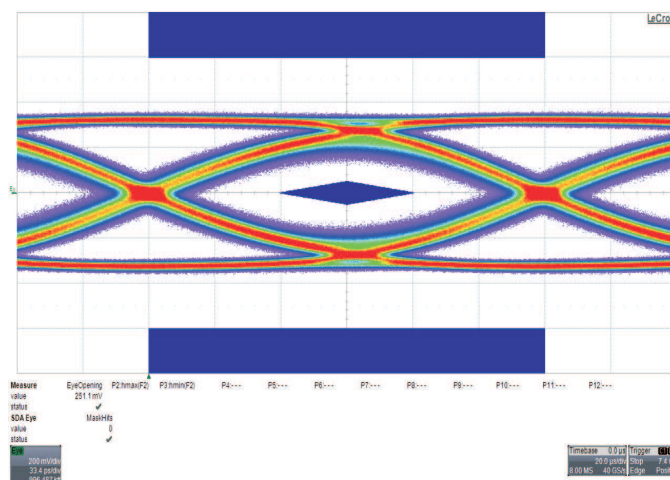
**DE= 0dB, EQ = 7dB, Input = 36", Output = 4" + 3m Cable**



**DE= 0dB, EQ = 15dB, Input = 36", Output = 4" + 3m Cable**

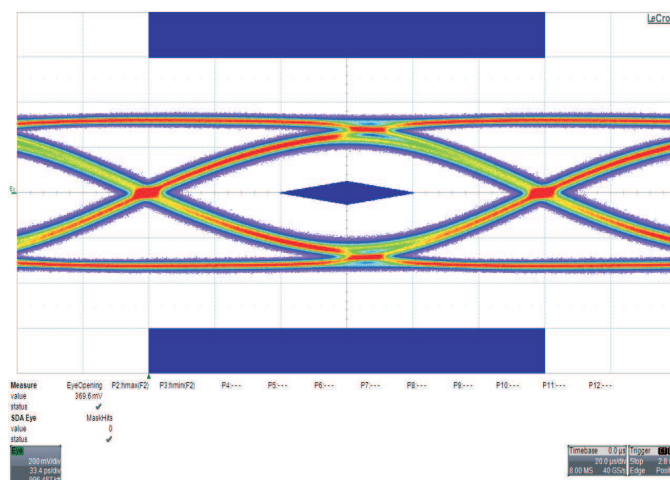


**DE= 0dB, EQ = 15dB, Input = 48", Output = 4" + 3m Cable**

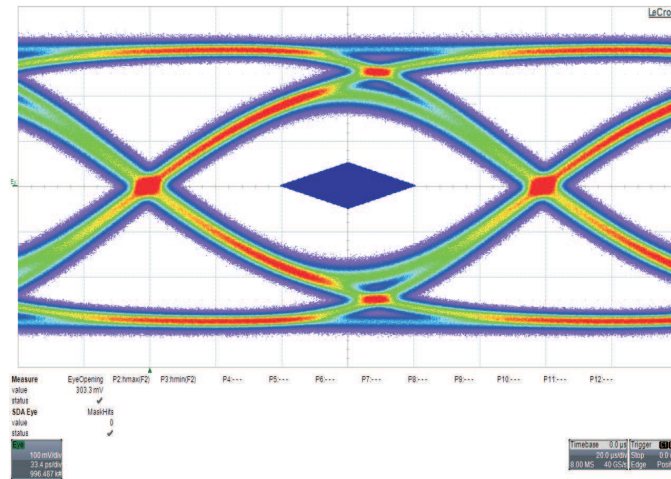


## CASE II FIXED INPUT AND VARIABLE OUTPUT TRACE+ 3m CABLE

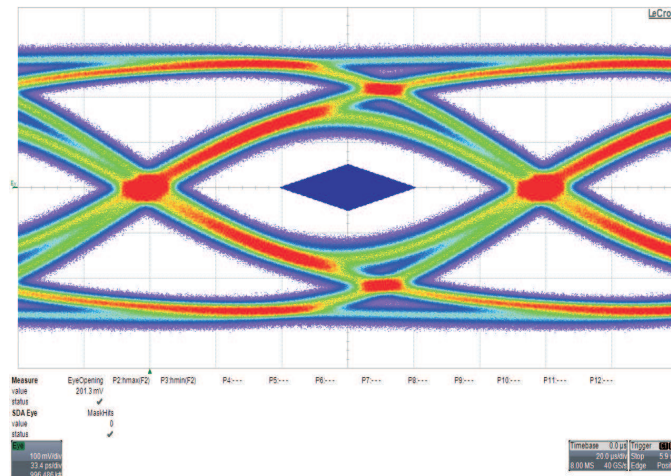
**DE= 0dB, EQ = 7dB, Input = 12", Output = 4" + 3m Cable**



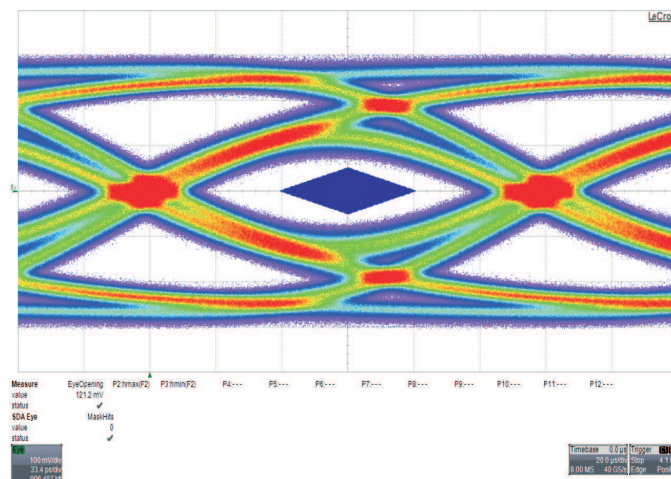
**DE= 0dB, EQ = 7dB, Input = 12", Output = 8" + 3m Cable**



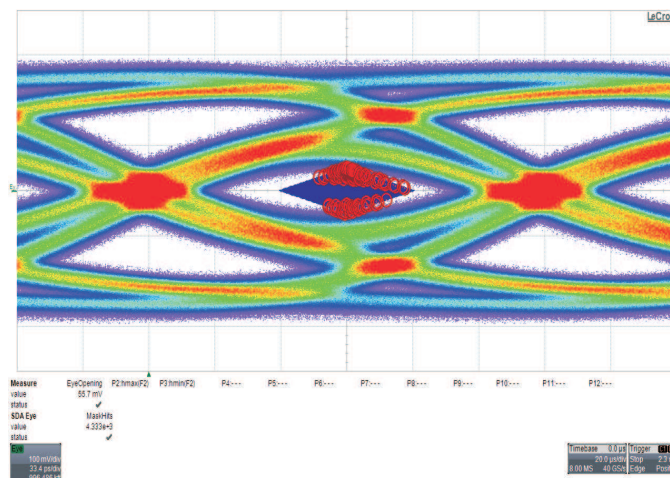
**DE= 0dB, EQ = 7dB, Input = 12", Output = 12" + 3m Cable**



**DE= 0dB, EQ = 7dB, Input = 12", Output = 16" + 3m Cable**

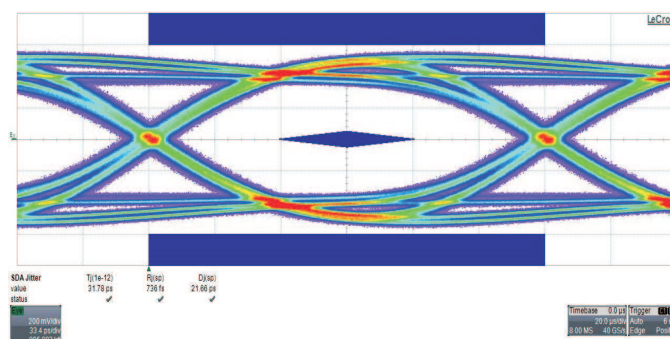


**DE= 0dB, EQ = 7dB, Input = 12", Output = 20" + 3m Cable**

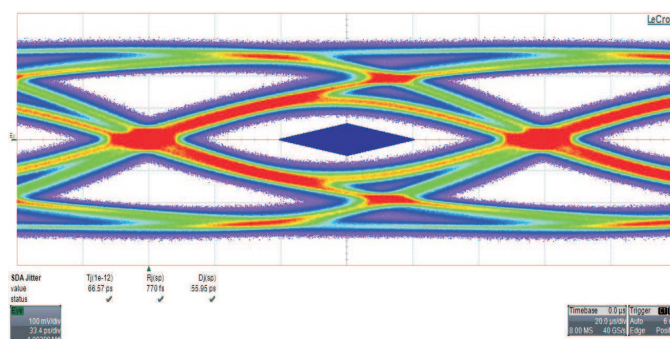


**CASE III FIXED INPUT AND VARIABLE OUTPUT TRACE (No Cable)**

**DE= 0dB, EQ = 7dB, Input = 12", Output = 8"**

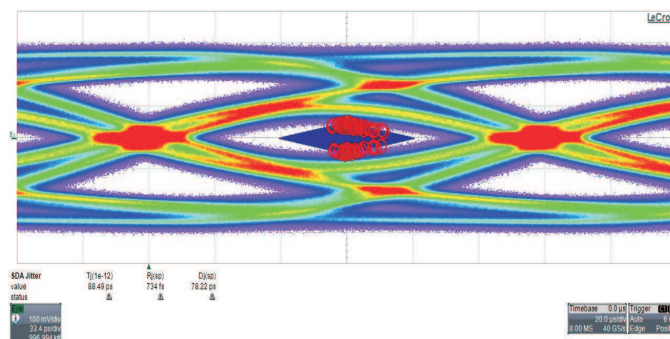


**DE= 0dB, EQ = 7dB, Input = 12", Output = 32"**

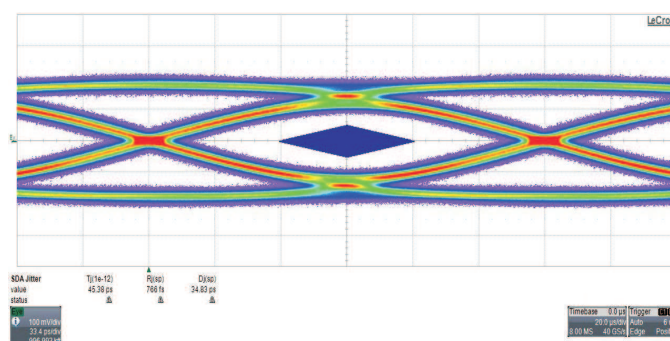




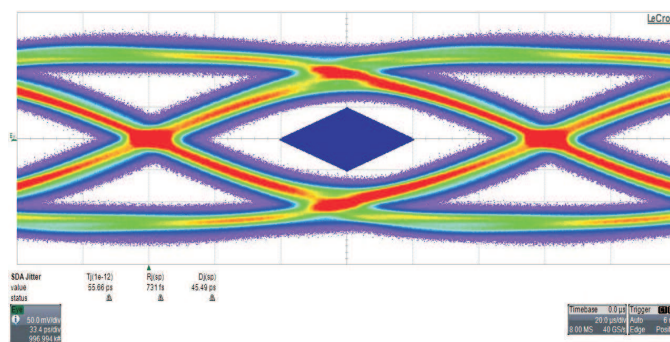
**DE= 0dB, EQ = 7dB, Input = 12", Output = 36"**



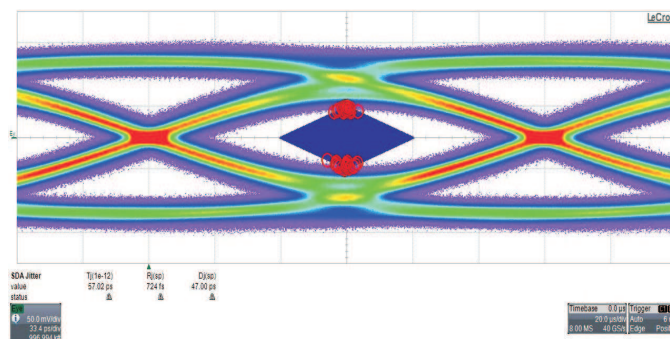
**DE= -3.5dB, EQ = 7dB, Input = 12", Output = 36"**



**DE= -6.0dB, EQ = 7dB, Input = 12", Output = 40"**



**DE= -6.0dB, EQ = 7dB, Input = 12", Output = 44"**



## REVISION HISTORY

Changes from Original (March 2011) to Revision A	Page
• Changed the Block Diagram label From: CM/EN_RXD To: EN_RXD .....	2
• Changed From: CM To: RSVD in the THERMAL CHARACTERISTICS table Test Conditions .....	3
• Changed From: CM To: RSVD in the RECOMMENDED OPERATING CONDITIONS table Test Conditions .....	4
• Changed pin name From: CM To: RSVD in the Flow-Through Pin-Out illustration .....	8
• Changed pin name and description From: CM To: RSVD in the Pin Functions table .....	9
• Deleted CM and Device Functions columns from the Control Pins Settings of <a href="#">Table 2</a> .....	9
• Deleted the USB Compliance Mode section .....	11
<hr/>	
Changes from Revision A (September 2011) to Revision B	Page
• Changed the I/O type for the TX pins (11, 12, 22, 23) From: O, CML To: O, VML .....	9
• Changed the pin Description for the TX pins (11, 12, 22, 23) From: Non-inverting and inverting CML differential output for CH 1 and CH 2 To: Non-inverting and inverting VML differential output for CH 1 and CH 2 .....	9

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65LVPE502CP1RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	502CP	<a href="#">Samples</a>
SN65LVPE502CPRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	502CP	<a href="#">Samples</a>
SN65LVPE502CPRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	502CP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVPE502CPRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2



## TAPE AND REEL BOX DIMENSIONS

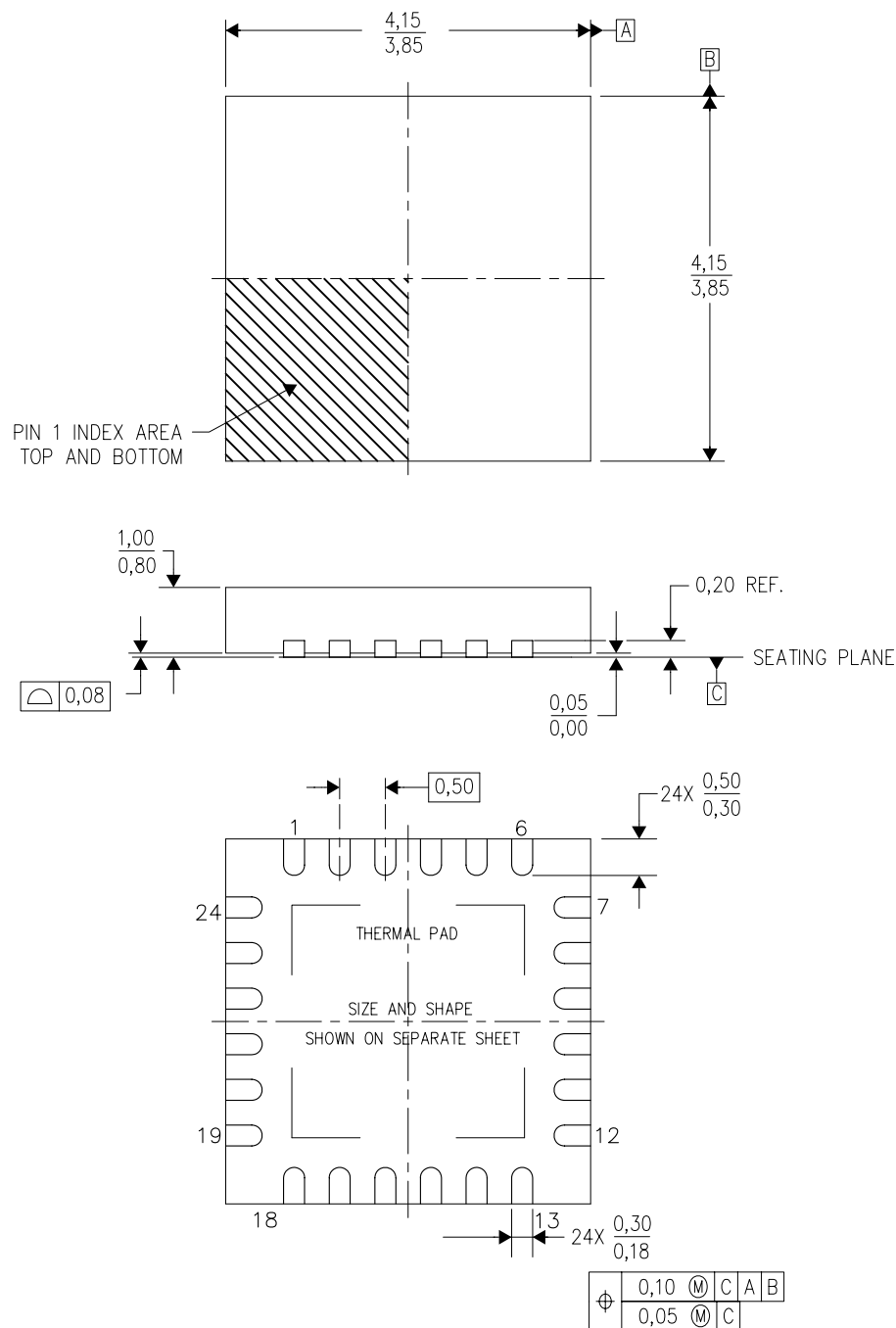


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVPE502CPRGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4204104/G 07/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-Leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

## THERMAL PAD MECHANICAL DATA

RGE (S-PVQFN-N24)

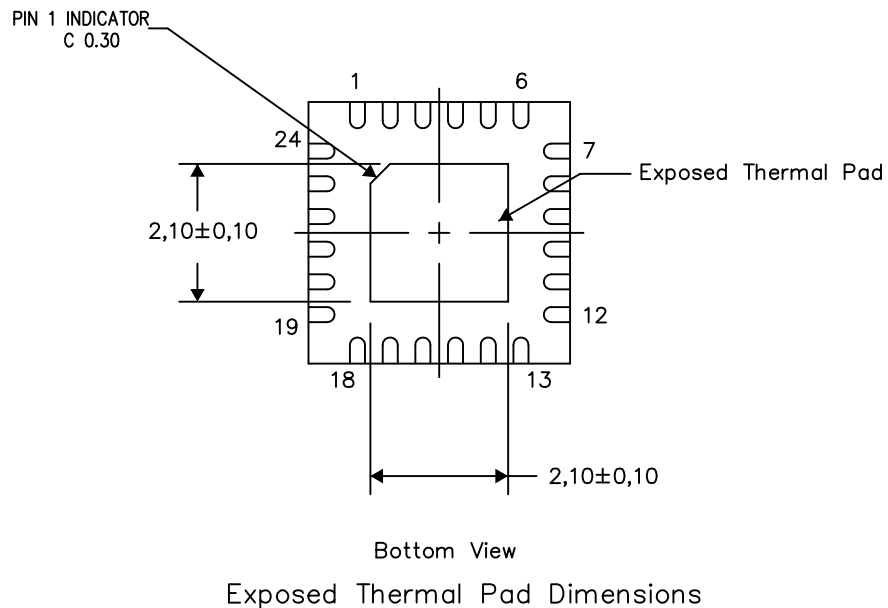
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

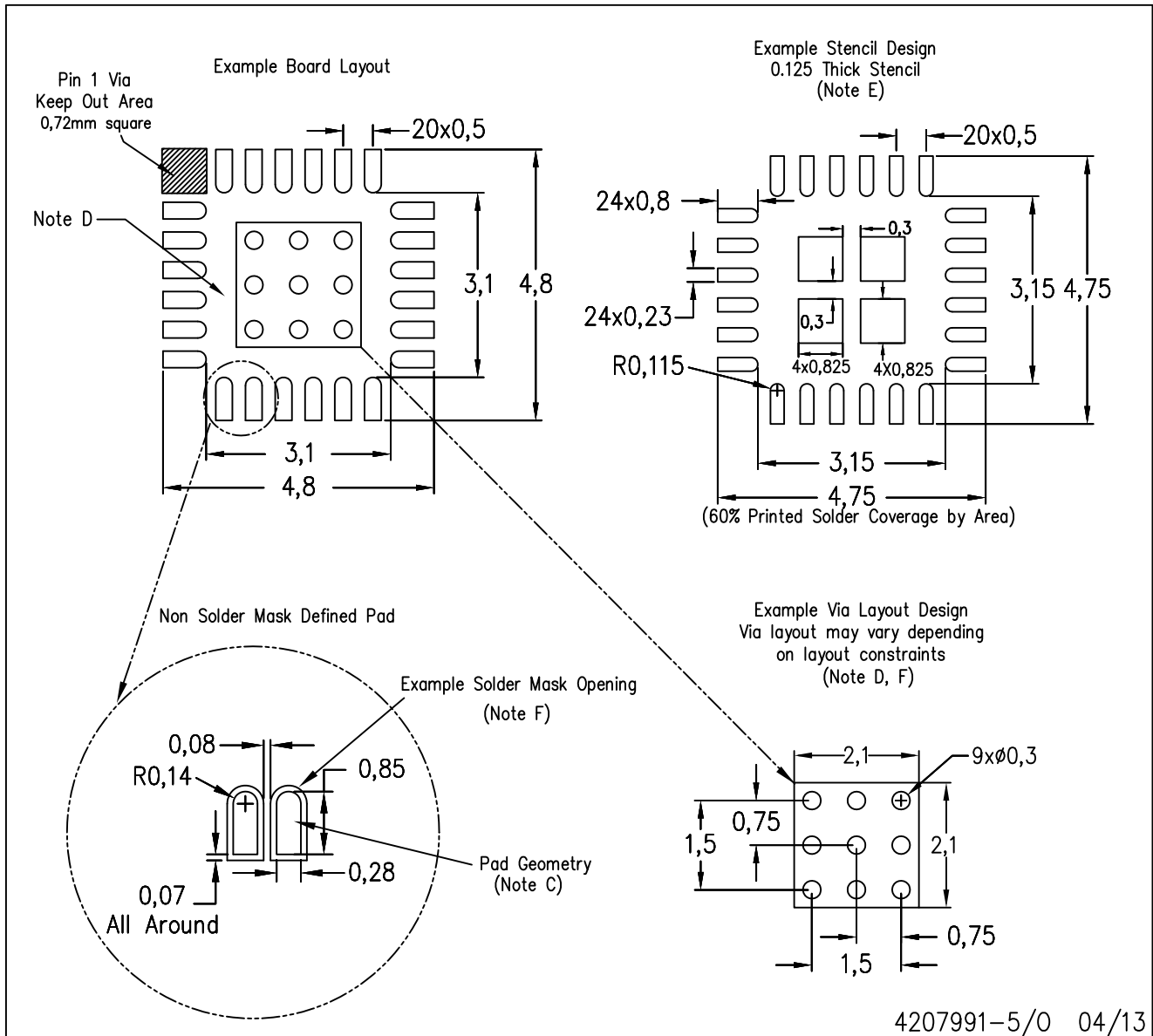


4206344-6/AC 03/13

NOTES: A. All linear dimensions are in millimeters

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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