Voltage Regulators, 1.0 A Low-Dropout Positive, Fixed and Adjustable

NCP1117LP

The NCP1117LP is the low power version of the popular NCP1117 family of low dropout voltage regulators, with reduced quiescent current. It is intended primarily for high volume consumer applications over the 0 to 125 degree temperature range. Capable of providing an output current in excess of 1 A, with a dropout voltage of 1.3 V at 1 A full current load, the series consists of an adjustable and five fixed voltage versions of 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V.

Internal protection features consist of output current limiting and built−in thermal shutdown. The NCP1117LP series can operate up to 18 V max input voltage. The device is available in the popular SOT−223 and DPAK packages.

Features

- Output Current in Excess of 1.0 A
- 1.4 V Maximum Dropout Voltage at 1 A
- Quiescent Current over 10 times Lower than Traditional 1117
- Fixed Output Voltages of 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V
- Adjustable Output Voltage Option
- No Minimum Load Requirement for Fixed Voltage Output Devices
- Good Noise Rejection
- Current Limit and Thermal Shutdown Protection
- Operation up to 18 V Input
- These are Pb−Free Devices

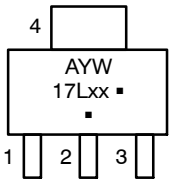
Applications

- TV and Monitors
- Set Top Boxes and Entertainment Devices
- Switching Power Supply Post Regulation
- Game Consoles and Consumer Applications
- Hard Drive Controllers

SOT−223
ST SUFFIX
CASE 318H

Pin: 1. Adjust/Ground
2. Output
3. Input

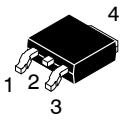
MARKING DIAGRAM



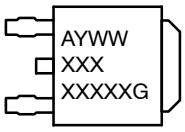
Heatsink tab is connected to Pin 2.

xx	= 15, 18, 25, 33, 50, AD
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)



DPAK
DT SUFFIX
CASE 369C



ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

TYPICAL APPLICATIONS

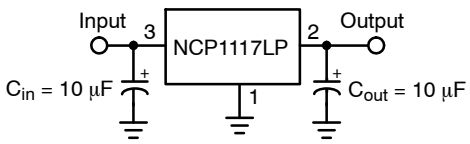


Figure 1. Fixed Output Regulator

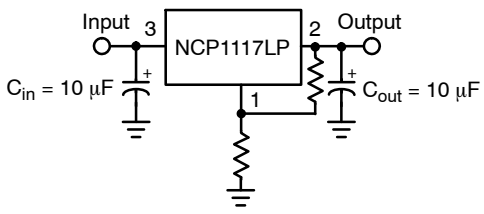


Figure 2. Adjustable Output Regulator

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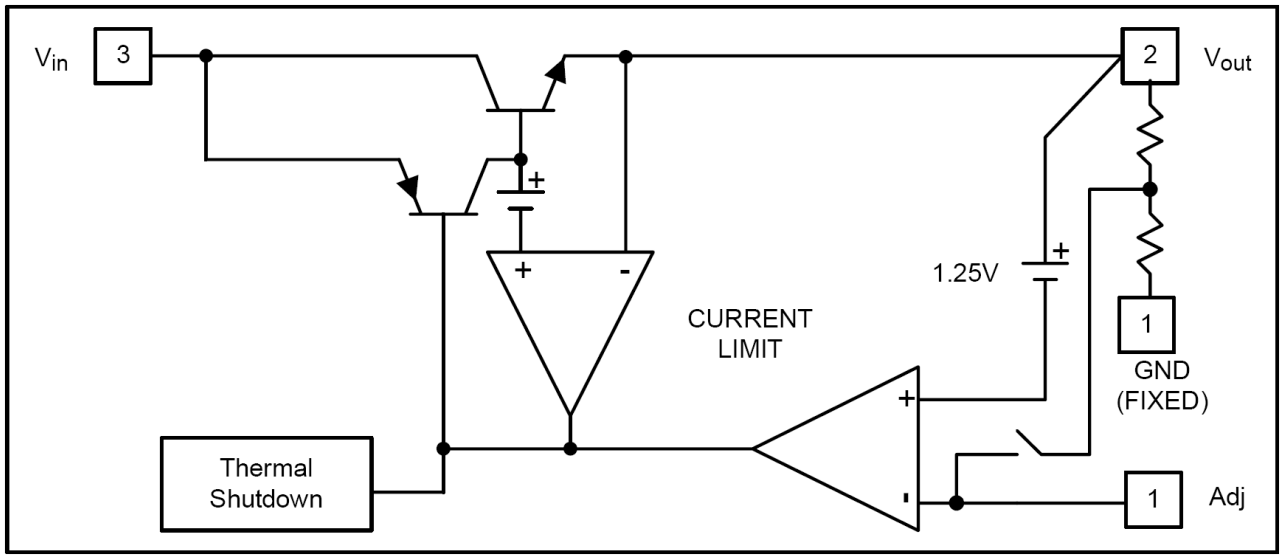


Figure 3. Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	Adj (GND)	A resistor divider from this pin to the Vout pin and ground sets the output voltage (Ground only for Fixed−Mode).
2	Vout	The output of the regulator. A minimum of 10 μF capacitor (20 mΩ ≤ ESR ≤ 20 Ω) must be connected from this pin to ground to insure stability.
3	Vin	The input pin of regulator. Typically a large storage capacitor (20 mΩ ≤ ESR ≤ 20 Ω) is connected from this pin to ground to insure that the input voltage does not sag below the minimum dropout voltage during the load transient response. This pin must always be 1.3 V (typ.) higher than Vout in order for the device to regulate properly.

Table 2. MAXIMUM RATINGS

Rating		Symbol	Value	Unit
DC Input Voltage		V_{in}	−0.3 to 18	V
Operating Junction Temperature Range		T_{OP}	0 to 125	°C
Operating Ambient Temperature Range		T_A	0 to 125	°C
Maximum Junction Temperature Range		$T_{J(max)}$	−55 to 150	°C
Power Dissipation and Thermal Characteristics − Power Dissipation (Note 1) − Thermal Resistance, Junction−to−Ambient (Note 2) − Thermal Resistance, Junction−to−Case		P_D $R_{\theta JA}$ $R_{\theta JC}$	Internally Limited 108 15	W °C/W °C/W
Electrostatic Discharge	Human Body Model	ESD	2000	V
	Machine Model		200	
Storage Temperature Range		T_{STG}	−65 to 150	°C
NOTE: This device series contains ESD protection and exceeds the following tests: ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A114) ESD MM tested per AEC−Q100−003 (EIA/JESD22−A115) Latch−up Current Maximum Rating: ≤ 150 mA per JEDEC standard: JESD78				

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: All voltages are referenced to GND pin.

1. The maximum package power dissipation is:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

2. $R_{\theta JA}$ on a 100 x 100 mm PCB Cu thickness 1 oz; T_A = 25°C

Table 3. ELECTRICAL CHARACTERISTICS (C_{in} = 10 μF, C_{out} = 10 μF, for typical value T_A = 25°C, for min and max values T_A is the operating ambient temperature range that applies unless otherwise noted.)

Parameter	Conditions		Symbol	Min	Typ	Max	Unit
Reference Voltage, Adjustable Output Devices	NCP1117−ADJ	T_J = 25°C (Vin − Vout) = 1.5 V, Io = 10 mA	V_{ref}	1.225	1.250	1.275	V
Output Voltage, Fixed Output Devices	NCP1117−1.5	T_J = 25°C 3 V ≤ Vin ≤ 12 V, Io = 10 mA	V_{out}	1.470	1.5	1.530	V
	NCP1117−1.8	T_J = 25°C 3.3 V ≤ Vin ≤ 12 V, Io = 10 mA		1.760	1.8	1.840	V
	NCP1117−2.5	T_J = 25°C 4 V ≤ Vin ≤ 12 V, Io = 10 mA		2.450	2.5	2.550	V
	NCP1117−3.3	T_J = 25°C 4.8 V ≤ Vin ≤ 12 V, Io = 10 mA		3.235	3.3	3.365	V
	NCP1117−5.0	T_J = 25°C 6.5 V ≤ Vin ≤ 12 V, Io = 10 mA		4.900	5	5.100	V
Line Regulation, Adjustable & Fixed (Note 3)	NCP1117−XXX	T_J = 25°C Vout + 1.5 V < Vin < 12 V, Io = 10 mA	Reg_{line}			0.2	%
Load Regulation (Note 3)	NCP1117−ADJ	T_J = 25°C 10 mA < Io < 1 A, Vin = 3.3 V	Reg_{load}			1	%
	NCP1117−1.5	T_J = 25°C 10 mA < Io < 1 A, Vin = 3 V			12	15	mV
	NCP1117−1.8	T_J = 25°C 10 mA < Io < 1 A, Vin = 3.3 V			15	18	mV
	NCP1117−2.5	T_J = 25°C 10 mA < Io < 1 A, Vin = 4 V			20	25	mV
	NCP1117−3.3	T_J = 25°C 10 mA < Io < 1 A, Vin = 4.7 V			26	33	mV
	NCP1117−5.0	T_J = 25°C 10 mA < Io < 1 A, Vin = 6.5 V			40	50	mV
Dropout Voltage (Vin − Vout), Adjustable & Fixed	NCP1117−XXX	Iout = 1 A, T_A = 25°C ΔVout = Vout − 100 mV			1.3	1.4	V
Current Limit, Adjustable & Fixed	NCP1117−XXX	Vin = 7 V, T_A = 25°C	Iout	1.1			A
Minimum Load Current (Note 4)	NCP1117−XXX	0°C ≤ Tj ≤ 125°C	I_{Lmin}		1	5	mA
Quiescent Current	NCP1117−fixed	Vin = 12 V Io = 10 mA	I_{QFIX}		550	700	μA
	NCP1117−ADJ		I_{QADJ}		30	50	μA
Thermal Regulation (Note 5)		T_A = 25°C, T = 30 ms pulse			0.008	0.04	%W
Ripple Rejection	NCP1117−XXX	F = 120 Hz, Cout = 25 μF tantalum, Iout = 1 A, Vin = Vout + 3 V	RR		60		dB
Thermal Shutdown	NCP1117−XXX		T_{shdn}		165		°C
Thermal Hysteresis	NCP1117−XXX		T_{hyst}		10		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
4. Guaranteed by design.
5. Thermal Regulation is defined as the change in output voltage at a time after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to Io_{max} at VIN = VIN + 1.5 V for T = 30 msec. Guaranteed by characterization.

TYPICAL CHARACTERISTICS

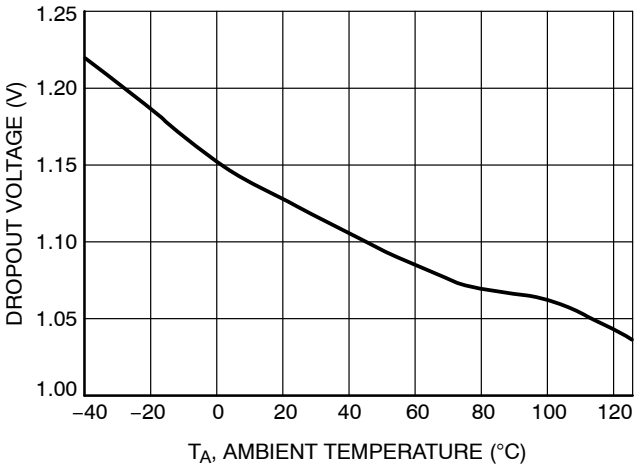


Figure 4. Dropout Voltage vs. Temperature
I_{load} = 10 mA

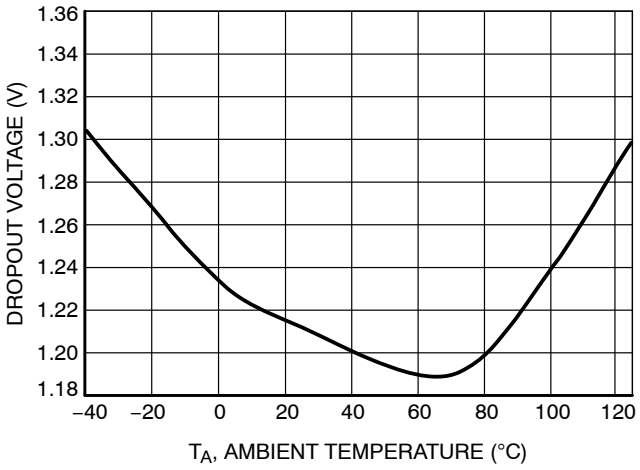


Figure 5. Dropout Voltage vs. Temperature
I_{load} = 1 A

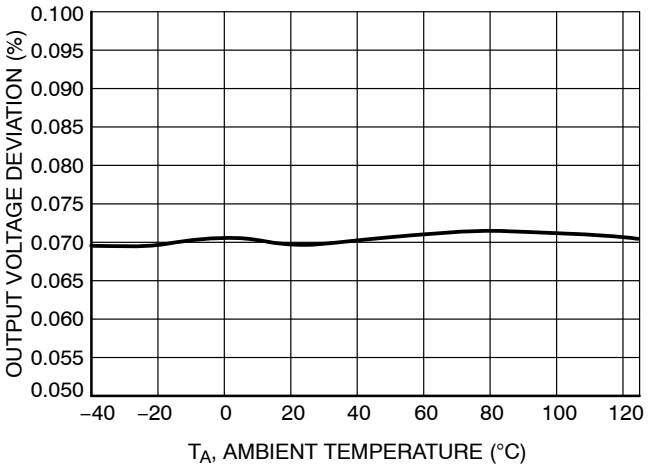


Figure 6. Line Regulation vs. Temperature
I_{load} = 10 mA

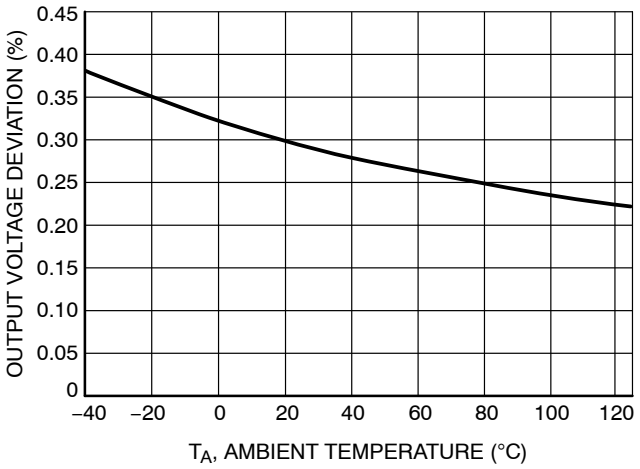


Figure 7. Load Regulation vs. Temperature
I_{load} = 1 A

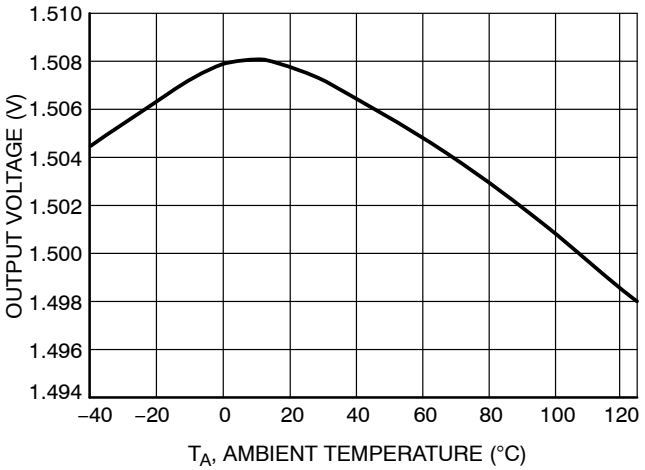


Figure 8. Output Voltage vs. Temperature
I_{load} = 10 mA

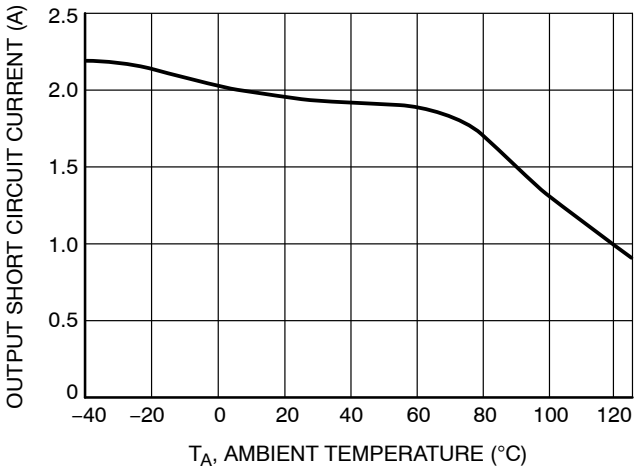


Figure 9. Output Short Circuit Current vs. Temperature

TYPICAL CHARACTERISTICS

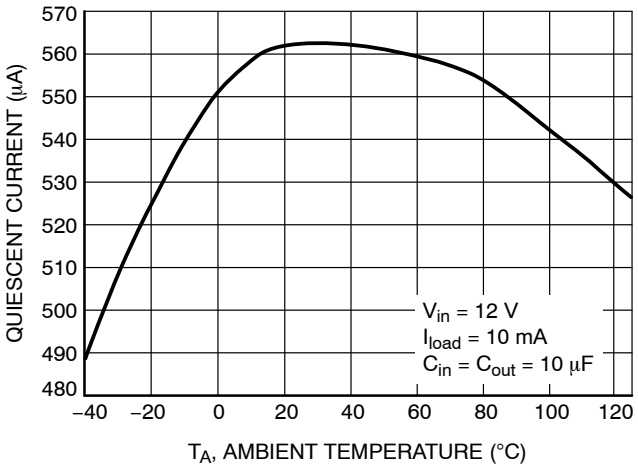


Figure 10. Quiescent Current vs. Temperature
I_{load} = 10 mA

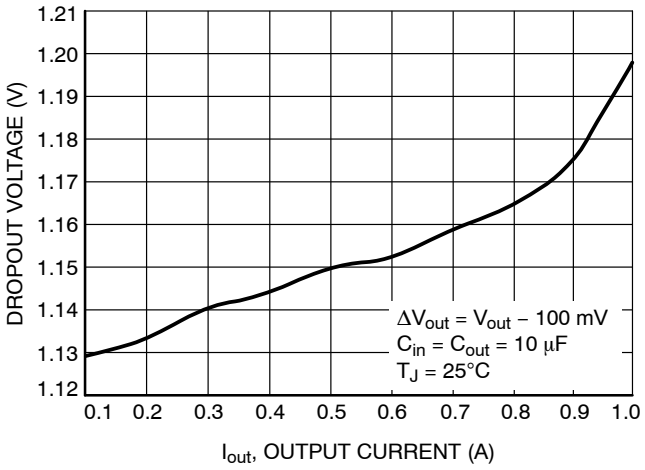


Figure 11. Dropout Voltage vs. Output Current

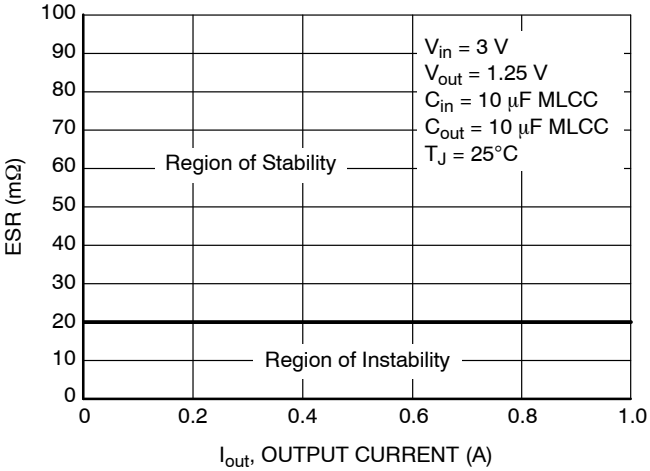


Figure 12. Equivalent Series Resistance vs. Output Current − MLCC Capacitor

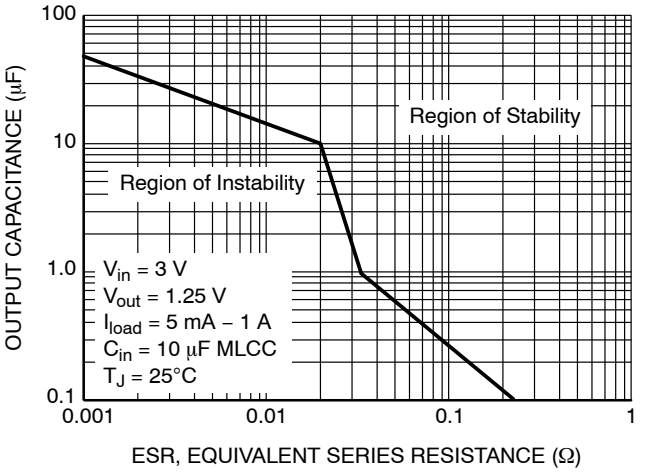


Figure 13. Output Capacitance vs. ESR MLCC Capacitor

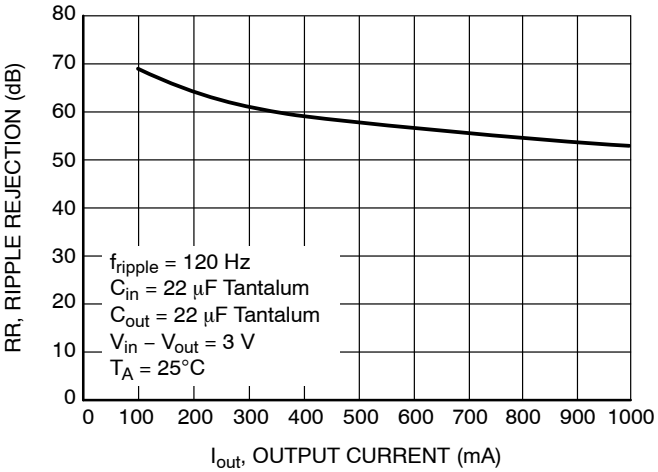


Figure 14. Ripple Rejection vs. Output Current − 1.5 V

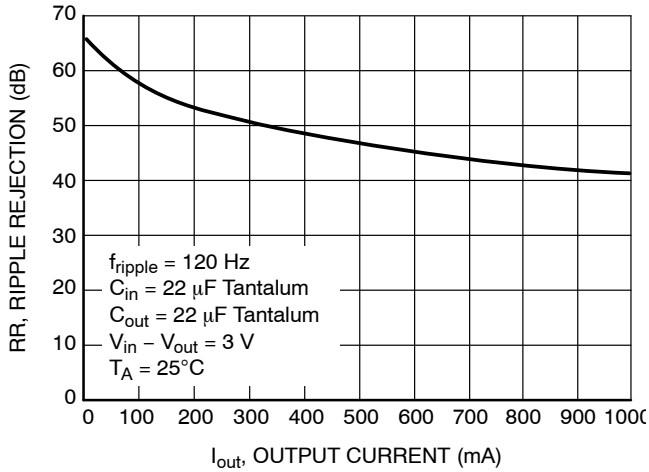


Figure 15. Ripple Rejection vs. Output Current − 5 V

TYPICAL CHARACTERISTICS

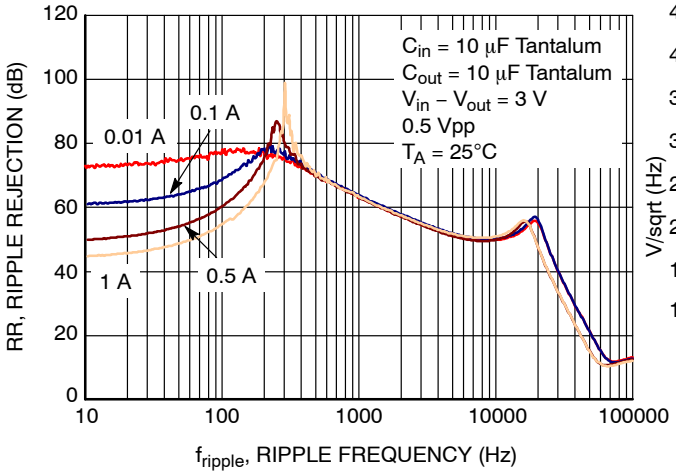


Figure 16. Ripple Rejection vs. Frequency – V_{out} = 1.5 V

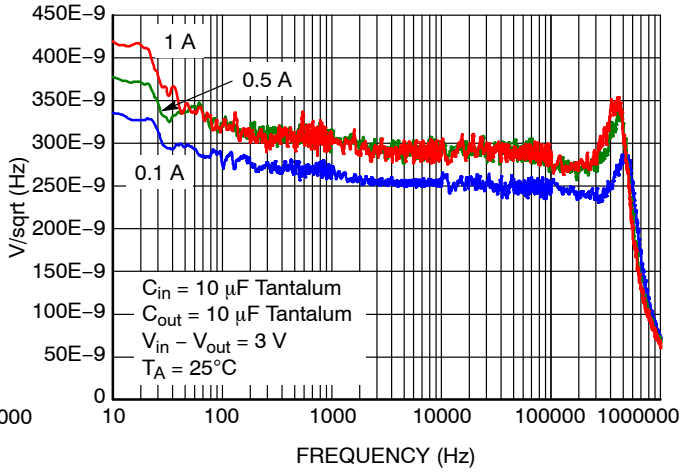


Figure 17. Output Spectral Noise Density vs. Frequency – V_{out} = 1V5

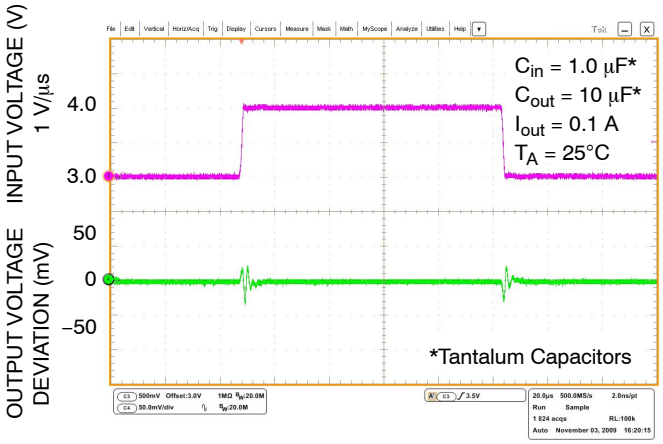


Figure 18. Line Transient Response – V_{out} = 1.5 V

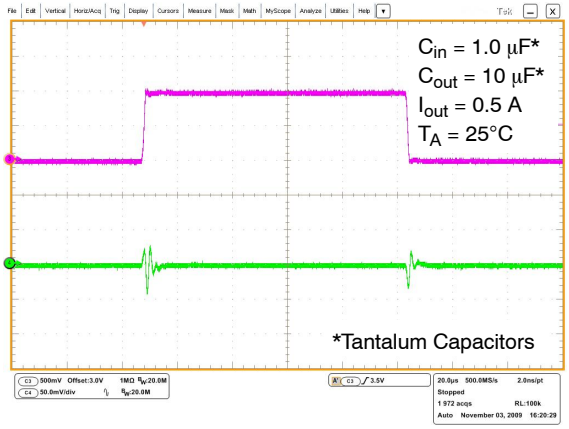


Figure 19. Line Transient Response – V_{out} = 1.5 V

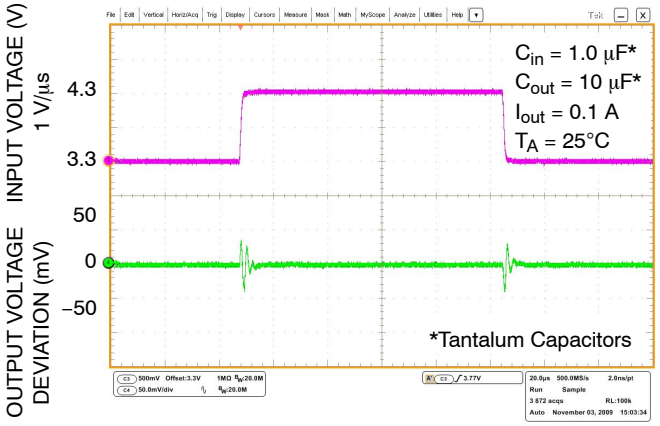


Figure 20. Line Transient Response – V_{out} = 1.8 V

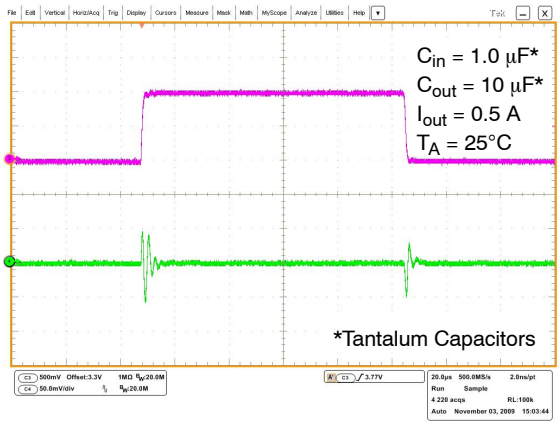


Figure 21. Line Transient Response – V_{out} = 1.8 V

TYPICAL CHARACTERISTICS

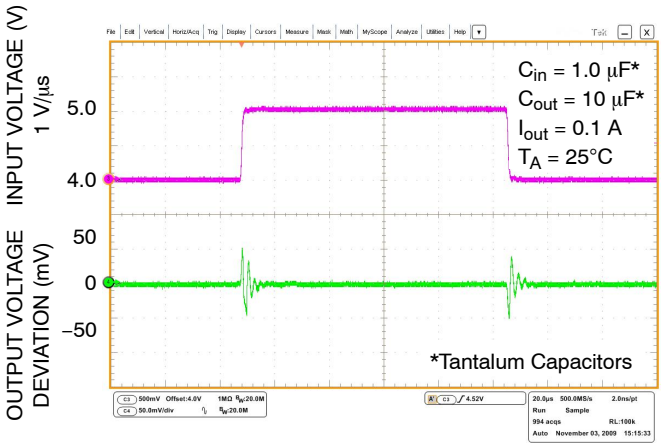


Figure 22. Line Transient Response – V_{out} = 2.5 V

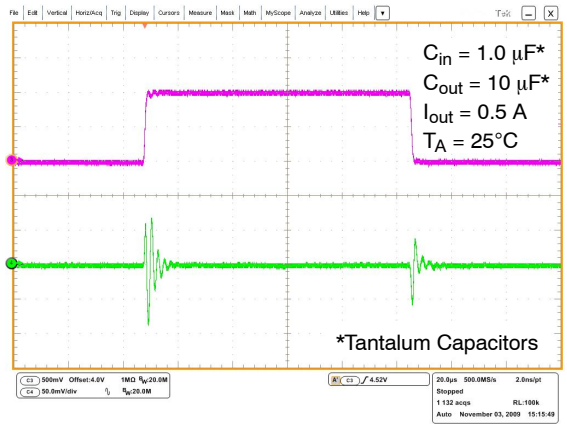


Figure 23. Line Transient Response – V_{out} = 2.5 V

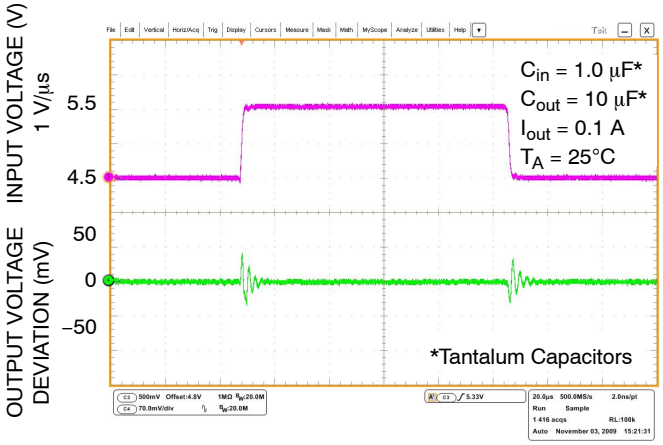


Figure 24. Line Transient Response – V_{out} = 3.3 V

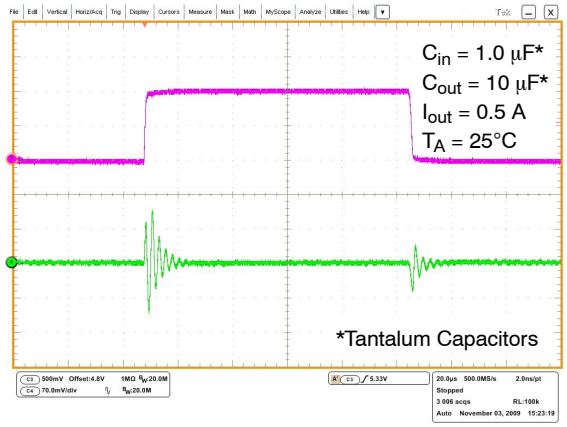


Figure 25. Line Transient Response – V_{out} = 3.3 V

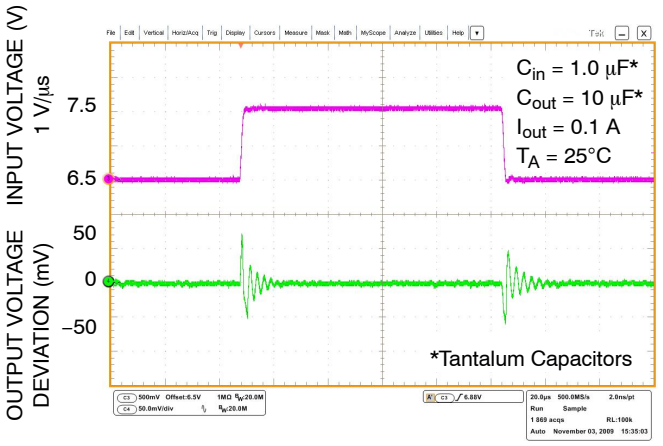


Figure 26. Line Transient Response – V_{out} = 5.0 V

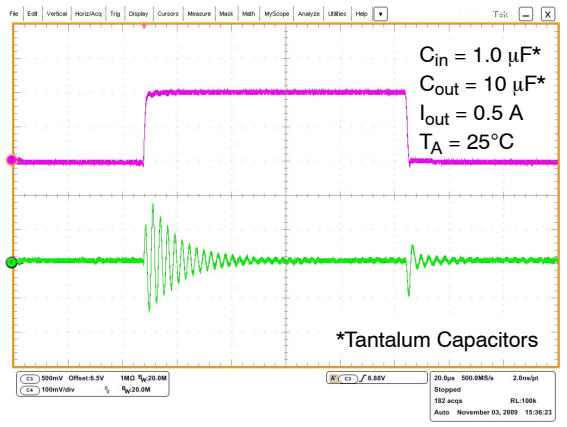


Figure 27. Line Transient Response – V_{out} = 5.0 V

TYPICAL CHARACTERISTICS

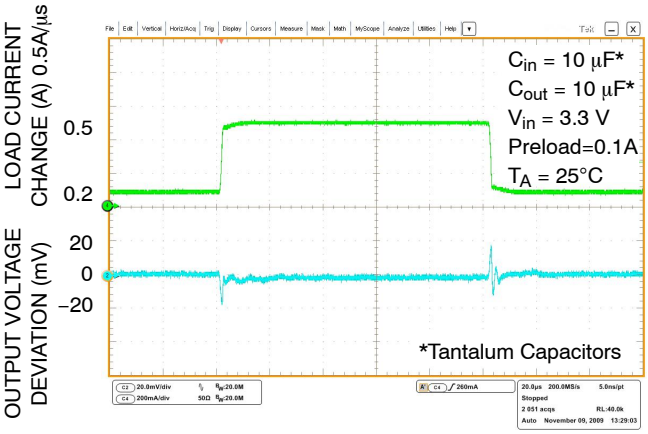


Figure 28. Load Transient Response – V_{out} = 1.8 V

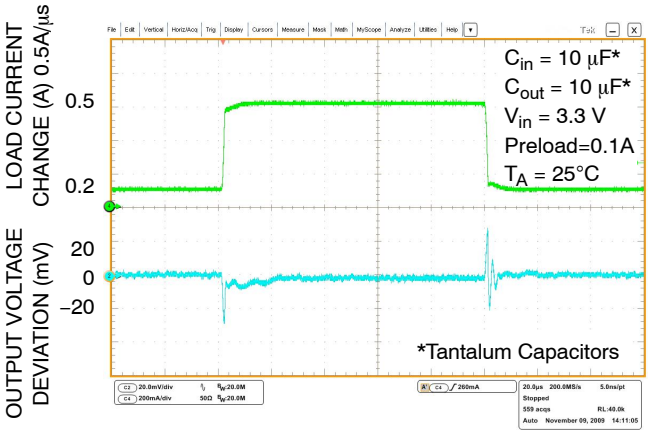


Figure 29. Load Transient Response – V_{out} = 2.5 V

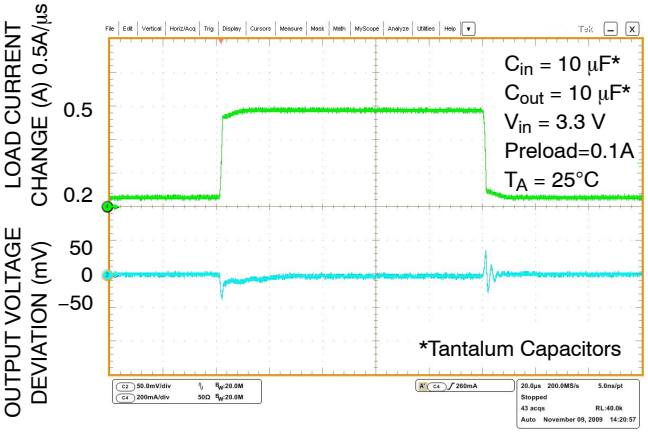


Figure 30. Load Transient Response – V_{out} = 3.3 V

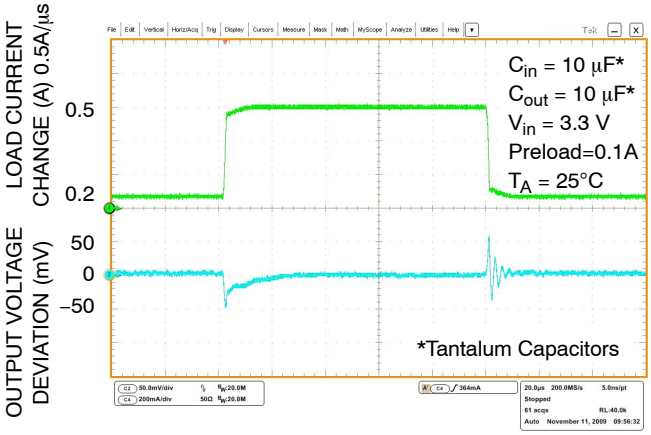


Figure 31. Load Transient Response – V_{out} = 5.0 V

TYPICAL CHARACTERISTICS

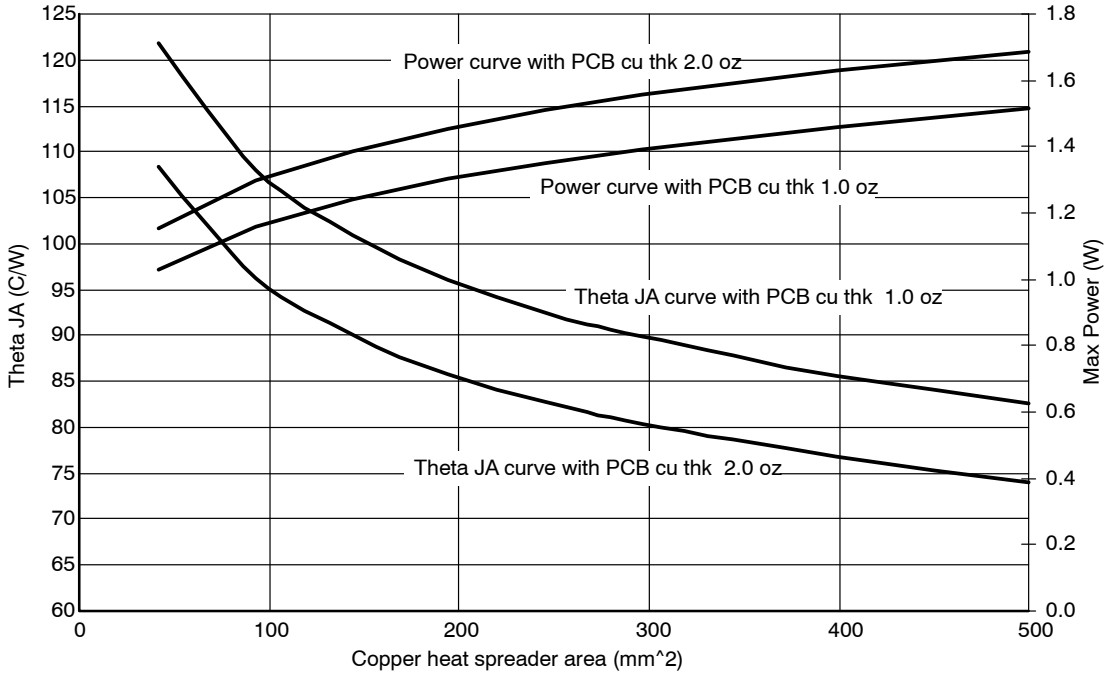


Figure 32. SOT−223 Thermal Resistance and Maximum Power Dissipation vs. P.C.B. Copper Length

APPLICATIONS INFORMATION

Introduction

The NCP1117LP is a low dropout positive fixed or adjustable mode regulator with 1 A output capability. This LDO is guaranteed to have a significant reduction in dropout voltage along with enhanced output voltage accuracy and temperature stability when compared to older industry standard three−terminal adjustable regulators.

These devices contain output current limiting, safe operating area compensation and thermal shutdown protection making them designer friendly for powering numerous consumer and industrial products. The NCP1117LP series is pin compatible with the older NCP1117.

Output Voltage

The typical application circuits for the fixed and adjustable output regulators are shown in Figures 33 and 34. The adjustable devices are floating voltage regulators. They develop and maintain the nominal 1.25 V reference voltage between the output and adjust pins. The reference voltage is programmed to a constant current source by resistor R1, and this current flows through R2 to ground to set the output voltage. The programmed current level is usually selected to be greater than the specified 5.0 mA minimum that is required for regulation. Since the adjust pin current, I_{adj}, is significantly lower and constant with respect to the programmed load current, it generates a small output voltage error that can usually be ignored. For the fixed output devices R1 and R2 are included within the device and the ground current I_{gnd} is 550 μA (typ).

External Capacitors

Input bypass capacitor C_{in} may be required for regulator stability if the device is located more than a few inches from the power source. This capacitor will reduce the circuit's sensitivity when powered from a complex source impedance and significantly enhance the output transient response. The input bypass capacitor should be mounted with the shortest possible track length directly across the regulator's input and ground terminals. A 10 μF ceramic or tantalum capacitor should be adequate for most applications.

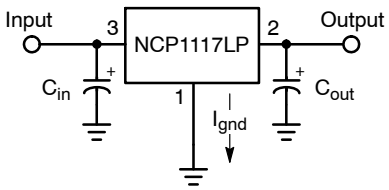
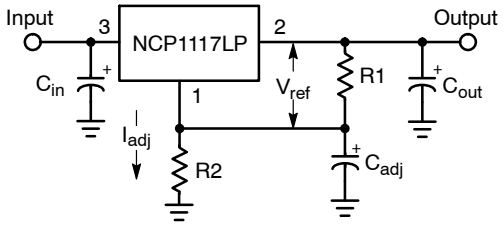


Figure 33. Fixed Output Regulator

Frequency compensation for the regulator is provided by capacitor C_{out} and its use is mandatory to ensure output stability. A minimum capacitance value of 4.7 μF with an equivalent series resistance (ESR) that is within the limits of 20 mΩ to 20 Ω is required. The capacitor type can be ceramic, tantalum, or aluminum electrolytic as long as it meets the minimum capacitance value and ESR limits over the circuit's entire operating temperature range. Higher values of output capacitance can be used to enhance loop stability and transient response with the additional benefit of reducing output noise.



$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + R2 \cdot I_{adj}$$

Figure 34. Adjustable Output Regulator

The output ripple will increase linearly for fixed and adjustable devices as the ratio of output voltage to the reference voltage increases. For example, with a 5 V regulator, the output ripple will increase by 5 V/1.25 V or 4 and the ripple rejection will decrease by 20 log of this ratio or 12 dB. The loss of ripple rejection can be restored to the values shown with the addition of bypass capacitor C_{adj}, shown in Figure 34. The reactance of C_{adj} at the ripple frequency must be less than the resistance of R1. The value of R1 can be selected to provide the minimum required load current to maintain regulation and is usually in the range of 100 Ω to 200 Ω.

$$C_{adj} > \frac{1}{2\pi \cdot f_{ripple} \cdot R1}$$

The minimum required capacitance can be calculated from the above formula. When using the device in an application that is powered from the AC line via a transformer and a full wave bridge, the value for C_{adj} is:

$$f_{ripple} = 120\ Hz,\ R1 = 120\ \Omega,\ \text{then}\ C_{adj} > 11.1\ \mu F$$

The value for C_{adj} is significantly reduced in applications where the input ripple frequency is high. If used as a post regulator in a switching converter under the following conditions:

$$f_{ripple} = 50\ kHz,\ R1 = 120\ \Omega,\ \text{then}\ C_{adj} > 0.027\ \mu F$$

Protection Diodes

The NCP1117LP family has two internal low impedance diode paths that normally do not require protection when used in the typical regulator applications. The first path connects between V_{out} and V_{in}, and it can withstand a peak surge current of about 15 A. Normal cycling of V_{in} cannot generate a current surge of this magnitude. Only when V_{in} is shorted or crowbarred to ground and C_{out} is greater than 50 μF, it becomes possible for device damage to occur. Under these conditions, diode D1 is required to protect the device. The second path connects between C_{adj} and V_{out}, and it can withstand a peak surge current of about 150 mA. Protection diode D2 is required if the output is shorted or crowbarred to ground and C_{adj} is greater than 1.0 μF.

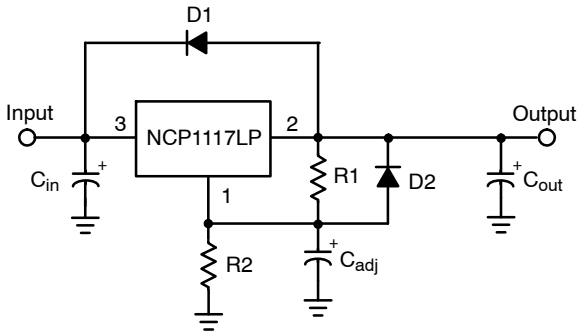


Figure 35. Protection Diode Placement

A combination of protection diodes D1 and D2 may be required in the event that V_{in} is shorted to ground and C_{adj} is greater than 50 μF. The peak current capability stated for the internal diodes are for a time of 100 μs with a junction temperature of 25°C. These values may vary and are to be used as a general guide.

Load Regulation

The NCP1117LP series is capable of providing excellent load regulation; but since these are three terminal devices, only partial remote load sensing is possible. There are two conditions that must be met to achieve the maximum available load regulation performance. The first is that the top side of programming resistor R1 should be connected as close to the regulator case as practicable. This will minimize the voltage drop caused by wiring resistance RW + from appearing in series with reference voltage that is across R1. The second condition is that the ground end of R2 should be connected directly to the load. This allows true Kelvin sensing where the regulator compensates for the voltage drop caused by wiring resistance RW –.

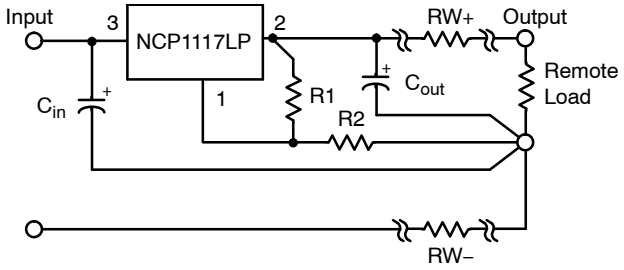


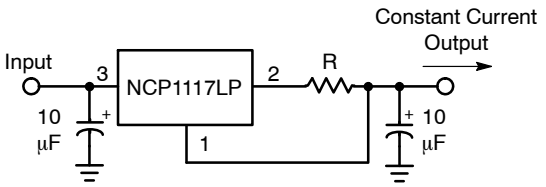
Figure 36. Load Sensing

Thermal Considerations

This series contains an internal thermal limiting circuit that is designed to protect the regulator in the event that the maximum junction temperature is exceeded. When activated, typically at 165°C, the regulator output switches off and then back on as the die cools. As a result, if the device is continuously operated in an overheated condition, the output will appear to be oscillating. This feature provides protection from a catastrophic device failure due to accidental overheating. It is not intended to be used as a substitute for proper heatsinking. The maximum device power dissipation can be calculated by:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The devices are available in surface mount SOT−223 package. This package has an exposed metal tab that is specifically designed to reduce the junction to air thermal resistance, $R_{\theta JA}$, by utilizing the printed circuit board copper as a heat dissipater. Figure 32 shows typical $R_{\theta JA}$ values that can be obtained from a square pattern using economical single sided 1.0 oz and 2.0 oz copper board material. The final product thermal limits should be tested and quantified in order to insure acceptable performance and reliability. The actual $R_{\theta JA}$ can vary considerably from the graphs shown. This will be due to any changes made in the copper aspect ratio of the final layout, adjacent heat sources, and air flow.



$$I_{out} = \frac{V_{ref}}{R} + I_{adj}$$

Figure 37. Constant Current Regulator

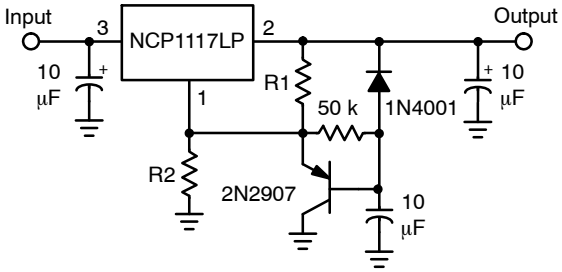
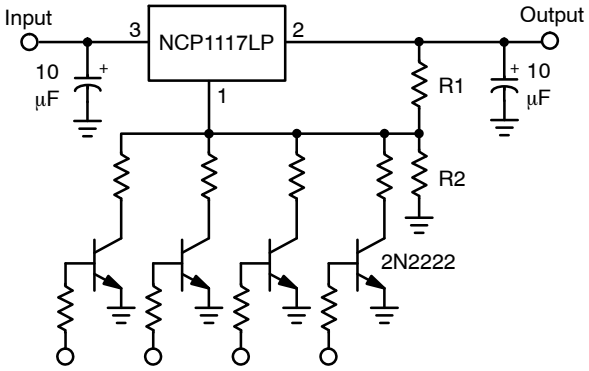


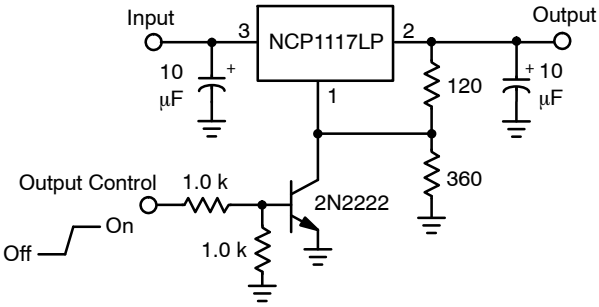
Figure 38. Slow Turn−On Regulator



Output Voltage Control

Resistor R2 sets the maximum output voltage. Each transistor reduces the output voltage when turned on.

Figure 39. Digitally Controlled Regulator



$V_{out(Off)} = V_{ref}$

Figure 40. Regulator with Shutdown

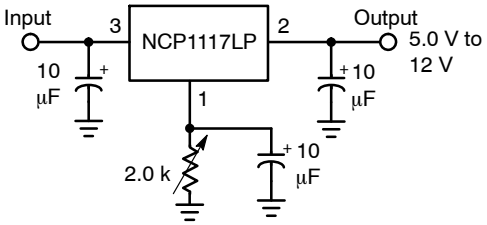


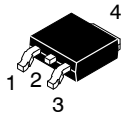
Figure 41. Adjusting Output of Fixed Voltage Regulators

DEVICE ORDERING INFORMATION

Device	Package	Shipping†
NCP1117LPST15T3G	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1117LPST18T3G		
NCP1117LPST25T3G		
NCP1117LPST33T3G		
NCP1117LPST50T3G		
NCP1117LPSTADT3G		
NCP1117LPDT18RKG	DPAK (Pb−Free)	2500 / Tape & Reel
NCP1117LPDT33RKG		
NCP1117LPDTADJRKG		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

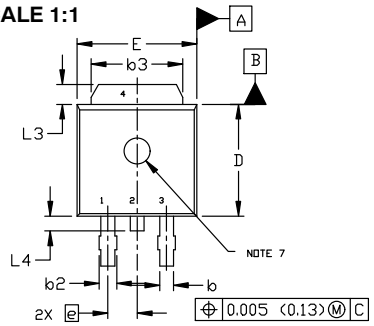
PACKAGE DIMENSIONS



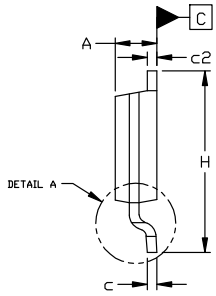
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

SCALE 1:1



TOP VIEW

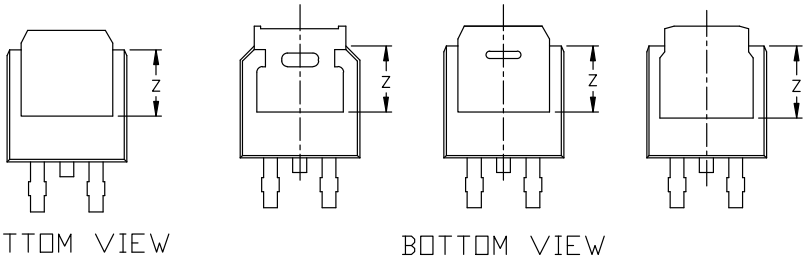


SIDE VIEW

NOTES:

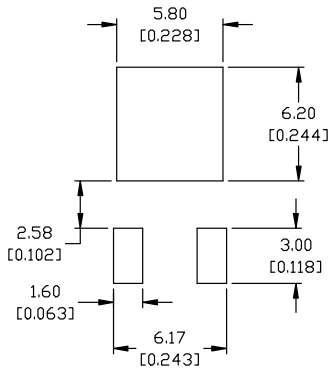
1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---



BOTTOM VIEW

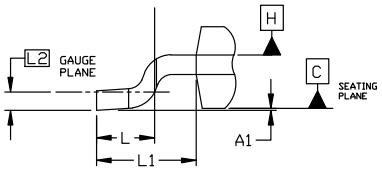
BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT*

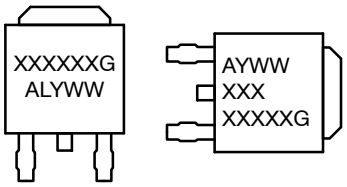
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

ALTERNATE CONSTRUCTIONS



DETAIL A
ROTATED 90° CW

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

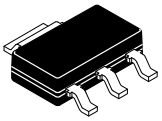
STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

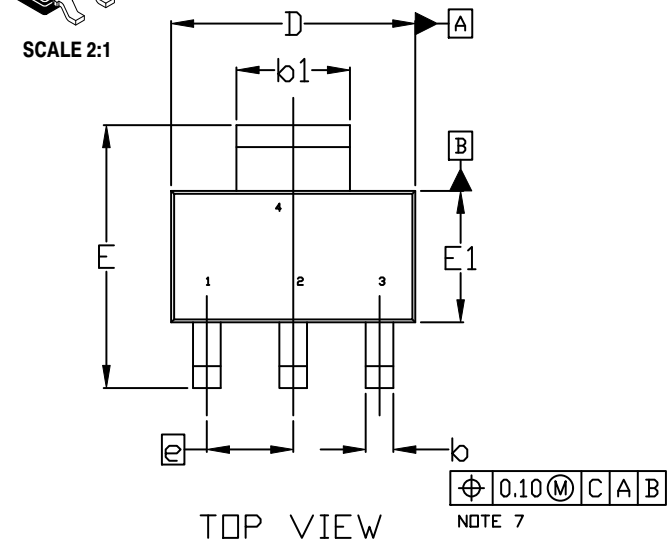
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

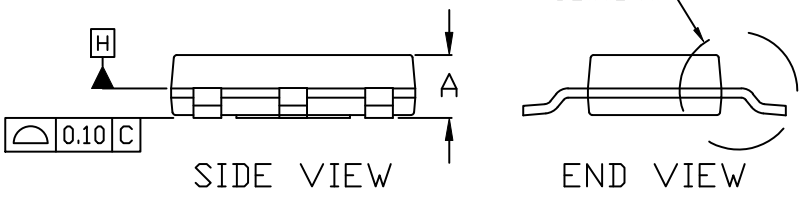
SOT−223
CASE 318H
ISSUE B

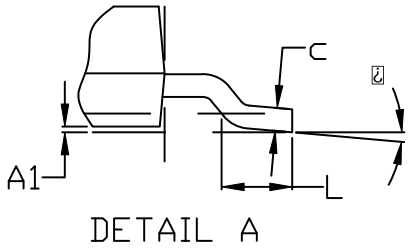
DATE 13 MAY 2020



SCALE 2:1

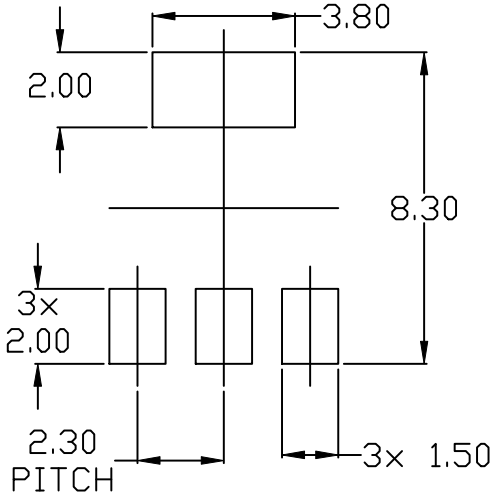






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

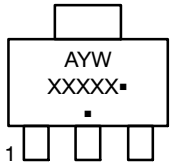
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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