1.5MHz, 800mA, High Efficiency PWM Step-Down DC/DC Converter

General Description

The RT8010B is a high-efficiency Pulse-Width-Modulated (PWM) step-down DC/DC converter. Capable of delivering 800mA output current over a wide input voltage range from 2.5V to 4V, the RT8010B is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources such as cellular phones, PDAs and hand-held devices.

Two operating modes are available including PWM/Low-Dropout autoswitch and shut-down modes. The internal synchronous rectifier with low $R_{DS(ON)}$ dramatically reduces conduction loss at PWM mode. No external Schottky diode is required in practical application.

The RT8010B enters Low-Dropout mode when normal PWM can not provide regulated output voltage by continuously turning on the upper PMOS. The RT8010B enters shut-down mode and consumes less than 0.1μA when EN pin is pulled low.

The switching ripple is easily smoothed-out by small package filtering elements due to a fixed operating frequency of 1.5MHz. This along with small WDFN-8L 2x2 package provides small PCB area application. Other features include soft start, lower internal reference voltage with 2% accuracy, over temperature protection, and over current protection.

Ordering Information

RT8010B □□

- Package Type
  QW : WDFN-8L 2x2 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

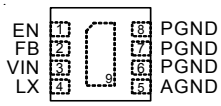
- **2.5V to 4V Input Range**
- **Output Voltage (Adjustable Output From 0.6V to V_{IN})**
- **800mA Output Current**
- **95% Efficiency**
- **No Schottky Diode Required**
- **1.5MHz Fixed Frequency PWM Operation**
- **Small 8-Lead WDFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Mobile Phones
- Personal Information Appliances
- Wireless and DSL Modems
- MP3 Players
- Portable Instruments

Pin Configurations

(TOP VIEW)

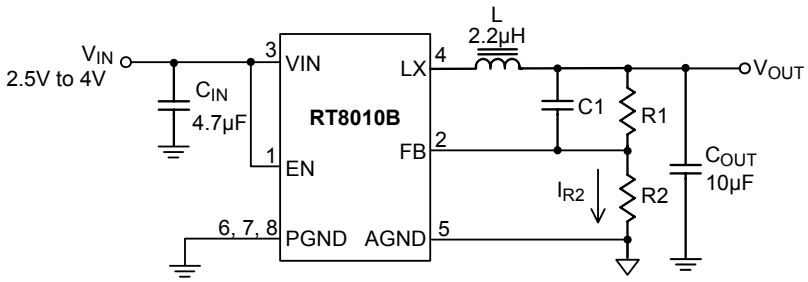


WDFN-8L 2x2

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Typical Application Circuit



$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

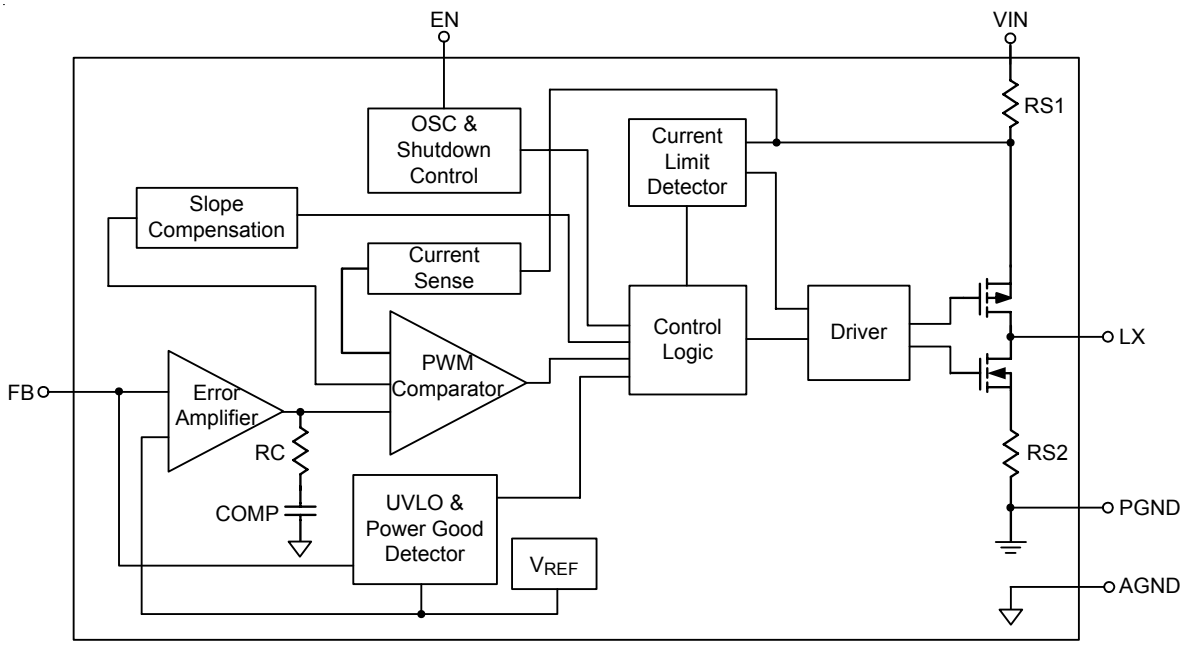
with R2 = 75kΩ to 200kΩ,

and (R1 x C1) should be in the range between $3x10^{-6}$ and $6x10^{-6}$ for component selection.

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Chip Enable (Active High).
2	FB	Feedback Pin.
3	VIN	Power Input.
4	LX	Pin for Switching.
5	AGND	Analog Ground.
6, 7, 8	PGND	Power Ground.
9 (Exposed Pad)	NC	No Internal Connection.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- 6.5V
- EN, FB Pin Voltage ---------- –0.3V to V_{IN}
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-8L 2x2 ---------- 0.606W
- Package Thermal Resistance (Note 2)
  WDFN-8L 2x2, θ_{JA} ---------- 165°C/W
  WDFN-8L 2x2, θ_{JC} ---------- 20°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- Junction Temperature ---------- 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.5V to 4V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, V_{OUT} = 2.5V, V_{REF} = 0.6V, L = 2.2µH, C_{IN} = 4.7µF, C_{OUT} = 10µF, I_{MAX} = 0.8A, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
Input Voltage Range		V_{IN}			2.5	–	4	V
Quiescent Current		I_Q	I_{OUT} = 0mA, V_{FB} = V_{REF} + 5%		--	50	70	µA
Shutdown Current		I_{SHDN}	EN = GND		--	0.1	1	µA
Reference Voltage		V_{REF}	For Adjustable Output Voltage		0.588	0.6	0.612	V
Adjustable Output Range		V_{OUT}	(Note 6)		V_{REF}	–	V_{IN} – 0.2V	V
Output Voltage Accuracy	Adjustable	ΔV_{OUT}	V_{IN} = V_{OUT} + ΔV to 4V (Note 5) 0A < I_{OUT} < 0.8A		–3	–	+3	%
FB Input Current		I_{FB}	V_{FB} = V_{IN}		–50	–	50	nA
P-MOSFET R_{ON}		$R_{DS(ON)\_P}$	I_{OUT} = 200mA	V_{IN} = 3.6V	--	0.28	--	Ω
				V_{IN} = 2.5V	--	0.38	--	
N-MOSFET R_{ON}		$R_{DS(ON)\_N}$	I_{OUT} = 200mA	V_{IN} = 3.6V	--	0.25	--	Ω
				V_{IN} = 2.5V	--	0.35	--	
P-Channel Current Limit		I_{LIM_P}	V_{IN} = 2.5V to 4V		1.2	1.5	--	A
EN High-Level Input Voltage		V_{EN_H}	V_{IN} = 2.5V to 4V		1.5	–	--	V
EN Low-Level Input Voltage		V_{EN_L}	V_{IN} = 2.5V to 4V		--	–	0.4	V
Under Voltage Lockout Threshold		UVLO			--	1.8	--	V
Hysteresis					--	0.1	--	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator Frequency	f_{OSC}	V_{IN} = 3.6V, I_{OUT} = 100mA	1.2	1.5	1.8	MHz
Thermal Shutdown Temperature	T_{SD}		--	160	--	°C
Max. Duty Cycle			100	--	--	%
LX Leakage Current		V_{IN} = 3.6V, V_{LX} = 0V or V_{LX} = 3.6V	−1	--	1	μA

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad of the package.

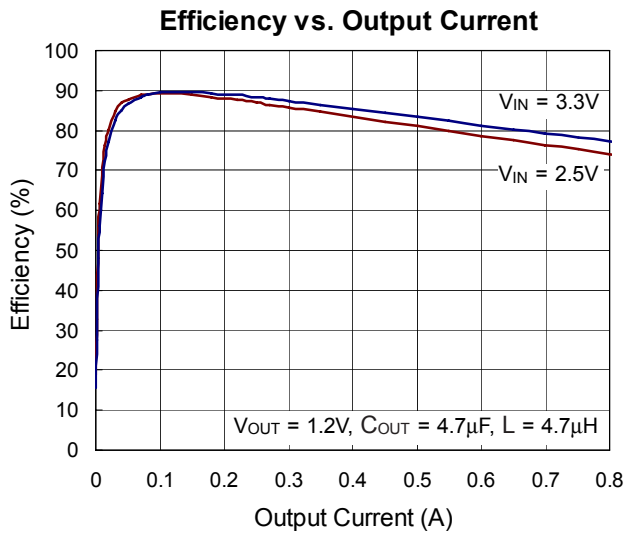
Note 3 Devices are ESD sensitive. Handling precaution is recommended.

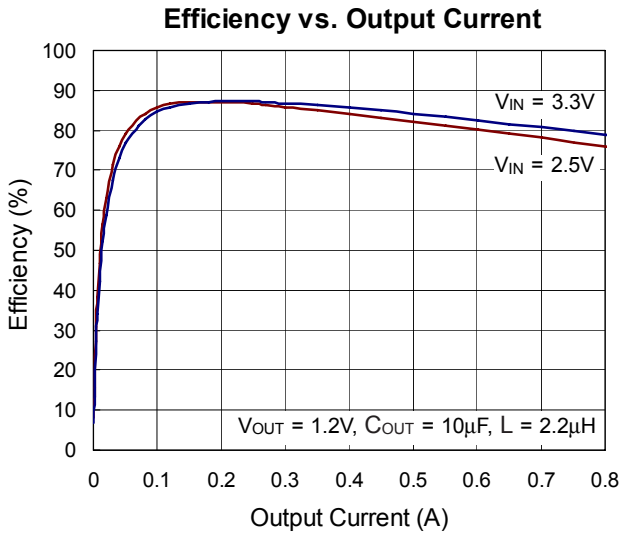
Note 4. The device is not guaranteed to function outside its operating conditions.

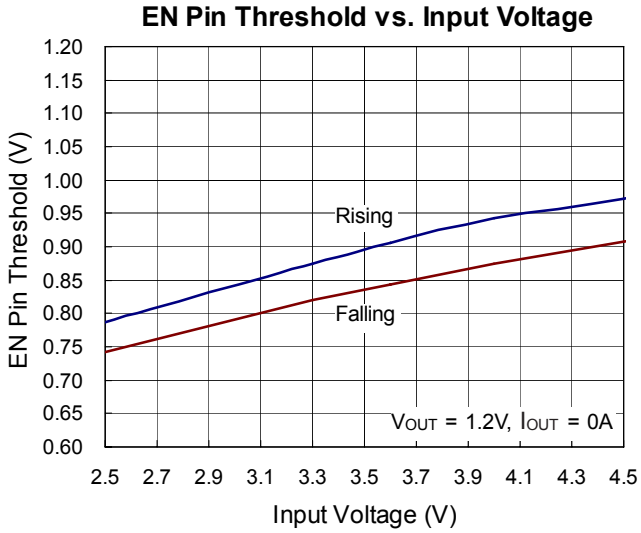
Note 5. $\Delta V = I_{OUT} \times P_{RDS(ON)}$

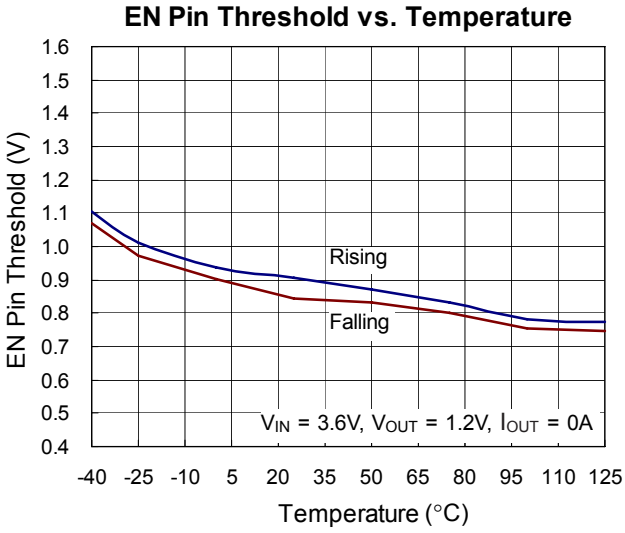
Note 6. Guarantee by design.

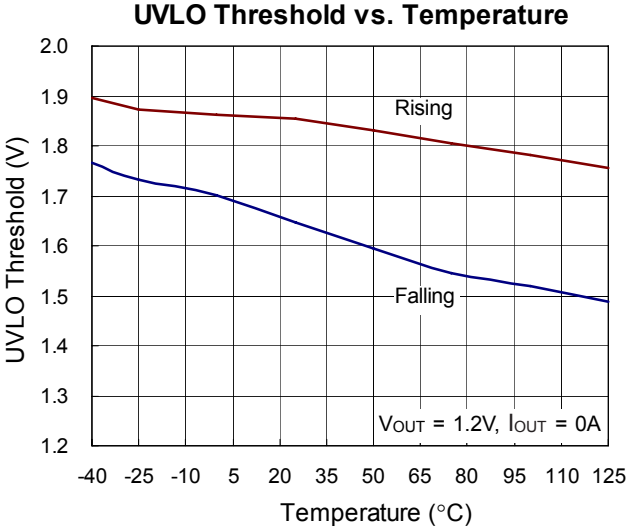
Typical Operating Characteristics

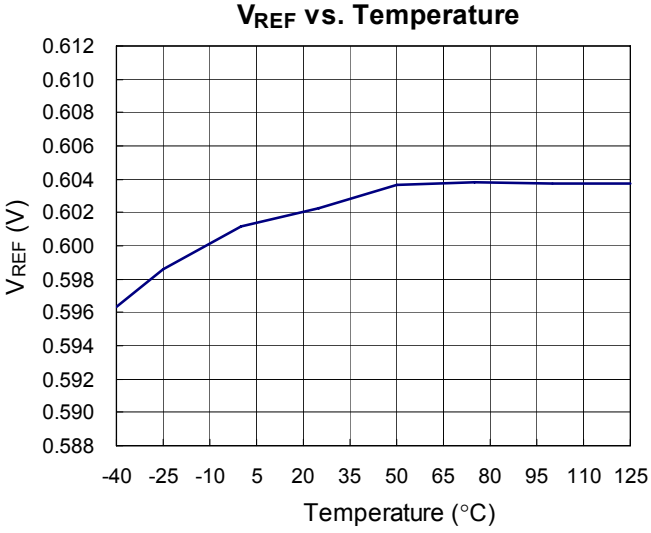




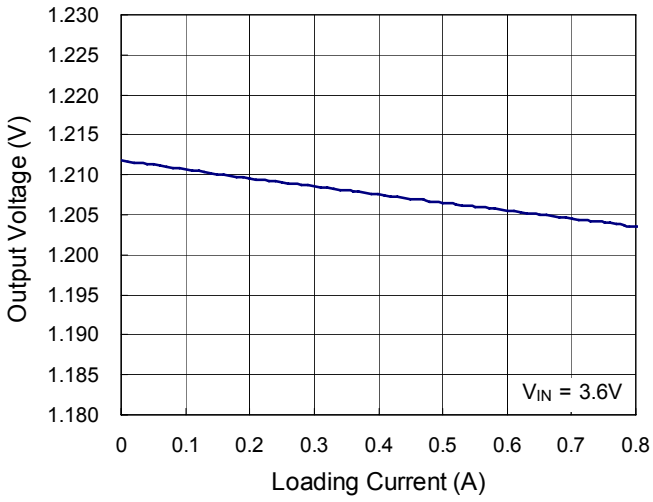




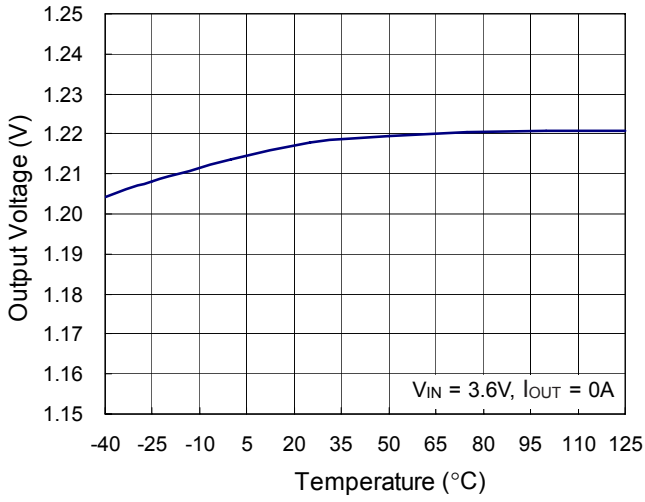




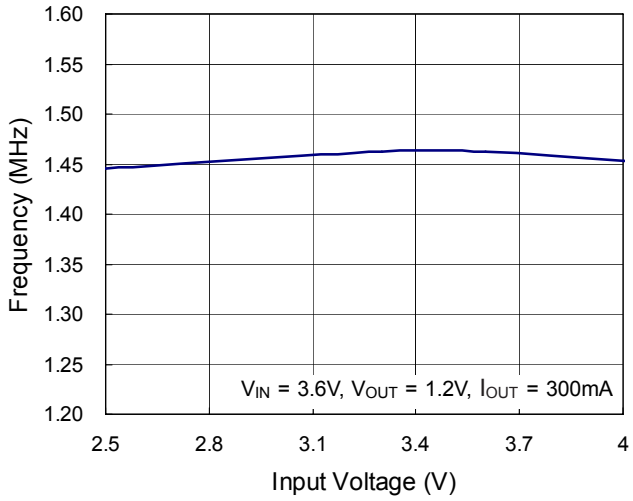
Output Voltage vs. Loading Current



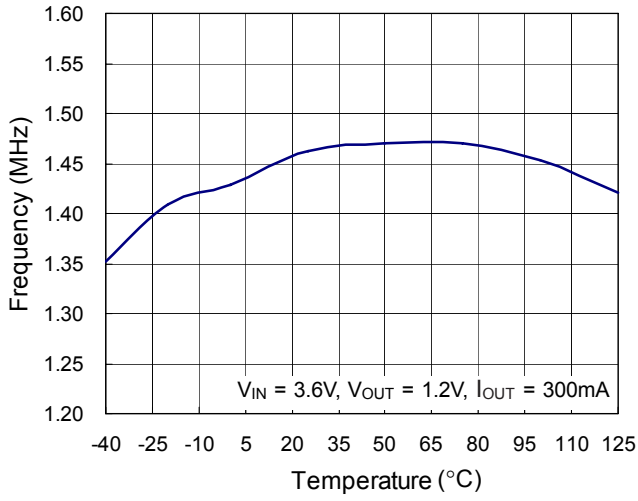
Output Voltage vs. Temperature



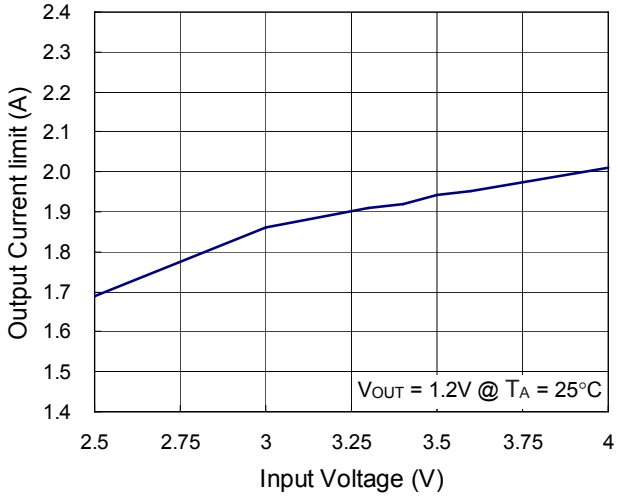
Frequency vs. Input Voltage



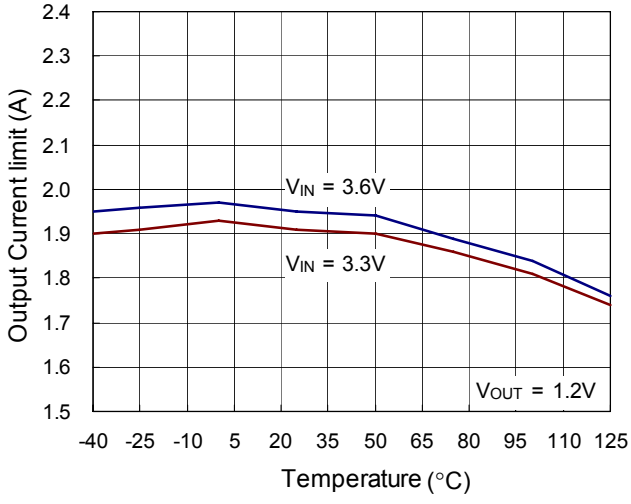
Frequency vs. Temperature



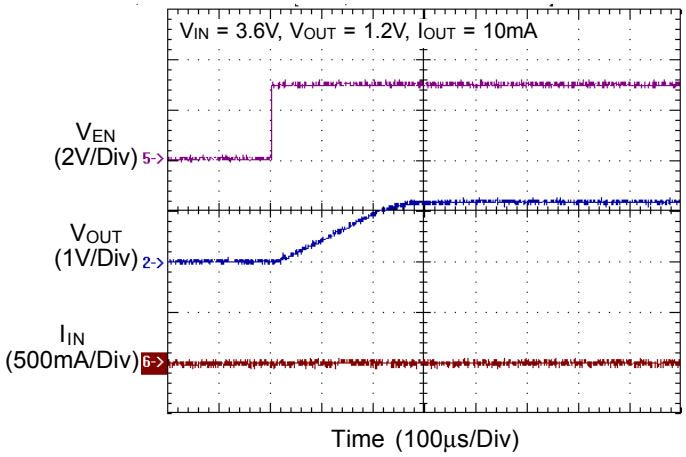
Output Current Limit vs. Input Voltage



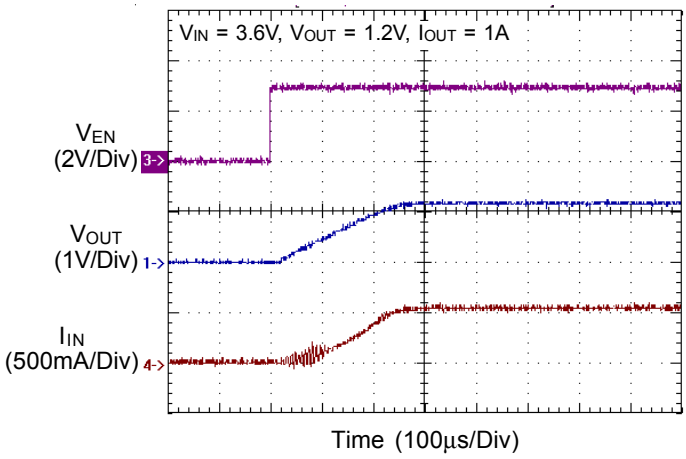
Output Current Limit vs. Temperature



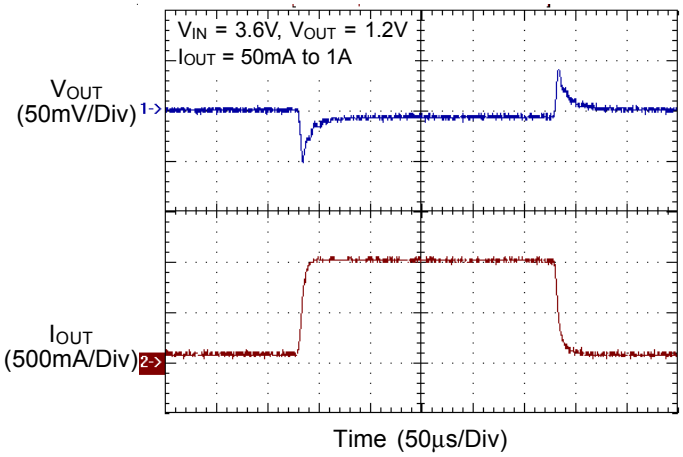
Power On from EN



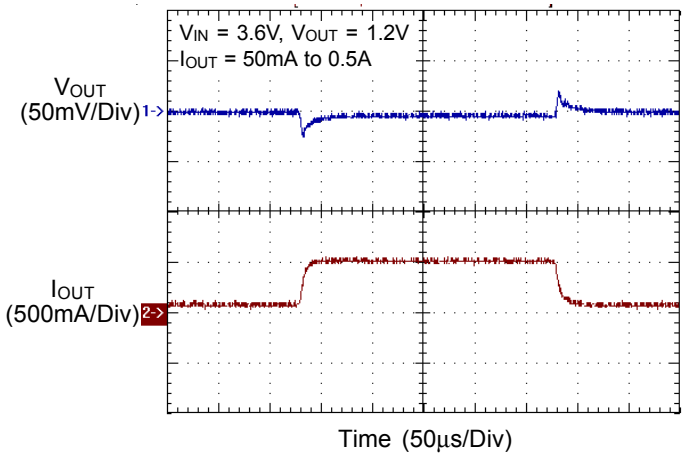
Power On from EN



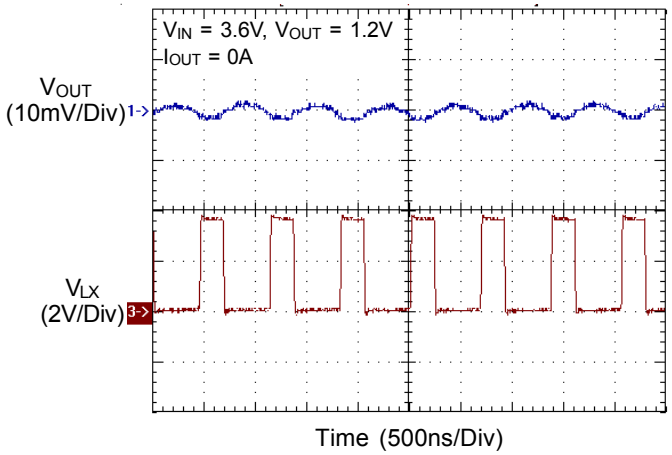
Load Transient Response



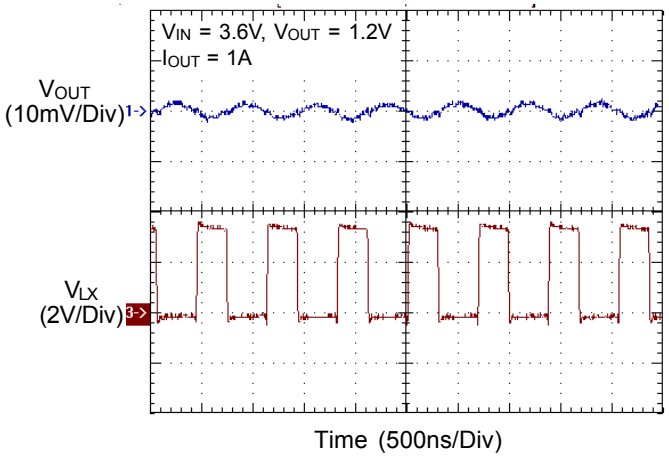
Load Transient Response



Output Ripple Voltage



Output Ripple Voltage



Applications Information

The basic RT8010B application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta IL(MAX)}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally can not afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or mollypermalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss reduction and saturation prevention. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/ current and price/current relationship of an inductor.

Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs size requirements and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

The output ripple is the highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output Voltage Programming

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 4.

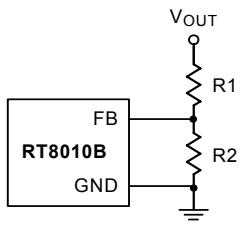


Figure 4. Setting the Output Voltage

For adjustable voltage mode, the output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF}(1+\frac{R1}{R2})$$

where V_{REF} is the internal reference voltage (0.6V typ.)

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as :

Efficiency = 100% – (L1+ L2+ L3+ ...)

where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses : VIN quiescent current and I^2R losses.

The VIN quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The VIN quiescent current appears due to two factors including : the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge ΔQ moves from V_{IN} to ground.

The resulting $\Delta Q/\Delta t$ is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode,

$I_{GATECHG} = f(Q_T+Q_B)$

where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L.

In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the LX pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows :

$R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1-DC)$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8010B, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WDFN-8L 2x2 packages, the thermal resistance θ_{JA} is 165°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)} = (125°C - 25°C) / (165°C/W) = 0.606W$ for WDFN-8L 2x2 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}.

For RT8010B packages, the Figure 5 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

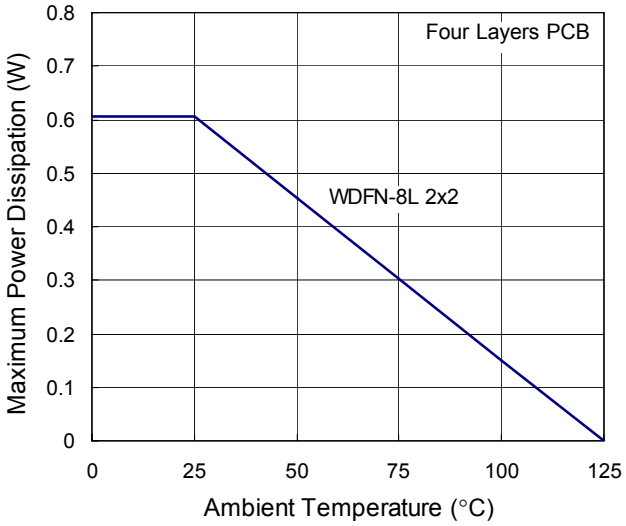


Figure 5. Derating Curves for RT8010B Package

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Layout Considerations

Follow the PCB layout guidelines for optimal performance of RT8010B.

- Put the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8010B.
- Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

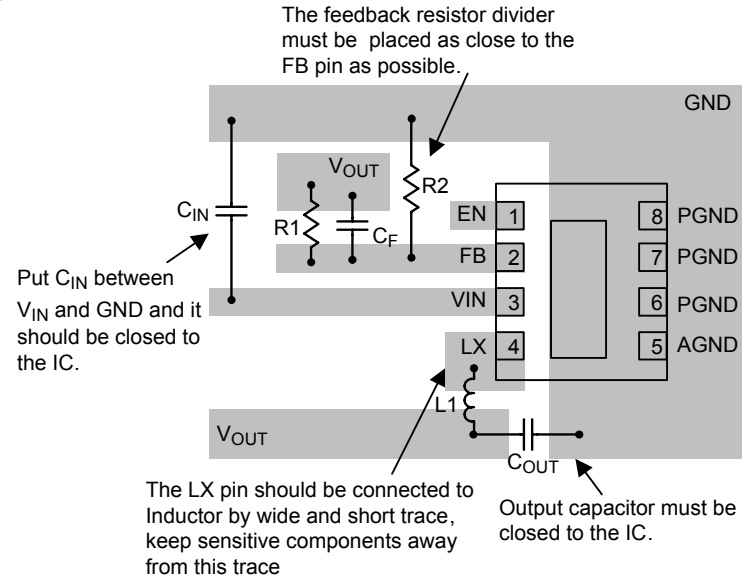


Figure 6

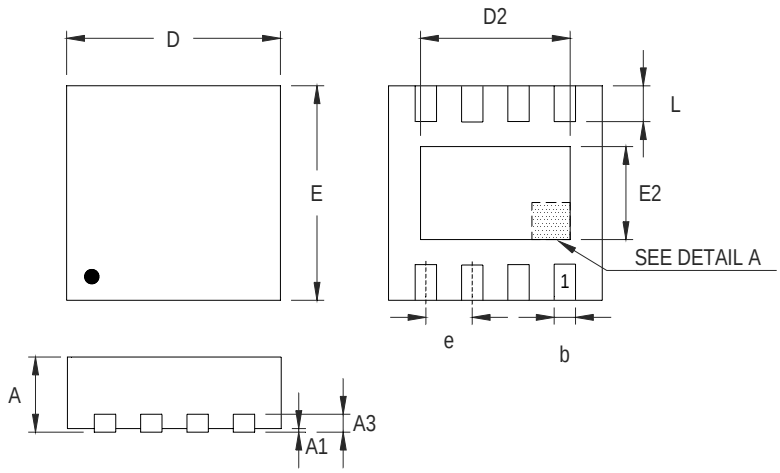
Table 1. Recommended Inductors

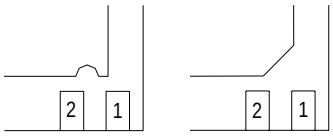
Supplier	Inductance (uH)	Current Rating (mA)	DCR (mΩ)	Dimensions (mm)	Series
TAIYO YUDEN	2.2	1480	60	3.00 x 3.00 x 1.50	NR 3015
GOTREND	2.2	1500	58	3.85 x 3.85 x 1.80	GTSD32
Sumida	2.2	1500	75	4.50 x 3.20 x 1.55	CDRH2D14
Sumida	4.7	1000	135	4.50 x 3.20 x 1.55	CDRH2D14
TAIYO YUDEN	4.7	1020	120	3.00 x 3.00 x 1.50	NR 3015
GOTREND	4.7	1100	146	3.85 x 3.85 x 1.80	GTSD32

Table 2. Recommended Capacitors for C_{IN} and C_{OUT}

Supplier	Capacitance (uF)	Package	Part Number
TDK	4.7	603	C1608JB0J475M
MURATA	4.7	603	GRM188R60J475KE19
TAIYO YUDEN	4.7	603	JMK107BJ475RA
TAIYO YUDEN	10	603	JMK107BJ106MA
TDK	10	805	C2012JB0J106M
MURATA	10	805	GRM219R60J106ME19
MURATA	10	805	GRM219R60J106KE19
TAIYO YUDEN	10	805	JMK212BJ106RD

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 8L DFN 2x2 Package

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