

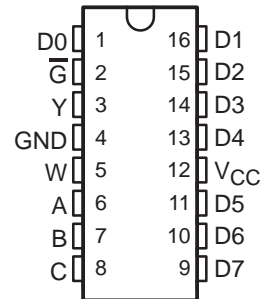
# 74ACT11251

## 1 OF 8 DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS076 – OCTOBER 1989 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- 3-State Outputs Interface Directly With System Bus
- Performs Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted Data
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, and Standard Plastic 300-mil DIPs

D OR N PACKAGE  
(TOP VIEW)



### description

This data selector/multiplexer contains full binary decoding to select one-of-eight data sources and features strobe-controlled complementary 3-state outputs.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the signal enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe ( $\overline{G}$ ). The outputs are disabled when  $\overline{G}$  is high.

The 74ACT11251 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

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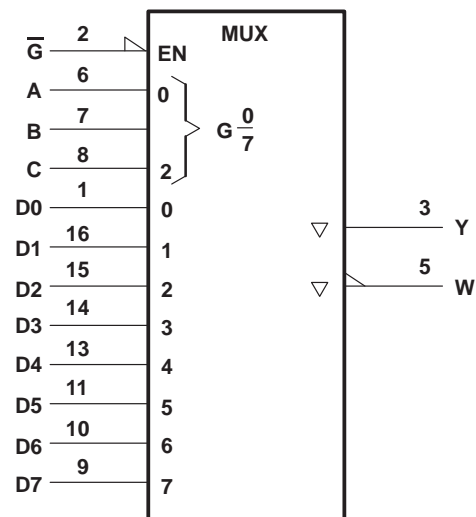
FAMILY NAME

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE $\overline{G}$	Y	W
C	B	A			
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

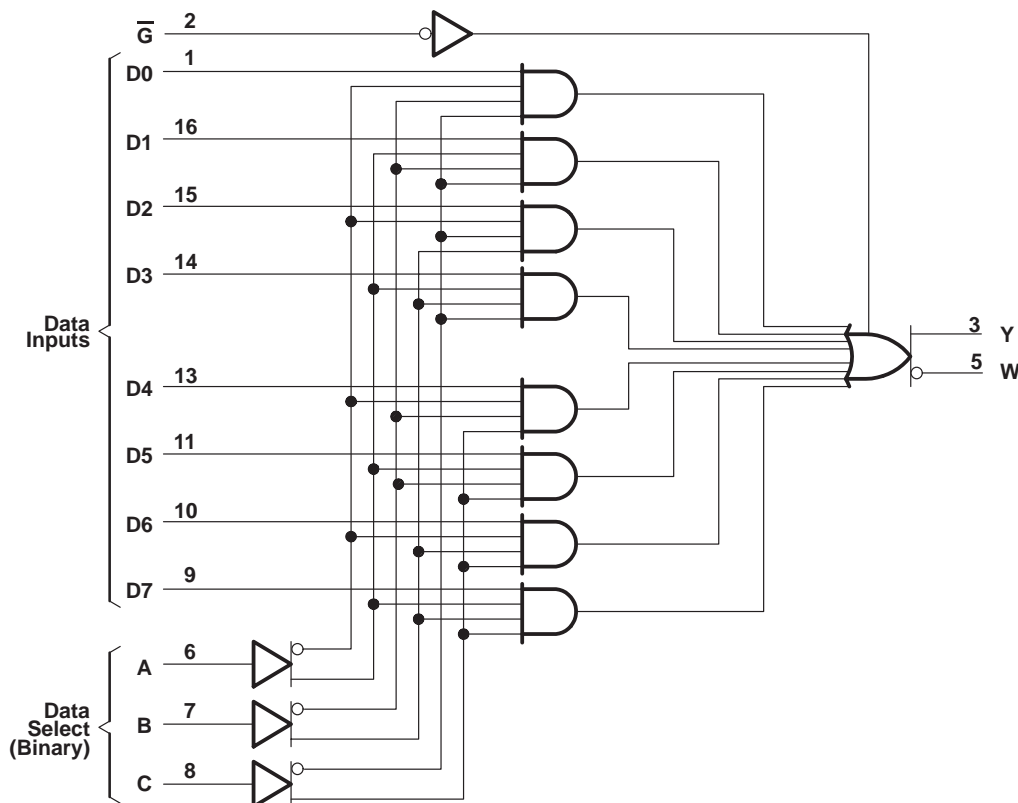
H = high level, L = low level, X = irrelevant.  
D0, D1,...D7 = the level of the respective D input

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**recommended operating conditions**

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		V
$V_{IL}$ Low-level input voltage		0.8	V
$V_I$ Input voltage	0	$V_{CC}$	V
$V_O$ Output voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current		–24	mA
$I_{OL}$ Low-level output current		24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0	10	ns/V
$T_A$ Operating free-air temperature	–40	85	°C

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**FAMILY NAME**

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = – 50 µA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I <sub>OH</sub> = – 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I <sub>OH</sub> = – 75 mA†	5.5 V				3.85		
V <sub>OL</sub>	I <sub>OL</sub> = – 50 µA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I <sub>OL</sub> = – 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I <sub>OL</sub> = 75 mA†	5.5 V					1.65	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.5		±5	µA
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			8		80	µA
ΔI <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			0.9		1	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		3.5				pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		8				pF

† Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V<sub>CC</sub>.

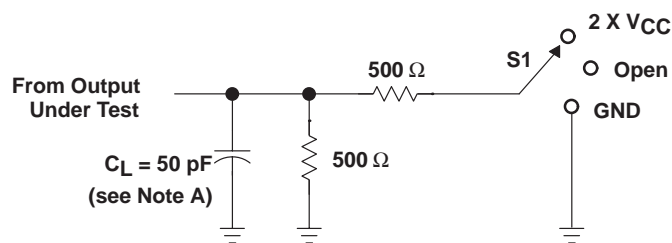
**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t <sub>PLH</sub>	A, B, or C	Y	3.2	6.8	10.2	3.2	11.4	ns
t <sub>PHL</sub>			2.7	6.7	9.5	2.7	10.5	
t <sub>PLH</sub>	A, B, or C	W	2.5	6.3	8.8	2.5	9.8	ns
t <sub>PHL</sub>			2.8	6.3	9.7	2.8	10.8	
t <sub>PLH</sub>	Any D	Y	3	5.7	7.8	3	8.7	ns
t <sub>PHL</sub>			2	5.2	7.9	2	8.6	
t <sub>PLH</sub>	Any D	W	1.7	4.7	7.1	1.7	7.8	ns
t <sub>PHL</sub>			2.7	5.1	7.2	2.7	8	
t <sub>PZH</sub>	$\overline{G}$	Y	1.3	3.7	6.2	1.3	6.8	ns
t <sub>PZL</sub>			1.3	4	6	1.3	6.8	
t <sub>PZH</sub>	$\overline{G}$	W	1	4.4	6.4	1	7	ns
t <sub>PZL</sub>			1.3	4.1	5.8	1.3	6.4	
t <sub>PHZ</sub>	$\overline{G}$	Y	4.1	5.7	7.6	4.1	8.1	ns
t <sub>PLZ</sub>			3.1	4	6.6	3.1	6.9	
t <sub>PHZ</sub>	$\overline{G}$	W	4.1	5.7	7.7	4.1	8.2	ns
t <sub>PLZ</sub>			3.2	4.1	6.6	3.2	6.9	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

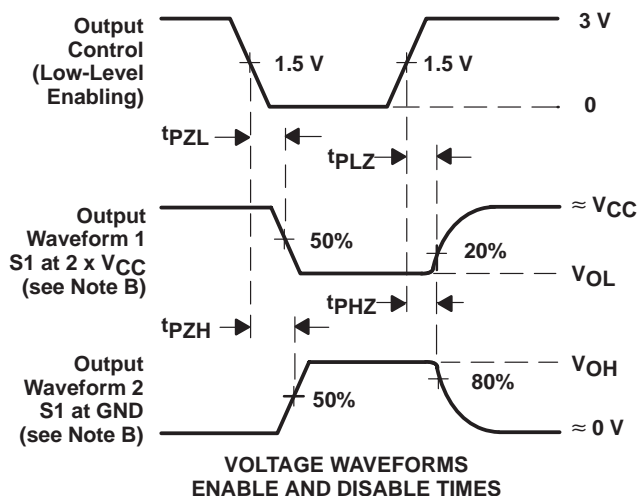
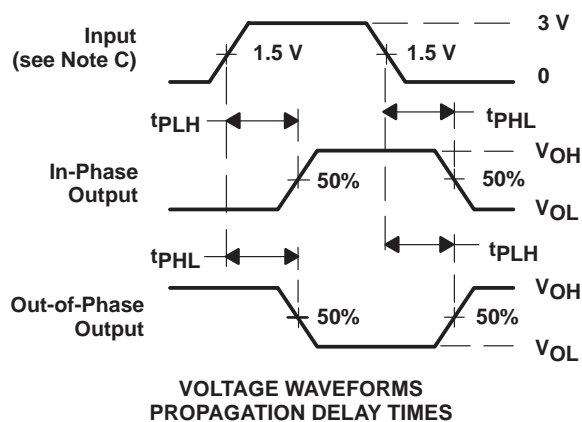
PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	60	pF
		Outputs disabled		16	

## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	OPEN
$t_{PLZ}/t_{PZL}$	2 x $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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