

Spread Spectrum Clock Generator

Features

- 4 to 32 MHz Input Frequency Range
- 4 to 128 MHz Output Frequency Range
- Accepts Clock, Crystal, and Resonator Inputs
- 1x, 2x, and 4x frequency multiplication:
 - CY25811: 1x; CY25812: 2x; CY25814: 4x
- Center and Down Spread Modulation
- Low Power Dissipation:
 - 3.3V = 52 mW - typ at 6 MHz
 - 3.3V = 60 mW - typ at 12 MHz
 - 3.3V = 72 mW - typ at 24 MHz
- Low Cycle to Cycle Jitter:
 - 8 MHz = 480 ps-max
 - 16 MHz = 400 ps-max
 - 32 MHz = 450 ps-max
- Available in 8-pin SOIC and TSSOP Packages
- Commercial and Industrial Temperature Ranges

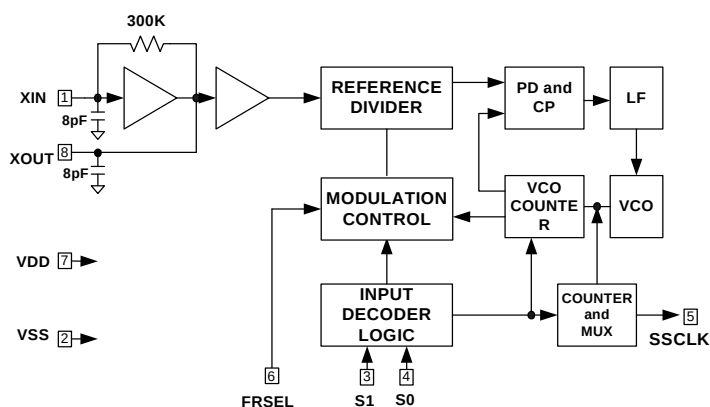
Applications

- Printers and MFPs
- LCD panels
- Digital copiers
- PDAs
- CD-ROM, VCD, and DVD
- Networking, LAN, and WAN
- Scanners
- Modems
- Embedded digital systems

Benefits

- Peak EMI reduction by 8 to 16 dB
- Fast time to market
- Cost reduction

Logic Block Diagram



Pinouts

Figure 1. Pin Configuration – 8 Pin SOIC/TSSOP

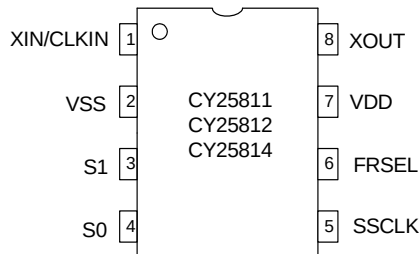


Table 1. Pin Definition

Pin No.	Name	Type	Description
1	Xin/CLK		Crystal, Ceramic Resonator or Clock Input Pin
2	VSS		Power Supply Ground.
3	S1		Digital Spread% Control Pin. 3-Level input (H-M-L). Default = M.
4	S0		Digital Spread% Control Pin. 3-Level input (H-M-L). Default = M.
5	SSCLK		Spread Spectrum Output Clock.
6	FRSEL		Input Frequency Range Selection Digital Control Input. 3-Level input (H-M-L). Default = M.
7	VDD		Positive Power Supply.
8	XOUT		Crystal or Ceramic Resonator Output Pin.

Functional Description

The CY25811/12/14 products are Spread Spectrum Clock Generator (SSCG) ICs used for the purpose of reducing electromagnetic interference (EMI) found in today's high speed digital electronic systems.

The devices use a Cypress proprietary phase-locked loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the input clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies is greatly reduced.

This reduction in radiated energy significantly reduces the cost of complying with regulatory agency requirements and improves time to market without degrading system performance.

The input frequency range is 4 to 32 MHz and accepts clock, crystal and ceramic resonator inputs. The output clock can be selected to produce 1x, 2x, or 4x multiplication of the input frequency with Spread Spectrum Frequency Modulation.

The use of 2x or 4x frequency multiplication eliminates the need for higher order crystals and enables you to generate up to 128 MHz Spread Spectrum Clock (SSC) by using only first order crystals. This reduces the cost while improving the system clock accuracy, performance, and complexity.

You select the Center Spread or Down Spread frequency modulation based on four discrete values of Spread % for each Spread mode with the option of a Non Spread mode for system test and verification purposes.

The CY25811/12/14 products are available in an 8 pin SOIC -150 mil package with a commercial operating temperature range of 0 to 70°C and Industrial Temperature range of -40 to 85°C. Refer to CY25568 for multiple clock output options such as modulated and unmodulated clock outputs or Power-down function.

Input Frequency Range and Selection

The CY25811/12/14 input frequency range is 4 to 32 MHz. This range is divided into three segments and controlled by a 3-Level FRSEL pin as given in [Table 2](#).

Table 2. Input Frequency Selection

FRSEL	Input Frequency Range
0	4.0 to 8.0 MHz
1	8.0 to 16.0 MHz
M	16.0 to 32.0 MHz

Spread Percentage Selection

The CY25811/12/14 SSCG products provide Center-Spread, Down-Spread, and No-Spread functions. The amount of Spread percentage is selected using 3-Level. S0 and S1 digital inputs and Spread percent values are given in [Table 3](#).

Table 3. Spread Percent Selection

XIN (MHz)	FRSEL	S1 = 0 S0 = 0	S1 = 0 S0 = M	S1 = 0 S0 = 1	S1 = M S0 = 0	S1 = 1 S0 = 1	S1 = 1 S0 = 0	S1 = M S0 = 1	S1 = 1 S0 = M	S1 = M S0 = M
		Center (%)	Center (%)	Center (%)	Center (%)	Down (%)	Down (%)	Down (%)	Down (%)	No Spread
4-5	0	±1.4	±1.2	±0.6	±0.5	-3.0	-2.2	-1.9	-0.7	0
5-6	0	±1.3	±1.1	±0.5	±0.4	-2.7	-1.9	-1.7	-0.6	0
6-7	0	±1.2	±0.9	±0.5	±0.4	-2.5	-1.8	-1.5	-0.6	0
7-8	0	±1.1	±0.9	±0.4	±0.3	-2.3	-1.7	-1.4	-0.5	0
8-10	1	±1.4	±1.2	±0.6	±0.5	-3.0	-2.2	-1.9	-0.7	0
10-12	1	±1.3	±1.1	±0.5	±0.4	-2.7	-1.9	-1.7	-0.6	0
12-14	1	±1.2	±0.9	±0.5	±0.4	-2.5	-1.8	-1.5	-0.6	0
14-16	1	±1.1	±0.9	±0.4	±0.3	-2.3	-1.7	-1.4	-0.5	0
16-20	M	±1.4	±1.2	±0.6	±0.5	-3.0	-2.2	-1.9	-0.7	0
20-24	M	±1.3	±1.1	±0.5	±0.4	-2.7	-1.9	-1.7	-0.6	0
24-28	M	±1.2	±0.9	±0.5	±0.4	-2.5	-1.8	-1.5	-0.6	0
28-32	M	±1.1	±0.9	±0.4	±0.3	-2.3	-1.7	-1.4	-0.5	0

3-Level Digital Inputs

S0, S1, and FRSEL digital inputs are designed to sense 3 different logic levels designated as High “1”, Low “0”, and Middle “M”. With this 3-Level digital input logic, the 3-Level Logic detects nine different logic states.

S0, S1, and FRSEL pins include an on chip 20K (10K and 10K) resistor divider. No external application resistors are needed to implement the 3-Level logic levels as shown here:

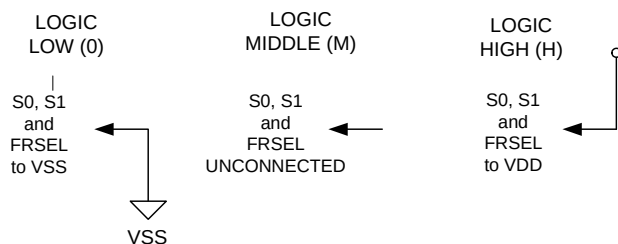
Logic Level “0”: 3-Level logic pin connected to GND.

Logic Level “M”: 3-Level logic pin left floating (no connection).

Logic Level “1”: 3-Level logic pin connected to V_{DD}.

[Figure 2](#) illustrates how to implement 3-Level Logic.

Figure 2. 3-Level Logic



Modulation Rate

SSCGs use frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (f_{max}), and minimum frequency of the clock (f_{min}) determine this band of frequencies. The time required to transition from f_{min} to f_{max} and back to f_{min} is the period of the Modulation Rate. The Modulation Rate of SSCG clocks are generally referred to in terms of frequency, or:

$$f_{\text{mod}} = 1/T_{\text{mod}}$$

The input clock frequency, f_{in}, and the internal divider determine the Modulation Rate.

In CY25811/2/4 devices, the (Spread Spectrum) modulation Rate, f_{mod}, is given by the following formula:

$$f_{\text{mod}} = f_{\text{in}}/DR$$

Here f_{mod} is the Modulation Rate, f_{in} is the Input Frequency, and DR is the Divider Ratio as given in [Table 4](#). Note that Input Frequency Range is set by FRSEL.

Table 4. Modulation Rate Divider Ratios

FRSEL	Input Frequency Range (MHz)	Divider Ratio (DR)
0	4 to 8	128
1	8 to 16	256
M	16 to 32	512

Input and Output Frequency Selection

The relationship between input frequency and output frequency in device selection and FRSEL setting is given in [Table 5](#). As shown, the input frequency range is selected by FRSEL and is the same for CY25811, CY25812, and CY25814. The selection of CY25811 (1x), CY25812 (2x), or CY25814 (4x) determines the frequency multiplication at the output (SSCLK, Pin 5) with respect to input frequency (XIN, Pin-1).

Table 5. Input and Output Frequency Selection

Input Frequency Range (MHz)	FRSEL	Product	Multiplication	Output Frequency Range (MHz)
4 to 8	0	CY25811	1x	4 to 8
8 to 16	1	CY25811	1x	8 to 16
16 to 32	M	CY25811	1x	16 to 32
4 to 8	0	CY25812	2x	8 to 16
8 to 16	1	CY25812	2x	16 to 32
16 to 32	M	CY25812	2x	32 to 64
4 to 8	0	CY25814	4x	16 to 32
8 to 16	1	CY25814	4x	32 to 64
16 to 32	M	CY25814	4x	64 to 128

Absolute Maximum Conditions

(Both Commercial and Industrial Grades)^[1,2]

Parameter	Description	Condition	Min	Max	Unit
V _{DD}	Supply Voltage		−0.5	4.6	V
V _{IN}	Input Voltage	Relative to V _{SS}	−0.5	V _{DD} + 0.5	VDC
T _S	Temperature, Storage	Non Functional	−65	150	°C
T _{A1}	Temperature, Operating Ambient	Functional, C-Grade	0	70	°C
T _{A2}	Temperature, Operating Ambient	Functional, I-Grade	−40	85	°C
T _J	Temperature, Junction	Functional	−	150	°C
ESD _{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	−	V
UL-94	Flammability Rating	at 1/8 in.	V−0		
MSL	Moisture Sensitivity Level		1		

DC Electrical Specifications

(Commercial Grade)

Parameter	Description	Condition	Min	Max	Unit
V _{DD}	3.3V Operating Voltage	3.3V ± 10%	2.97	3.63	V
V _{IL}	Input Low Voltage	S0, S1 and FRSEL Inputs	0	0.15V _{DD}	V
V _{IM}	Input Middle Voltage	S0, S1 and FRSEL Inputs	0.40V _{DD}	0.60V _{DD}	V
V _{IH}	Input High Voltage	S0, S1 and FRSEL Inputs	0.85V _{DD}	V _{DD}	V
V _{OL1}	Output Low Voltage	I _{OL} = 4 ma, SSCLK Output	−	0.4	V
V _{OL2}	Output Low Voltage	I _{OL} = 10 ma, SSCLK Output	−	1.2	V
V _{OH1}	Output High Voltage	I _{OH} = 4 ma, SSCLK Output	2.4	−	V
V _{OH2}	Output High Voltage	I _{OH} = 6 ma, SSCLK Output	2.0	−	V
C _{IN1}	Input Pin Capacitance	XIN (Pin 1) and XOUT (Pin 8)	3.5	9.0	pF
C _{IN2}	Input Pin Capacitance	All Digital Inputs	2.8	6.0	pF
C _L	Output Load Capacitor	SSCLK Output	−	15	pF
I _{DD1}	Dynamic Supply Current	Fin = 12 MHz, no load	−	28	mA
I _{DD2}	Dynamic Supply Current	Fin = 24 MHz, no load	−	33	mA
I _{DD3}	Dynamic Supply Current	Fin = 32 MHz, no load	−	40	mA

Notes

1. Operation at any Absolute Maximum Rating is not implied.
2. Single Power Supply: The voltage on any input or I/O pin cannot exceed the power pin during power up.

AC Electrical Specifications

(Commercial Grade)

Parameter	Description	Condition	Min	Max	Unit
F_{IN}	Input Frequency Range	Clock, Crystal, or Ceramic Resonator Input	4	32	MHz
T_{R1}	Clock Rise Time	SSCLK, CY25811 and CY25812	2.0	5.0	ns
T_{F1}	Clock Fall Time	SSCLK, CY25811 and CY25812	1.6	4.4	ns
T_{R2}	Clock Rise Time	SSCLK, only CY25814 when FRSEL = M	1.0	2.2	ns
T_{F2}	Clock Fall Time	SSCLK, only CY25814 when FRSEL = M	0.8	2.2	ns
T_{DCIN}	Input Clock Duty Cycle	XIN	40	60	%
T_{DCOUT}	Output Clock Duty Cycle	SSCLK	40	60	%
T_{CCJ1}	Cycle to Cycle Jitter, Spread on	$F_{in} = 4$ MHz, $F_{out} = 4$ MHz, CY25811	–	800	ps
T_{CCJ2}	Cycle to Cycle Jitter, Spread on	$F_{in} = 8$ MHz, $F_{out} = 8$ MHz, CY25811	–	480	ps
T_{CCJ3}	Cycle to Cycle Jitter, Spread on	$F_{in} = 8$ MHz, $F_{out} = 16$ MHz, CY25812	–	400	ps
T_{CCJ4}	Cycle to Cycle Jitter, Spread on	$F_{in} = 16$ MHz, $F_{out} = 32$ MHz, CY25812	–	450	ps
T_{CCJ5}	Cycle to Cycle Jitter, Spread on	$F_{in} = 16$ MHz, $F_{out} = 64$ MHz, CY25814	–	550	ps
T_{CCJ6}	Cycle to Cycle Jitter, Spread on	$F_{in} = 32$ MHz, $F_{out} = 128$ MHz, CY25814	–	380	ps
T_{SU}	PLL Lock Time	From $V_{DD} = 3.0V$ to valid SSCLK	–	3	ms

DC Electrical Specifications

(Industrial Grade)

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	3.3V Operating Voltage	$3.3V \pm 5\%$	3.135	3.465	V
V_{IL}	Input Low Voltage	S0, S1 and FRSEL Inputs	0	$0.13V_{DD}$	V
V_{IM}	Input Middle Voltage	S0, S1 and FRSEL Inputs	$0.40V_{DD}$	$0.60V_{DD}$	V
V_{IH}	Input High Voltage	S0, S1 and FRSEL Inputs	$0.85V_{DD}$	V_{DD}	V
V_{OL1}	Output Low Voltage	$I_{OL} = 4$ ma, SSCLK Output	–	0.4	V
V_{OL2}	Output Low Voltage	$I_{OL} = 10$ ma, SSCLK Output	–	1.2	V
V_{OH1}	Output High Voltage	$I_{OH} = 4$ ma, SSCLK Output	2.4	–	V
V_{OH2}	Output High Voltage	$I_{OH} = 6$ ma, SSCLK Output	2.0	–	V
C_{IN1}	Input Pin Capacitance	XIN (Pin 1) and XOUT (Pin 8)	3.5	9.0	pF
C_{IN2}	Input Pin Capacitance	All Digital Inputs	2.8	6.0	pF
C_L	Output Load Capacitor	SSCLK Output	–	15	pF
I_{DD1}	Dynamic Supply Current	$F_{in} = 12$ MHz, no load	–	28	mA
I_{DD2}	Dynamic Supply Current	$F_{in} = 24$ MHz, no load	–	33	mA
I_{DD3}	Dynamic Supply Current	$F_{in} = 32$ MHz, no load	–	41	mA

AC Electrical Specifications

(Industrial Grade)

Parameter	Description	Condition	Min	Max	Unit
F_{IN}	Input Frequency Range	Clock, Crystal or Ceramic Resonator Input	4	32	MHz
T_{R1}	Clock Rise Time	SSCLK, CY25811, and CY25812	2.0	5.0	ns
T_{F1}	Clock Fall Time	SSCLK, CY25811, and CY25812	1.6	4.4	ns
T_{R2}	Clock Rise Time	SSCLK, only CY25814 when FRSEL = M	1.0	2.2	ns
T_{F2}	Clock Fall Time	SSCLK, only CY25814 when FRSEL = M	0.8	2.2	ns
T_{DCIN}	Input Clock Duty Cycle	XIN	40	60	%

AC Electrical Specifications

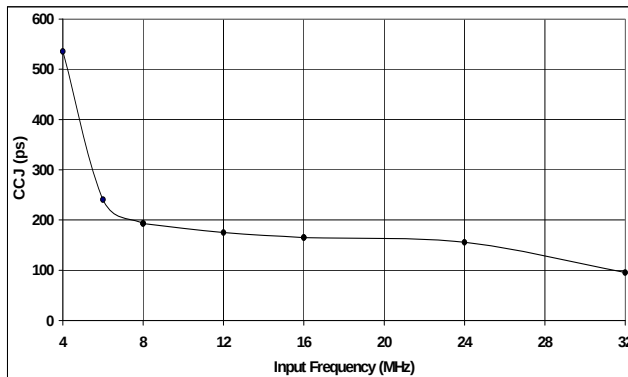
(Industrial Grade) (continued)

Parameter	Description	Condition	Min	Max	Unit
T_{DCOUT}	Output Clock Duty Cycle	SSCLK	40	60	%
T_{CCJ1}	Cycle to Cycle Jitter, Spread on	$F_{in} = 6 \text{ MHz}$, CY25811/12/14	–	650	ps
T_{CCJ2}	Cycle to Cycle Jitter, Spread on	$F_{in} = 12 \text{ MHz}$, CY25811/12/14	–	630	ps
T_{CCJ3}	Cycle to Cycle Jitter, Spread on	$F_{in} = 24 \text{ MHz}$, CY25811/12/14	–	520	ps
T_{SU}	PLL Lock Time	From $V_{DD} = 3.0V$ to valid SSCLK	–	4	ms

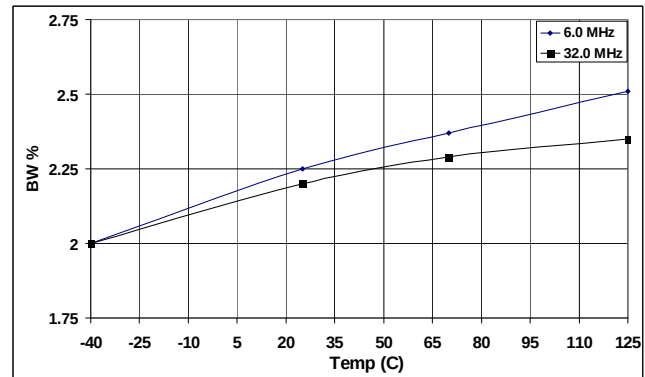
Characteristic Curves

The following curves demonstrate the characteristic behavior of CY25811/12/14 when tested over a number of environmental and application specific parameters. These are typical performance curves and are not meant to replace any parameter specified in DC and AC Specification tables.

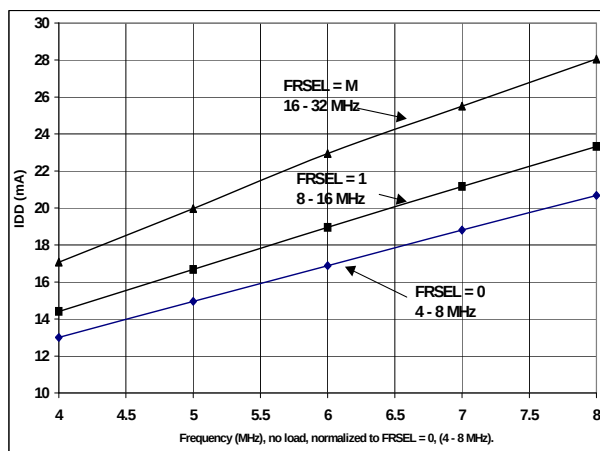
Figure 3. Characteristic Curves



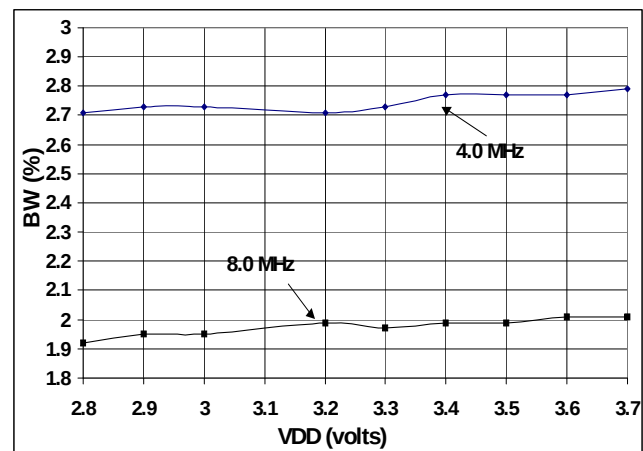
Jitter vs. Input Frequency (No Load)



Bandwidth % vs. Temperature



IDD vs. Frequency (FRSEL = 0, 1, M)

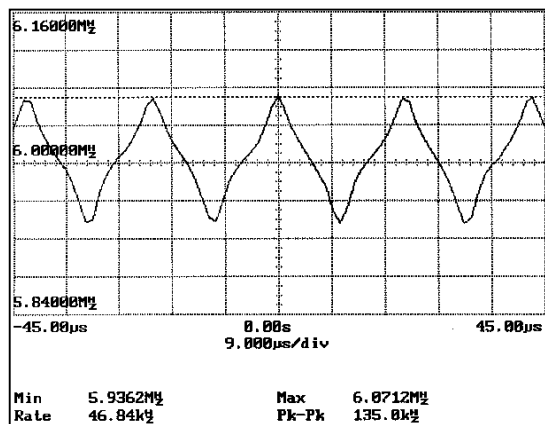


Bandwidth % vs. VDD

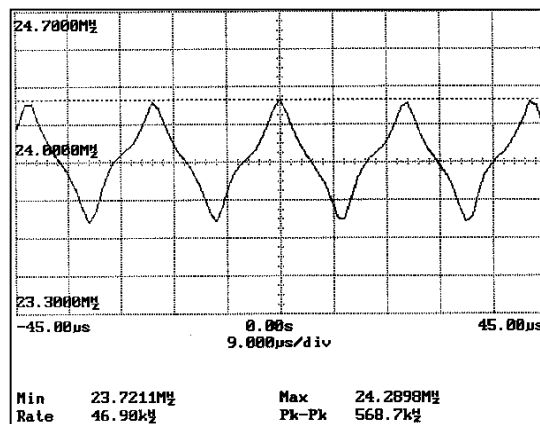
SSCG Profiles

CY25811/12/14 SSCG products use a non-linear “optimized” frequency profile as shown In [Figure 4](#). The use of Cypress proprietary “optimized” frequency profile maintains flat energy distribution over the fundamental and higher order harmonics. This results in additional EMI reduction in electronic systems.

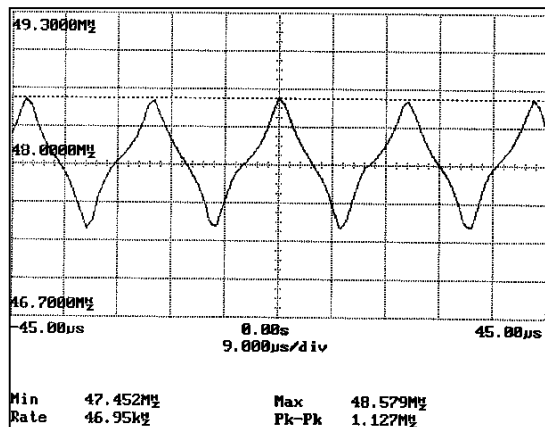
Figure 4. Spread Spectrum Profiles (Frequency versus Time)



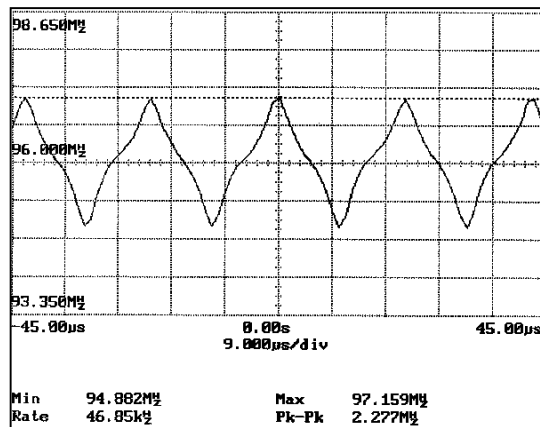
Xin = 6.0 MHz
S1, S0 = 0
FRSEL = 0
SSCLK1 = 6.0 MHz
P/N = CY25811



Xin = 24.0 MHz
S1, S0 = 0
FRSEL = M
SSCLK1 = 24.0 MHz
P/N = CY25811

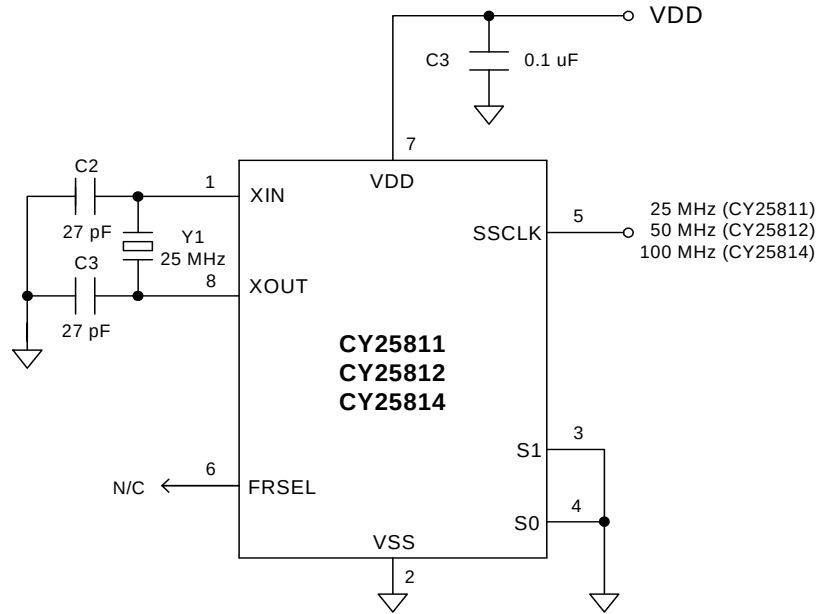


Xin = 12.0 MHz
S1, S0 = 0
FRSEL = 1
SSCLK1 = 48.0 MHz
P/N = CY25814



Xin = 24.0 MHz
S1, S0 = 0
FRSEL = M
SSCLK1 = 96.0 MHz
P/N = CY25814

Application Schematic



Ordering Information

Part Number	Package Type	Product Flow
Pb-Free Devices		
CY25811SXC	8-pin SOIC	Commercial, 0° to 70°C
CY25811SXCT	8-pin SOIC – Tape and Reel	Commercial, 0° to 70°C
CY25811SXI	8-pin SOIC	Industrial, –40° to 85°C
CY25811SXIT	8-pin SOIC – Tape and Reel	Industrial, –40° to 85°C
CY25811ZXC	8-pin TSSOP	Commercial, 0° to 70°C
CY25811ZXCT	8-pin TSSOP – Tape and Reel	Commercial, 0° to 70°C
CY25812SXC	8-pin SOIC	Commercial, 0° to 70°C
CY25812SXCT	8-pin SOIC – Tape and Reel	Commercial, 0° to 70°C
CY25812ZXC	8-pin TSSOP	Commercial, 0° to 70°C
CY25812ZXCT	8-pin TSSOP – Tape and Reel	Commercial, 0° to 70°C
CY25814SXC	8-pin SOIC	Commercial, 0° to 70°C
CY25814SXCT	8-pin SOIC – Tape and Reel	Commercial, 0° to 70°C
CY25814SXI	8-pin SOIC	Industrial, –40° to 85°C
CY25814SXIT	8-pin SOIC – Tape and Reel	Industrial, –40° to 85°C

Package Drawing and Dimensions

Figure 5. 8-Pin (150-Mil) SOIC S8

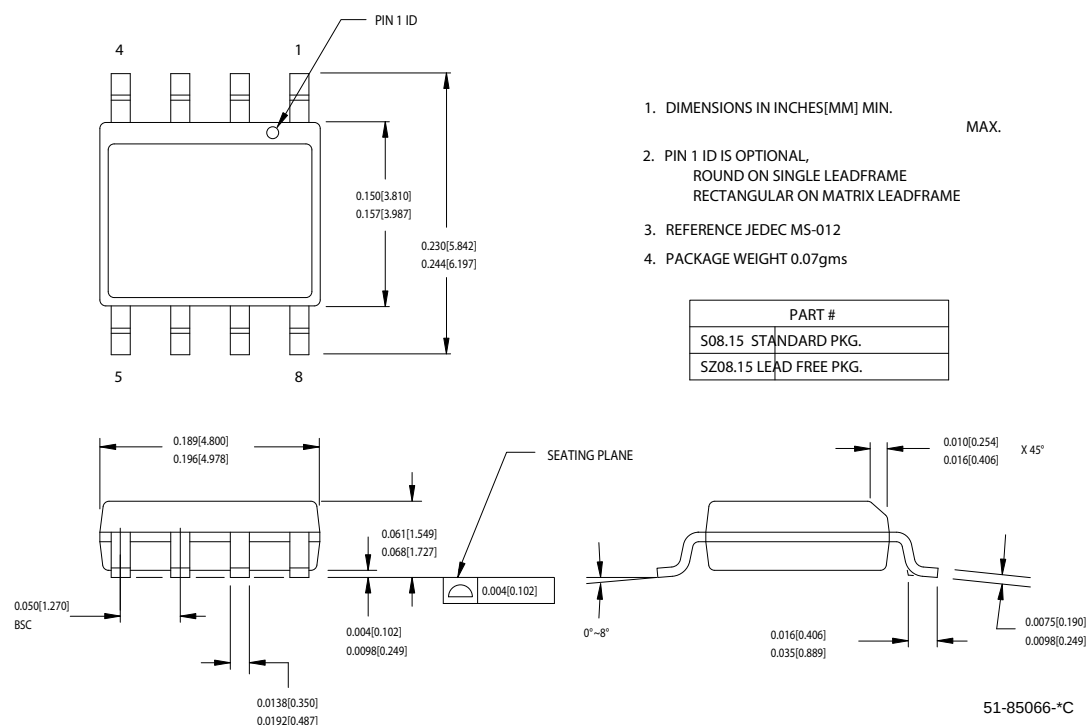
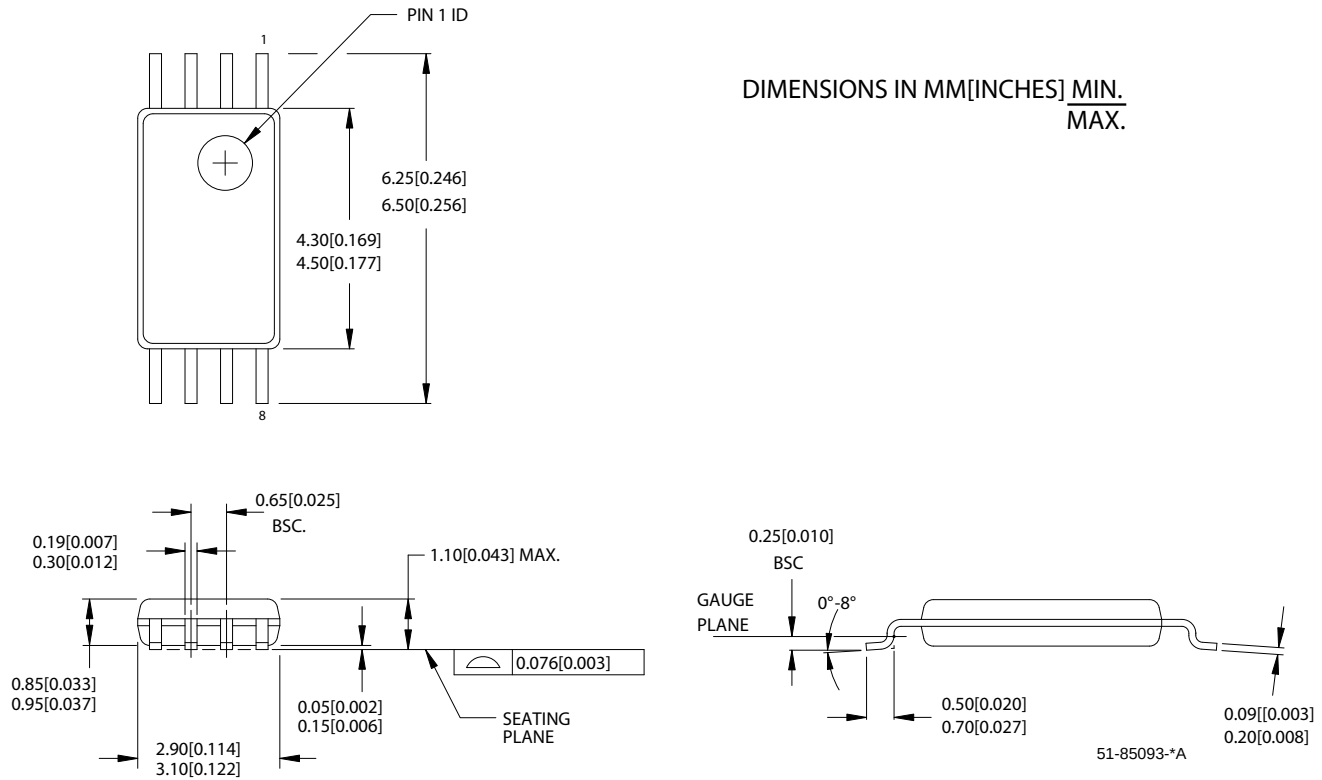


Figure 6. 8-Pin Thin Shrunk Small Outline Package (4.40 MM Body) Z8



Document History Page

Document Title: CY25811/12/14 Spread Spectrum Clock Generator Document Number: 38-07112				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	107516	NDP	06/14/02	Converted from IMI to Cypress
*A	108002	NDP	06/29/02	Deleted Junction Temp. in Absolute Maximum Ratings
*B	121578	RGL	01/29/03	Converted from Word to FrameMaker Added 8-pin TSSOP package in Commercial Temp. only Added an Industrial Temperature Range to all existing 8-pin SOIC packages
*C	125550	RGL	05/14/03	Changed IDD values from 19.6/22/27.2 to 25/30/35 in Commercial Grade DC Specs table Changed IDD values from 24/26.5/33 to 26/32/37 in Industrial grade DC Specs table Changed T _{CCJ1/2} values from 675/260 to 800/450 in Commercial grade AC Specs table Changed T _{CCJ1} value from 350 to 650 in Industrial grade AC Specs table
*D	131941	RGL	12/24/03	Removed automotive in the Applications section Changed the Output Clock Duty Cycle (T _{DCOUT}) from min. 45 and max. 55 to 40 and 60% respectively for both industrial and commercial grade Changed the min. Input Low Voltage (V _{IL}) from 0.15V _{DD} to 0.13V _{DD} Removed preliminary from the industrial AC/DC Electrical Specifications table
*E	231057	RGL	See ECN	Added Pb Free Devices
*F	1499165	KVM	See ECN	Updated Ordering Information table Corrected jitter values in features section on page 1 Changed: VDD from ±5% to ±10%, CIN1 min from 6 to 3.5 pF, CIN2 min from 3.5 to 2.8 pF, TF1 min from 2 to 1.6 ns, and TF2 min from 1.0 to 0.8 ns. Commercial grade: IDD1 max from 25 to 28 mA, IDD2 max from 30 to 33 mA, IDD3 max from 35 to 40 mA, TCCJ2 from 450 to 480 ps, TCCJ4 from 380 to 450 ps, and TCCJ5 from 380 to 550 ps Industrial grade: IDD1 max from 26 to 28 mA, IDD2 max from 32 to 33 mA, IDD3 max from 37 to 41 mA, TCCJ2 from 400 to 630 ps, and TCCJ3 from 400 to 520 ps
*G	2592288	CXQ/PYRS	10/23/08	Removed Pb package devices from Ordering Table
*H	2761988	CXQ	09/10/09	Removed reference to non-existent "Automotive" version. Fixed typo in DC spec table for VDD from min of 3.97 to 2.97. Fixed typo for PLL Lock time conditions. Removed CY25812SXI, CY25812SXIT, CY25814ZXC, and CY25814ZXCT from Ordering Information.

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