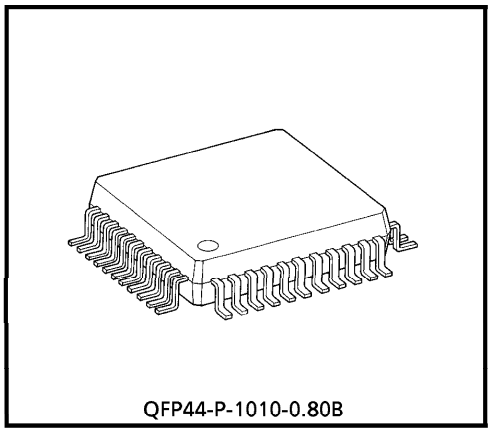
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8508AF

R/W IC FOR FLOPPY DISK DRIVE

TA8508AF is a bipolar monolithic IC developed as a read/write IC for perpendicular floppy disk drives (PFD). TA8508AF consists of a floppy disk drive read circuit, a write circuit, and various control circuits, all integrated on a single chip to reduce disk drive size and power consumption.

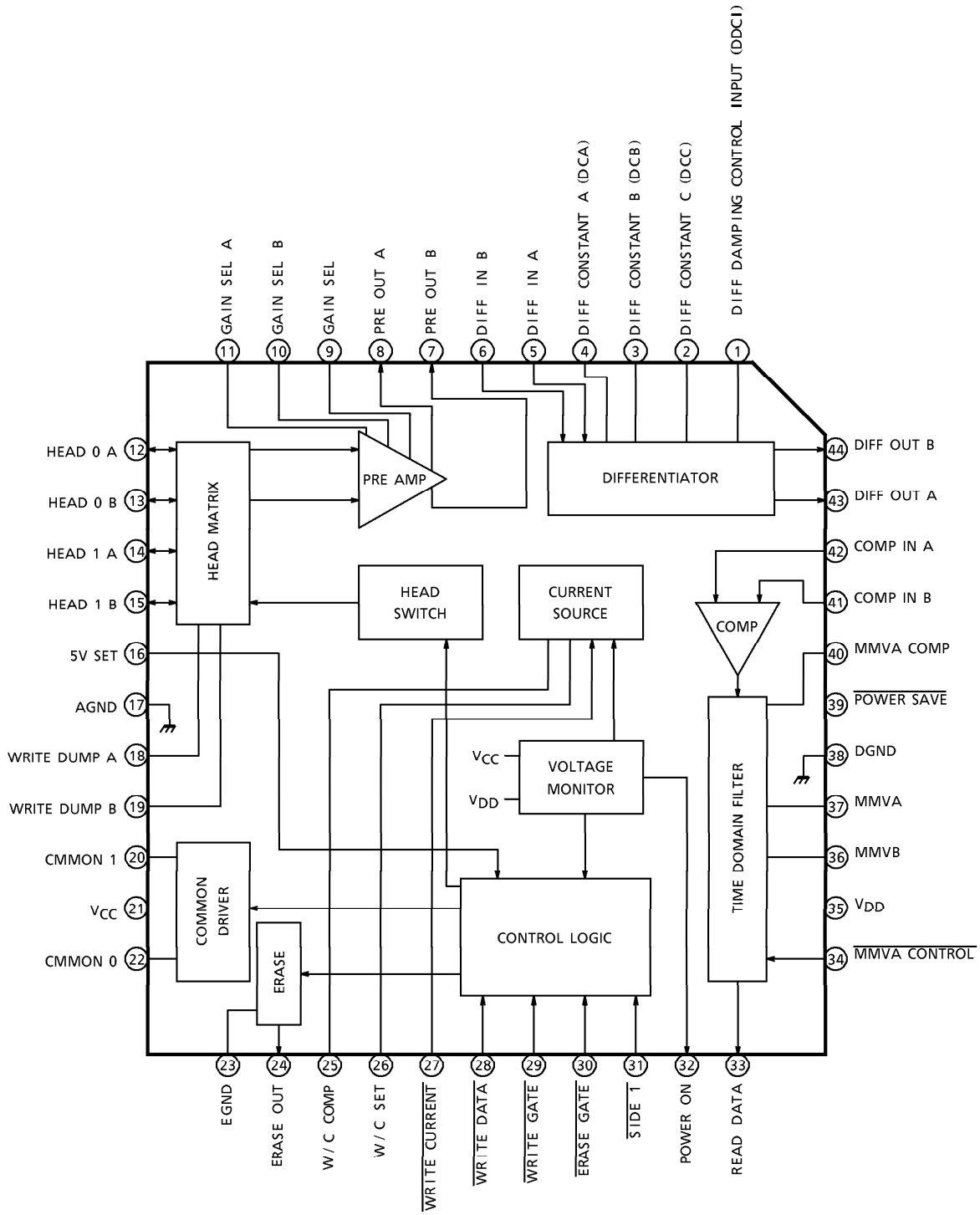


Weight: : 0.56g (Typ.)

FEATURES

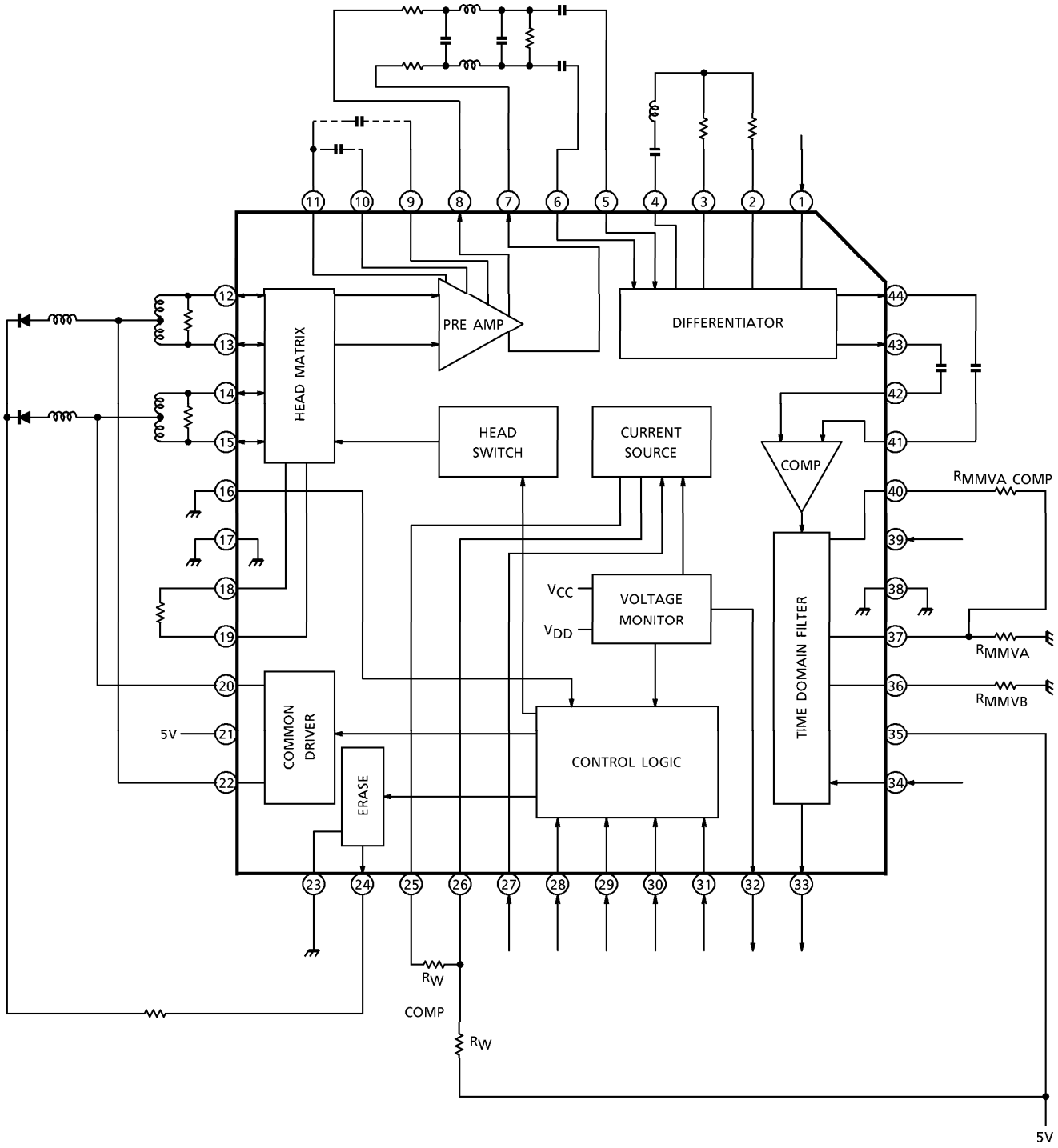
- Power save function which reduces power dissipation (to 9mW typ.) during non-operation (not reading, writing, or erasing).
- 5V single power supply (4.3V to 6.0V)
- Incorporates a diode switch for switching between read and write heads. The differential voltage gain of the read amp can be set to 200 times or 400 times using the gain select pin.
- The write current can be set to a maximum of $25mA_{DC}$ using external resistance.
- A built-in write current switching circuit allows the current value to be switched between outer and inner tracks.
- Read, write, and erase circuits are incorporated in a single chip and can be controlled independently by $\overline{WG}$ and $\overline{EG}$ signals.
- A built-in power monitor circuit prevents writing in error at such times as when the power is turned on or abnormal voltage is applied.
- Incorporates a time constant capacitor for the time domain filter. Time constants can be set using an external resistor.
- Incorporates a time constant switching circuit for the time domain filter. Time constants can be switched between outer and inner tracks.
- Incorporates a differentiator constant switching circuit. The differentiator frequency characteristics can be switched.

PIN LAYOUT DIAGRAM/INTERNAL EQUIVALENT BLOCK DIAGRAM



Take care when using pins 9, 11, 12, 13, 14, and 15, as the allowable overvoltage surge margin is small (up to ±100V).

EXTERNAL CONNECTION



PIN FUNCTION

PIN No.	PIN NAME	PIN FUNCTION
1	DIFF DUMPING CONTROL INPUT	Differentiator constant select pin Inputting low logic voltage selects pins 3 (DCB) and 4 (DCA); inputting high logic voltage selects pins 2 (DCC) and 4 (DCA).
2	DIFF CONSTANT C	Differentiator constant connecting pins These pins connect the differentiator constants between pins 4 (DCA) and 2 (DCC), and between pins 4 (DCA) and 3 (DCB).
3	DIFF CONSTANT B	
4	DIFF CONSTANT A	
5	DIFF IN A	Differentiator input pins. These pins input a read signal from the pre-amp output pin to the differentiator via the filter circuit.
6	DIFF IN B	
7	PRE OUT B	Pre-amp output pins These differential output pins output a read signal to the differentiator input pin via the filter circuit.
8	PRE OUT A	
9	GAIN SEL	Pre-amp gain select pins AC coupling of pins 9 and 11 selects a 400-times pre-amp gain. AC coupling of pins 10 and 11 selects a 200-times pre-amp gain.
10	GAIN SEL B	
11	GAIN SEL A	
12	HEAD 0 A	Magnetic head 0 input/output pins These pins connect the write/read magnetic head with a center tap, and the damping resistor at a read.
13	HEAD 0 B	
14	HEAD 1 A	Magnetic head 1 input/output pins Another pair of input/output pins like those above.
15	HEAD 1 B	
16	5V SET	V_{CC} power select input pin Grounding this pin selects V_{CC} = 5V mode.
17	AGND	Analog GND connecting pin
18	WRITE DUMP A	Write dumping resistor connecting pins The head dumping resistor is connected between these pins at a write.pin voltage at read and write.
19	WRITE DUMP B	
20	COMMON 1	Head 1 common driver connecting pin This pin connects to the center tap of magnetic head 1. It sets the head 1 pin voltage at read and write.
21	V_{CC}	Analog power connecting pin
22	COMMON 0	Head 0 common driver connecting pin This pin connects to the center tap of magnetic head 0. It sets the head 0 pin voltage at read and write.
23	EGND	Erase GND connecting pin
24	ERASE OUTPUT	Erase current sink pin Open collector pin for the erase current sink.
25	W / C COMP	Connecting pin for write current compensation resistor Between this pin and pin 26, connect a write current compensation resistor R_W COMP to set the write current increase (I_{WC}). Equation $I_{WC} = \frac{1.3 - V_{WC}}{R_W \text{ COMP } (\Omega)} \times 10\ (A_{DC})$
26	W / C SET	Connecting pin for write current setting resistor Between this pin and pin V_{DD} 35, connect a write current setting resistor R_W to set the write current value. Equation $I_W = \frac{1.3}{R_W\ (\Omega)} \times 10\ (A_{DC})$

PIN No.	PIN NAME	PIN FUNCTION
27	$\overline{\text{WRITE CURRENT}}$	Write current control pin (digital input) When low logic voltage is input, the write current is defined as the sum of IW and IWC. When high logic voltage is input, the write current is I_W only.
28	$\overline{\text{WRITE DATA}}$	Write data input pin (Schmitt digital input) The write data input pin is triggered when digital input goes from high to low.
29	$\overline{\text{WRITE GATE}}$	Write gate signal input pin (digital input) Inputting low logic voltage activates the write.
30	$\overline{\text{ERASE GATE}}$	Erase gate signal input pin (digital input) Inputting low logic voltage activates the erase.
31	$\overline{\text{SIDE 1}}$	Head side switching signal input pin (digital input) Inputting low logic voltage activates head 1; inputting high logic voltage activates head 0.
32	POWER ON	Voltage drop detection output pin This open collector pin outputs low while at least one / both of the V_{DD} and V_{CC} is / are below the specified value.
33	READ DATA	Read data output pin This pin outputs the read data (totem pole type).
34	$\overline{\text{MMVA CONTROL}}$	Time domain filter time constant switching signal input pin (digital input) Inputting low logic voltage narrows the output width of the first monostable circuit.
35	V_{DD}	Digital power connecting pin
36	MMVB	Second monostable circuit R connecting pin for time domain filter Connect the second monostable circuit time constant setting resistor R_{MMVB}. The following equation determines the second monostable circuit's pulse width t_2. $t_2 = 27 \times (R_{MMVB}\ (k\Omega) + 0.1)$ (ns)
37	MMVA	First monostable circuit R connecting pin for time domain filter. Connect the first monostable circuit time constant setting resistor R_{MMVA}. The following equation determines the first monostable circuit's pulse width t_1. $t_1 = 53.5 \times (R_A\ (k\Omega) + 0.1)$ (ns) Note: When MMVA CONTROL logic input voltage is high, $R_A = R_{MMVA}$. When $\overline{\text{MMVA CONTROL}}$ logic input voltage is high, $R_A = R_{MMVA} // R_{MMVA}$ COMP.
38	DGND	Digital GND connecting pin
39	$\overline{\text{POWER SAVE}}$	Power save mode select signal input pin (digital input) Inputting low logic voltage selects power save mode, which reduces R / W I_C power dissipation. During power save mode, read, write, and erase operations are disabled. (The power monitor circuit still functions.)
40	MMVA COMP	Resistor connecting pin for time domain filter time constant switching. This open collector pin connects resistor R_{MMVA} COMP between this and pin 37 to compensate the output width of the time domain filter's first monostable circuit.
41	COMP IN B	Comparator input pins A read signal is input to these two pins from the differentiator output pins via the AC coupling capacitors.
42	COMP IN A	
43	DIFF OUT A	Differentiator output pins These two pins output a read signal to the comparator input pin via the AC coupling capacitors.
44	DIFF OUT B	

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTICS	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	7	V
Supply Voltage	V_{DD}	7	V
Digital Signal Input Voltage (Note 1)	—	−0.5~5.5	V
Voltage Applied to Power On Pin (Note 2)	—	7	V
Voltage Applied to Erase Output Pin (Note 3)	—	7	V
Voltage Applied to Head 0 / 1 A / B Pins (Note 4)	—	7	mA
Common Drive Source Current	I_{COM}	75	mA
Erase Drive Sink Current	I_E	50	mA
Write Drive Current (Note 2)	I_W	25	mA_{DC}
Sink Current on Power On Pin	—	7	mA
Ambient Operating Temperature	Ta	−20~75	°C
Junction Operating Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−55~150	°C
Power Dissipation (Ta = 25°C for IC only) (Note 5)	P_D	0.75	W

(Note1) The $\overline{\text{WRITE CURRENT}}$, $\overline{\text{WRITE DATA}}$, $\overline{\text{WRITE GATE}}$, $\overline{\text{ERASE GATE}}$, $\overline{\text{SIDE1}}$, $\overline{\text{MMVA CONTROL}}$, $\overline{\text{POWER SAVE}}$, DDCI signals are input to the 5V SET pin.

(Note2) Applies to POWER ON pin (pin 32).

(Note3) Applies to ERASE OUTPUT pin (pin 24).

(Note4) Applies to HEAD 0 A, HEAD 0 B, HEAD 1 A, and HEAD 1 B pins (pins 12, 13, 14, and 15).

(Note5) For device usage conditions, see Figure 1 Power Dissipation (P_D)-Ambient Temperature (Ta).

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	CONDITIONS	UNIT
V_{CC}, V_{DD} supply voltage	4.3~6.0	V
Operating ambient temperature	0~60	°C

ELECTRICAL CHARACTERISTICS

(1) CURRENT DISSIPATION (Ta = 25°C, V_{CC} = 5V, V_{DD} = 5V)

CHARACTERISTICS		SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
In Read	V_{DD} Current Dissipation	I_{DDR}	1	—	—	17.7	23.4	mA
	V_{CC} Current Dissipation	I_{CCR}	1	—	—	7.5	8.6	mA
In Write	V_{DD} Current Dissipation	I_{DDW}	1	(Note 1)	—	9.5	15.4	mA
	V_{CC} Current Dissipation	I_{CCW}	1	—	—	12.3	18.8	mA
In Erase	V_{DD} Current Dissipation	I_{DDE}	1	—	—	9.4	13.9	mA
	V_{CC} Current Dissipation	I_{CCE}	1	—	—	12.6	19.2	mA
In write + Erase	V_{DD} Current Dissipation	I_{DDW+E}	1	(Note 1)	—	12.3	19.4	mA
	V_{CC} Current Dissipation	I_{CCW+E}	1	—	—	12.3	18.8	mA
In Power Save	V_{DD} Current Dissipation	I_{DDPS}	1	—	—	1.35	2.7	mA
	V_{CC} Current Dissipation	I_{CCPS}	1	—	—	0.27	0.4	mA
	Total Power Dissipation	P_{DPS}	1	—	—	8.1	15.5	mW

(Note 1) When Write Current I_W = 0

(2) POWER MONITOR (Ta = 25°C, V_{CC} = 0~7V, V_{DD} = 0~7V)

CHARACTERISTICS		SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}, V_{CC} Threshold Voltage	Positive Direction	V_T^+	—	—	—	4.0	4.2	V
	Negative Direction	V_T^-	—		3.6	4.0	—	
Threshold Voltage Width		$V_T^+ - V_T^-$	—	—	—	150	—	mV
Saturation Voltage When Power On Pin (Pin 32) Detection On		—	—	V_{DD} = 3.6V I_{SINK} = 5mA	—	—	0.4	V
Leakage Current When PoweR On Pin (Pin 32) Detection Off		—	—	V_{DD} > 4.5V	—	—	10	μA

(3) PRE-AMP, DIFFERENTIATOR, COMPARATOR (Ta = 25°C, V_{CC} = 5V, V_{DD} = 5V)

	CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Head Switcher / Pre-amp	Differential Voltage Gain	G_{V1}	2	Test Frequency f = 1MHz	340	375	415	V / V
		G_{V2}	2	Test Frequency f = 1MHz	170	185	200	
	Gain Attenuation Bandwidth (– 3dB)	F_C	2	—	8	12	—	MHz
	COMMON MODE Rejection Ratio	CMRR	—	Input Sine Wave f = 1MHz 200mV_{rms}	50	—	—	dB
	Power Supply Rejection Ratio	RSRR	—	Multiplexed sine wave f = 10kHz 1V_{p-p}	70	—	—	dB
	Differential Input Resistance	R_{IN}	—	f = 62.5~625kHz	6.0	9.0	16.0	kΩ
	Differential Input Capacitance	C_{IN}	—	f = 250kHz	—	24	—	pF
Pre-Amp	Differential Input Voltage Amplitude	V_{IN}	—	At × 200 Gain	0.8	—	7.5	mV_{p-p}
	Differential Output Voltage Amplitude	V_{OUT}	2	—	2.0	3.0	—	V_{p-p}
	Differential Output Current Amplitude	I_{OUT}	—	—	3.0	4.0	5.0	mA_{p-p}
	Differential Output Offset Voltage	V_{OFS}	—	—	—	—	0.5	V
	Input Equivalent Noise Voltage	E_N	2	Head Connected f = 400Hz to 1MHz	—	4.0	6.0	μV_{rms}
Differentiator	Gain Attenuation Bandwidth (– 3dB)	F_{CD}	—	—	20	—	—	MHz
	Differential Output Voltage Amplitude	V_{OUTD}	—	—	—	2	—	V_{p-p}
	Differential Output Offset Voltage	V_{OFD}	—	—	—	20	—	mV
	Differential Input Resistance	R_{IND}	—	—	16	24	—	kΩ
	Differential Output Resistance	R_{OUTD}	—	—	—	200	—	Ω
	Sink Current (Pins 2, 3, 4)	I_{SINKD}	—	—	1.4	2.0	—	mA
Comparator	Maximum Differential Input Voltage Amplitude	V_{INC}	—	—	—	2	—	V_{p-p}
	Differential Input Resistance	R_{INC}	—	—	20	32	—	kΩ

(4) TIME DOMAIN/WAVEFORM SHAPING BLOCK (Ta = 25°C, V_{CC} = 5V, V_{DD} = 5V)

CHARACTERISTICS		SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
First Monostable Output Pulse Width		t_1	3	—	200	—	3000	ns
Second Monostable Output Pulse Width		t_2	3	—	100	—	1200	ns
Saturation Voltage On MMVA COMP Pin		V_{MMC}	—	I_{SINK} = 10μA	—	—	50	mV
First Monostable Output Pulse Width Precision		E_{TM1}	3	—	− 18	—	18	%
Second Monostable Output Pulse Width Precision		E_{TM2}	3	—	− 20	—	20	%
First Monostable Output Pulse Width Compensation Precision		E_{TM1C}	3	—	− 15	—	15	%
Peak Shift		PS	3	COMP Input f = 62.5 to 500kHz Differential Input = 200mVp-p	—	—	1	%
Read Output	Low Output Voltage	V_{LOUT}	—	I_{OL} = 2mA	—	—	0.5	V
	High Output Voltage	V_{HOUT}	—	I_{OH} = − 10μA	3.5	—	—	V
				I_{OH} = − 0.4mA	2.8	—	—	
	Sink Current	$I_{SI\ RD}$	—	V_{OUT} = 0.8V	2	4	—	mA
	Source Current	$I_{SO\ RD}$	—	V_{OUT} = 2.8V	0.4	1	—	mA
	Rising Time	t_r	3	At Read Output = 0.5 to 2.2V With Load Capacitance Of 20pF	—	—	25	ns
	Falling Time	t_f			—	—	25	ns

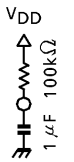
(5) WRITE SYSTEM/ERASE SYSTEM (Ta = 25°C, V_{CC} = 5V, V_{DD} = 5V)

	CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Common Driver	Output voltage in write selected	V_{WCMH}	—	I_W = 25mA$_{DC}$	4.4	—	—	V
	Output voltage in write not-selected	V_{WCML}	—	—	—	—	0.2	V
	Output voltage in read selected	V_{RCMH}	—	—	2.3	2.6	2.9	V
	Output voltage in read not-selected	V_{RCMH}	—	—	—	—	0.2	V
	Output current range	I_{COM}	—	—	—	—	75	mA
Erase Driver	ERASE OUTPUT pin output saturation voltage	V_{ER}	—	I_{Erase} = 50mA	—	0.2	0.5	V
	ERASE OUTPUT pin leakage current	I_{LKER}	—	—	—	—	15	μA
	Erase current range	I_{ERASE}	—	—	—	—	50	mA
Write Driver	Write current setting precision	E_W	—	—	– 8	—	8	%
		E_{WC}			– 10	—	10	
	Write current output imbalance	D_W	—	—	—	—	1	%
	Write current variable range (one side)	I_W	—	—	—	—	20	mA$_{DC}$
				V_{DD} = 5.0V, Ta = 25°C	—	—	28	
	Write current compensation variable range (one side)	I_{WC}	—	—	—	—	5	mA$_{DC}$
	W / C COMP pin saturation voltage	V_{WC}	—	I_{source} = 0.5mA	—	50	300	mV
(Pins 12·13·14·15) in Write HEAD 0 / 1 A / B Pins	Leakage Current	I_{LKW}	—	—	—	—	10	μA
	Saturation voltage	V_{SAT}	—	—	—	2	—	V
	Differential output capacitance	C_{OUT}	—	—	—	23	—	pF
	Differential output resistance	R_{OUT}	—	f = 1MHz	—	280	—	kΩ

(6) LOGIC INPUT/OUTPUT BLOCK (Ta = 25°C, V_{CC} = 5V, V_{DD} = 5V)

CHARACTERISTICS			SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital Signal Input	Low Logic Input Voltage		V_{LIN}	—	—	—	—	0.8	V
	High Logic Input Voltage		V_{HIN}	—	—	2.0	—	—	V
	Low Logic Input Current	$\overline{PS}$ Pin (Pin 39)	I_{LIN}	—	0.4V Applied	—	—	50	μA
		Others		—	0.4V Applied	—	—	250	
	High Logic Input Current (Pins 28, 29, 30, 31)		I_{HIN1}	—	2.4V Applied	—	—	10	μA
	High Logic Input Current (Pin 27)		I_{HIN2}	—	2.4V Applied	—	—	130	μA
	High Logic Input Current (Pin 34)		I_{HIN3}	—	2.4V Applied	—	—	80	μA
Schmitt Digital Signal Input	Negative Direction Threshold Voltage (Input H → L)		V_{LINS}	—	—	0.8	1.0	—	V
	Positive Direction Threshold Voltage (Input L → H)		V_{HINS}	—	—	—	1.6	2.0	V
	Hysteresis Voltage Width		V_{HINS}-V_{LINS}	—	—	0.3	0.6	—	V
Write Data	Write Data Maximum Input Frequency		f_{IND}	—	V_{IN} = 0.8~2.2V (50% Duty)	—	—	12	MHz

(7) SWITCHING CHARACTERISTICS (Ta = 25°C, V_{CC} = 5V, V_{DD} = 5V)

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Recovery Time From Power Save to Read Mode	—	—	$\overline{PS}$ off→DIFF Output 90 to 110% (Note 1)	—	1	2	ms
Head Switching Time	—	—	$\overline{SIDE1}$ 50%→Selected V_{COM} 90%, Head Pin and Common Pin Connected	—	—	4	μs
Read to write mode	—	—	$\overline{WG}$ Off→Selected V_{COM} 90%	—	—	1	μs
WD-Iw Delay	—	—	$\overline{WD}$ 50%→I_W 50%	—	—	0.3	μs
Write Current Rise Time	—	—	L_h = 0mH	—	—	0.1	μs
Recovery Time From Erase Mode to Read Mode	—	—	$\overline{EG}$ Off→ DIFF Output 90 to 110%	—	—	20	μs
Read Recovery Time	—	—	$\overline{WG}$, $\overline{EG}$ Off→ DIFF Output 90%	—	30	40	μs
Sink Current Rise and Fall Time When Power Monitor Detection Turned Off or Off	—	—	Load (Pin 32) 	—	—	100	ms

Note 1 : When returning from power save to read mode, raise $\overline{WG}$ and $\overline{EG}$ to high level 10μs before $\overline{PS}$ goes from low to high.

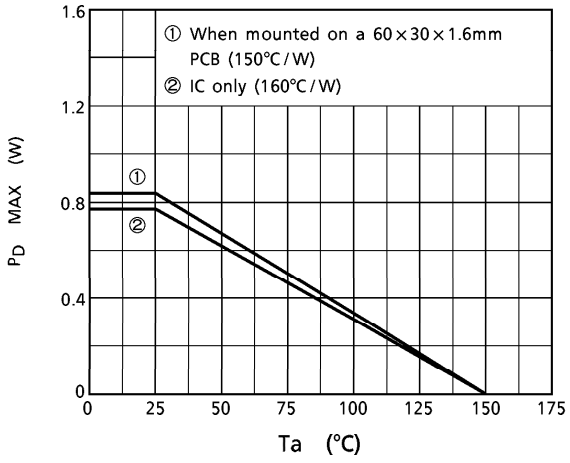
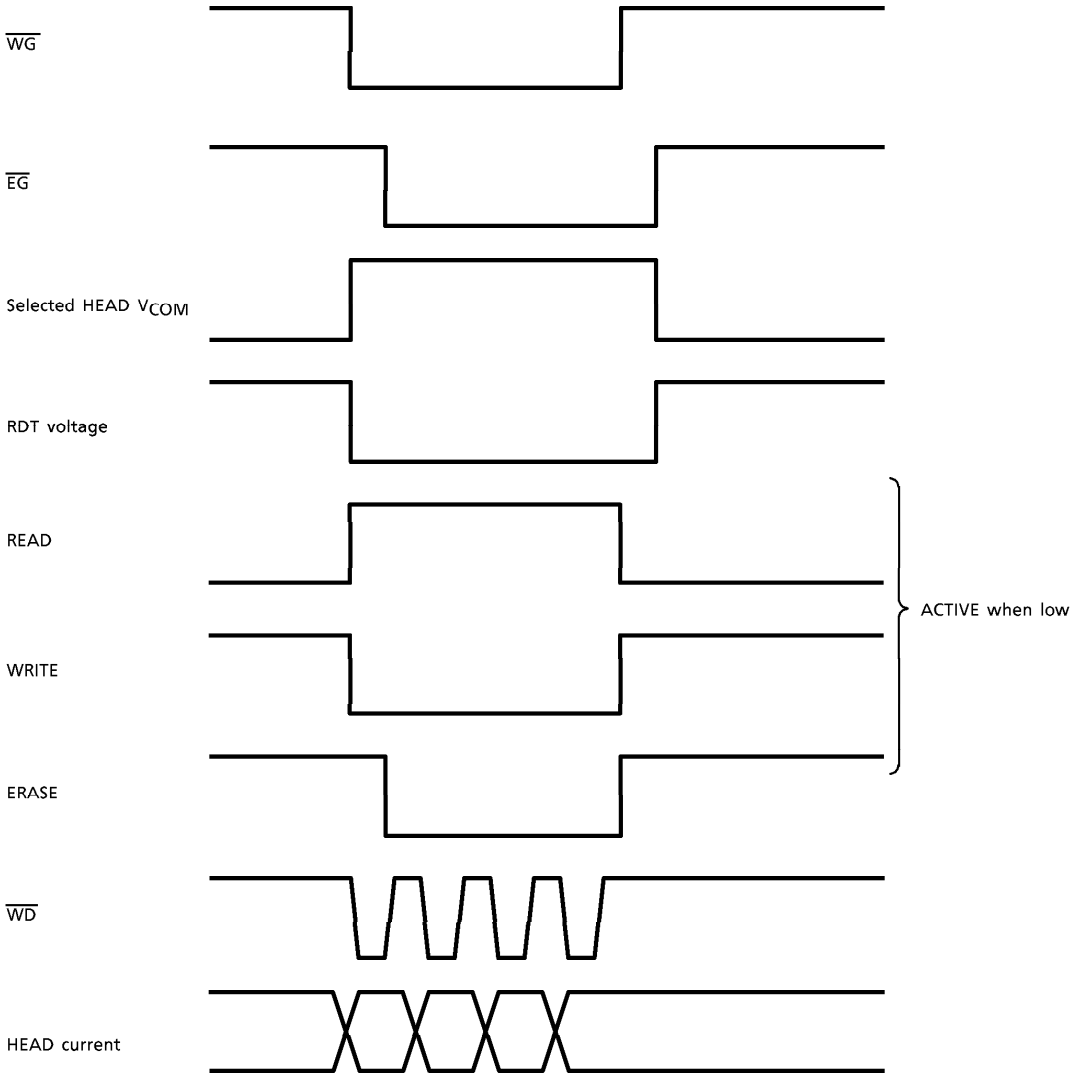


Fig.1 Power dissipation (P_D) – Ambient Temperature (Ta)

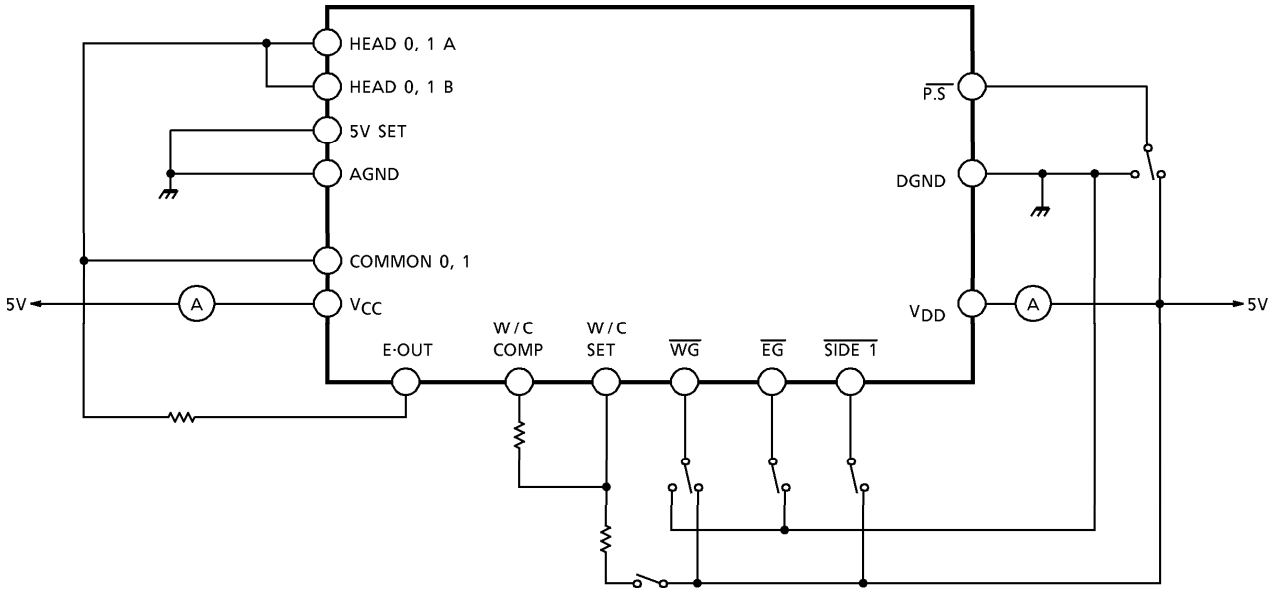
The TA8508AF maximum operating ambient temperature (Ta) is 75°C. However, refer to the above graph when using, as the package's power dissipation (P_D) varies according to the ambient temperature.

TIMING CHART

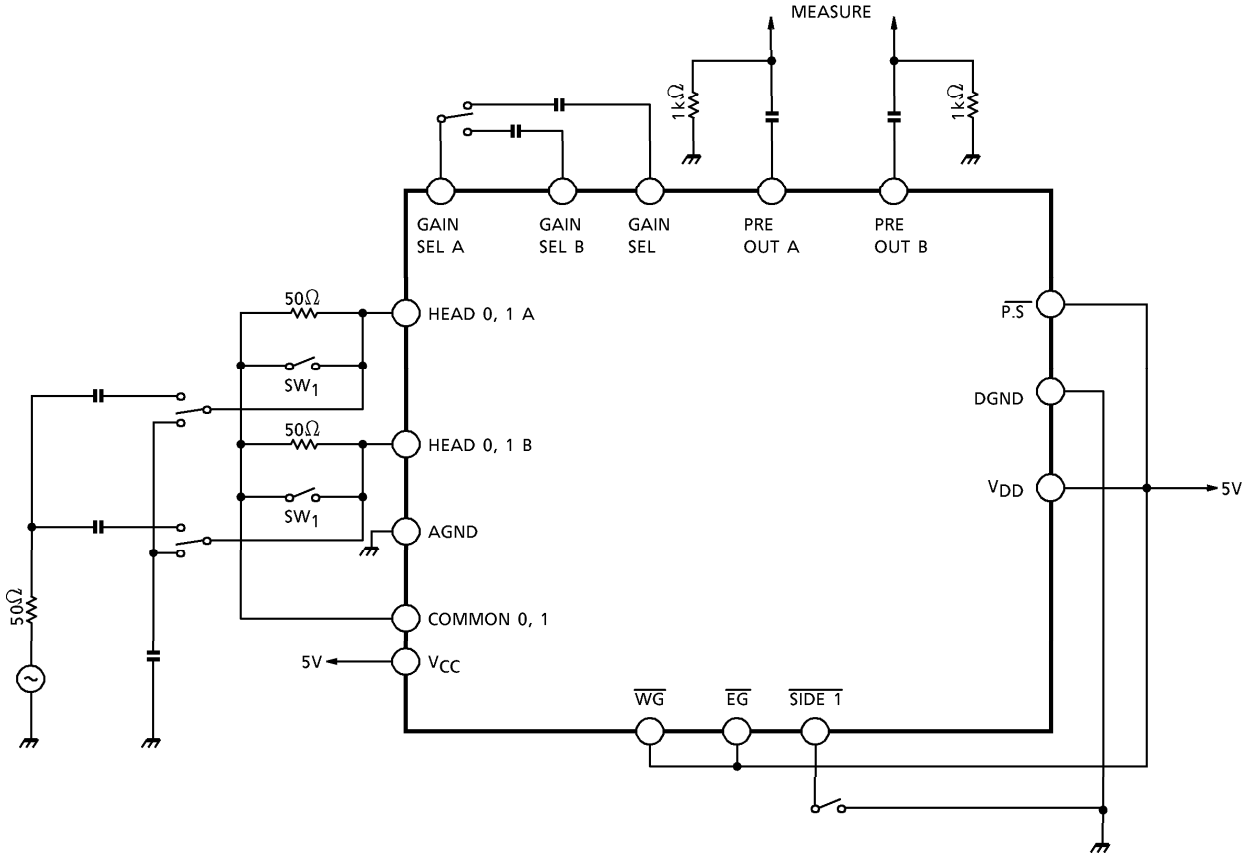


TEST CIRCUIT

1. I_{CC}, I_{DD}



2. G_V, F_C, V_{OUT}, E_N



Note1 : When G_V, F_C, or V_{OUT} is measured, the signal is input to either of the HEAD 0, 1 A pins or HEAD 0, 1 B pins, whichever pair is selected.

Note2 : Turn SW_1 off only when measuring E_N.

3. t_1, t_2, ETM1, ETM2, ETM1C, PS, t_r, t_f

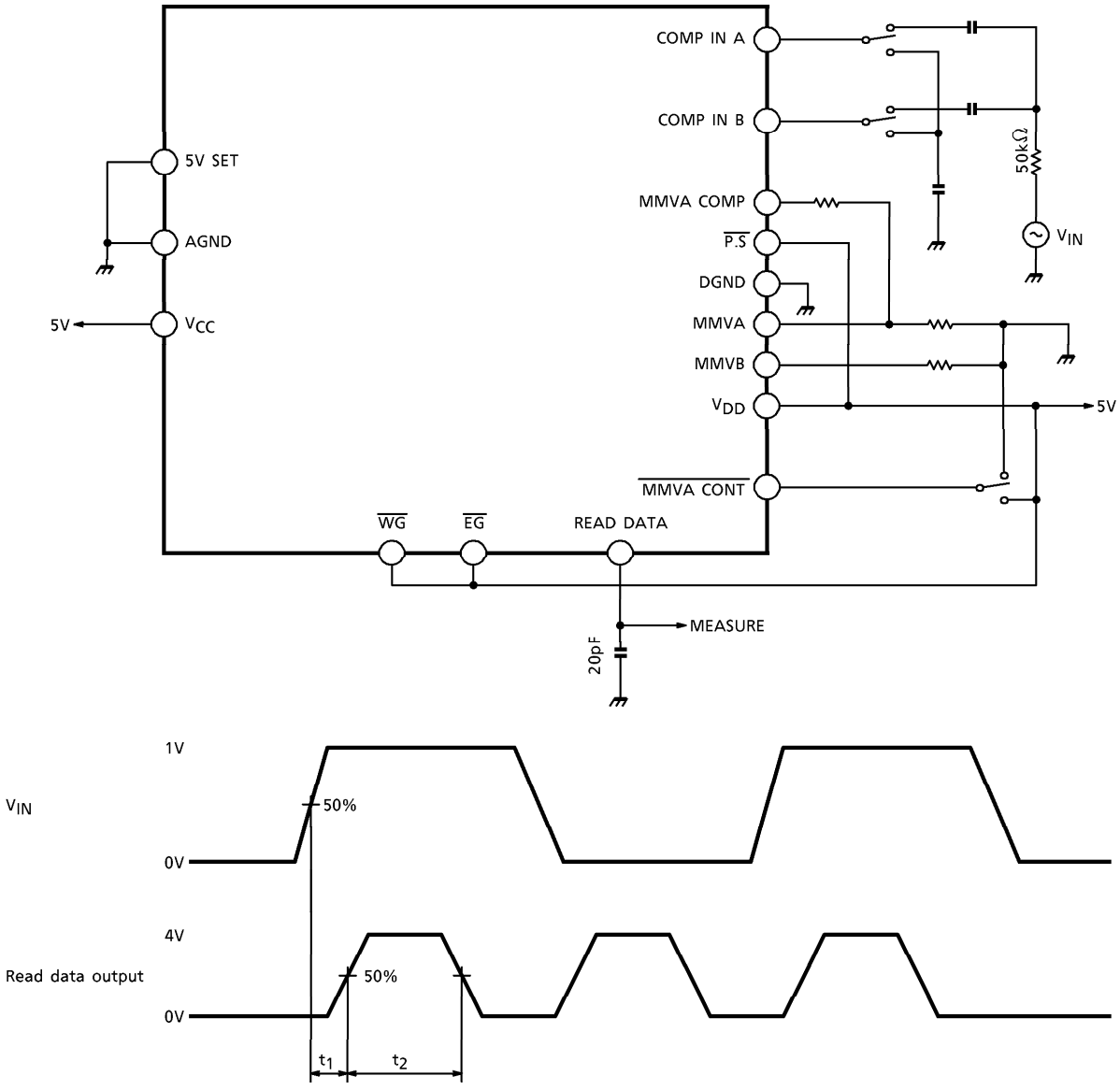


Figure 3-1 t_1, t_2

(1) First and second monostable output pulse precision

Connect R_{MMVA} to set t_1 to 1μs and connect R_{MMVB} to set t_2 to 0.5μs. Observe t_1 and t_2 in the read data output.

ETM1 and ETM2 are defined as: $ETM1 = (1 - t_1 / 1) \times 100\ (\%)$

$STM2 = (1 - t_2 / 0.5) \times 100\ (\%)$ (t_1 (μs)、 t_2 (μs))

(2) First monostable output pulse width compensation precision

Connect R_{MMVA}, R_{MMVA} COMP so that t_1 to t'_1 (the difference between t_1 prior to pulse width compensation and t'_1 after pulse width compensation) is 1μs.

Observe t'_1 and t_1 when 0.8V and 2.0V are applied to $\overline{\text{MMVA CONTROL}}$.

EMT1C is defined as:

$$EMT1C = \{ 1 - (t_1 - t'_1) / 1 \} \times 100\ (\%)\ (t_1\ (\mu s)、\ t'_1\ (\mu s))$$

(3) Peak shift

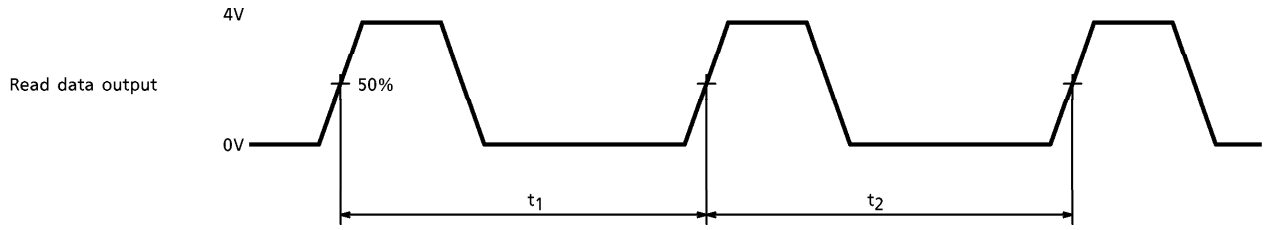


Figure3.2 P.S.

$$PS = \frac{1}{2} \times \left| \frac{t_1 - t_2}{t_1 + t_2} \right| \times 100\ (\%)$$

(4) Read data output rise and fall times

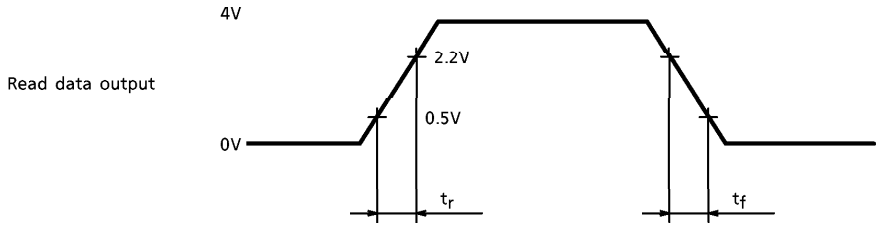
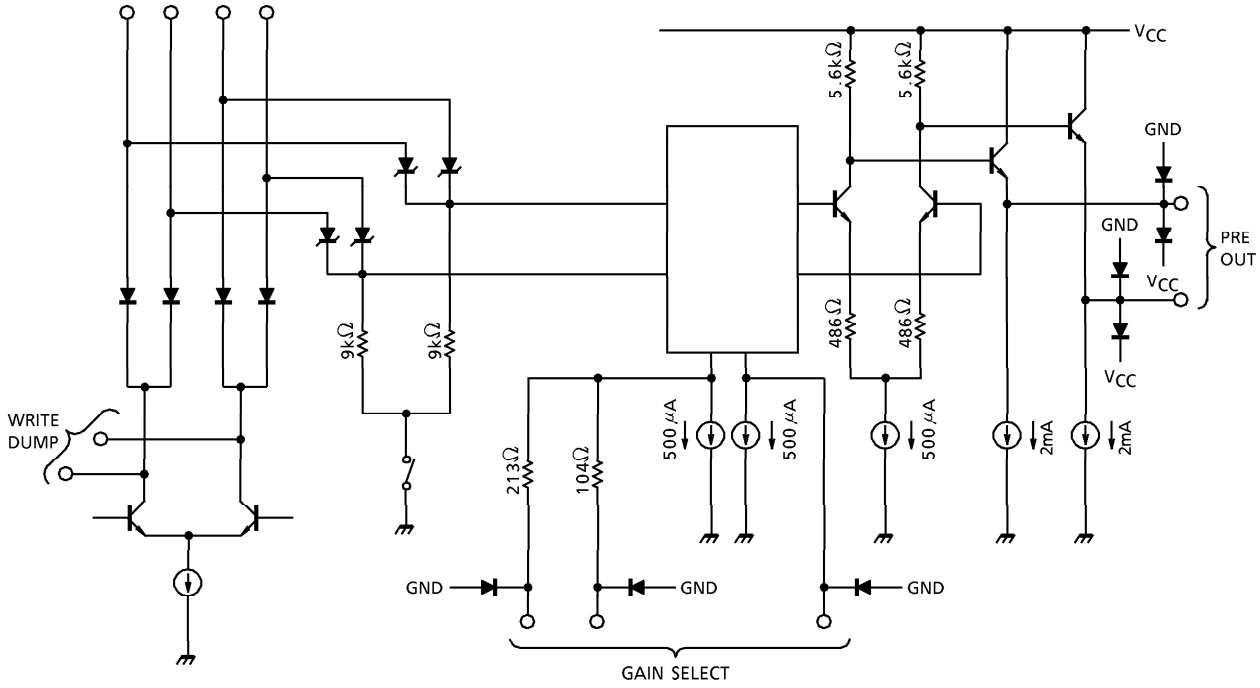


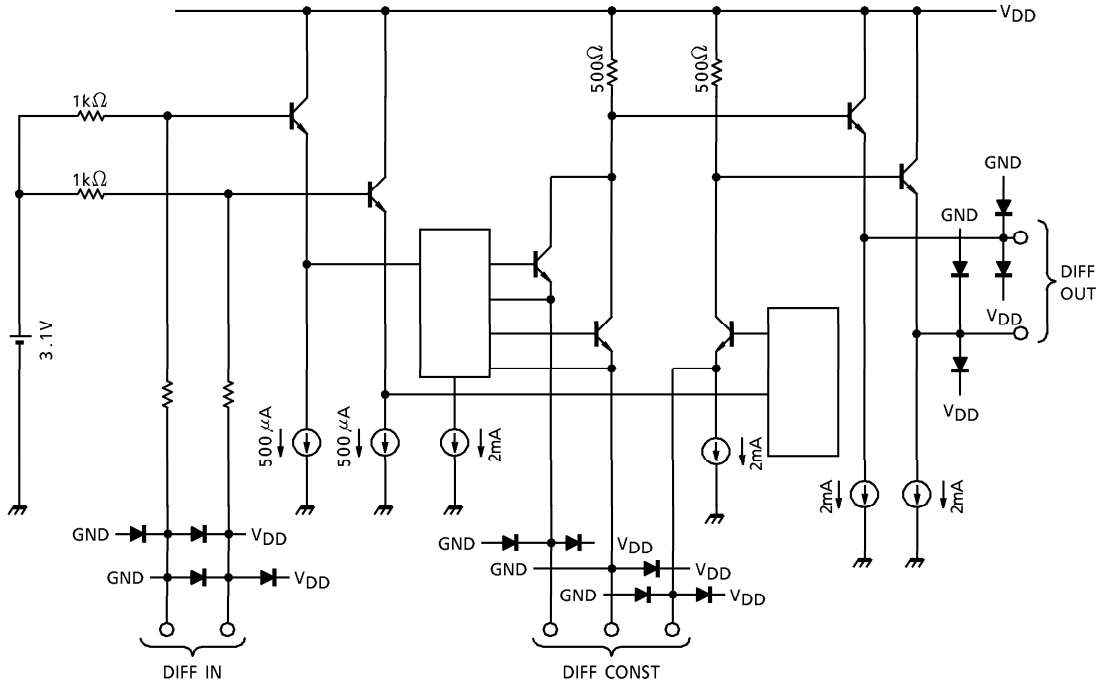
Figure3.3 t_r and t_f

INTERNAL EQUIVALENT CIRCUITS

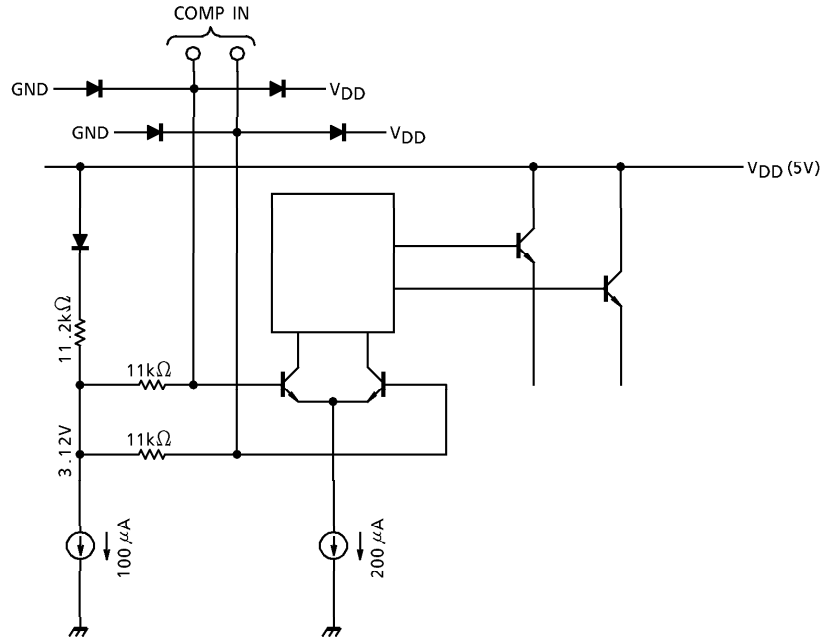
1. Pre-amp



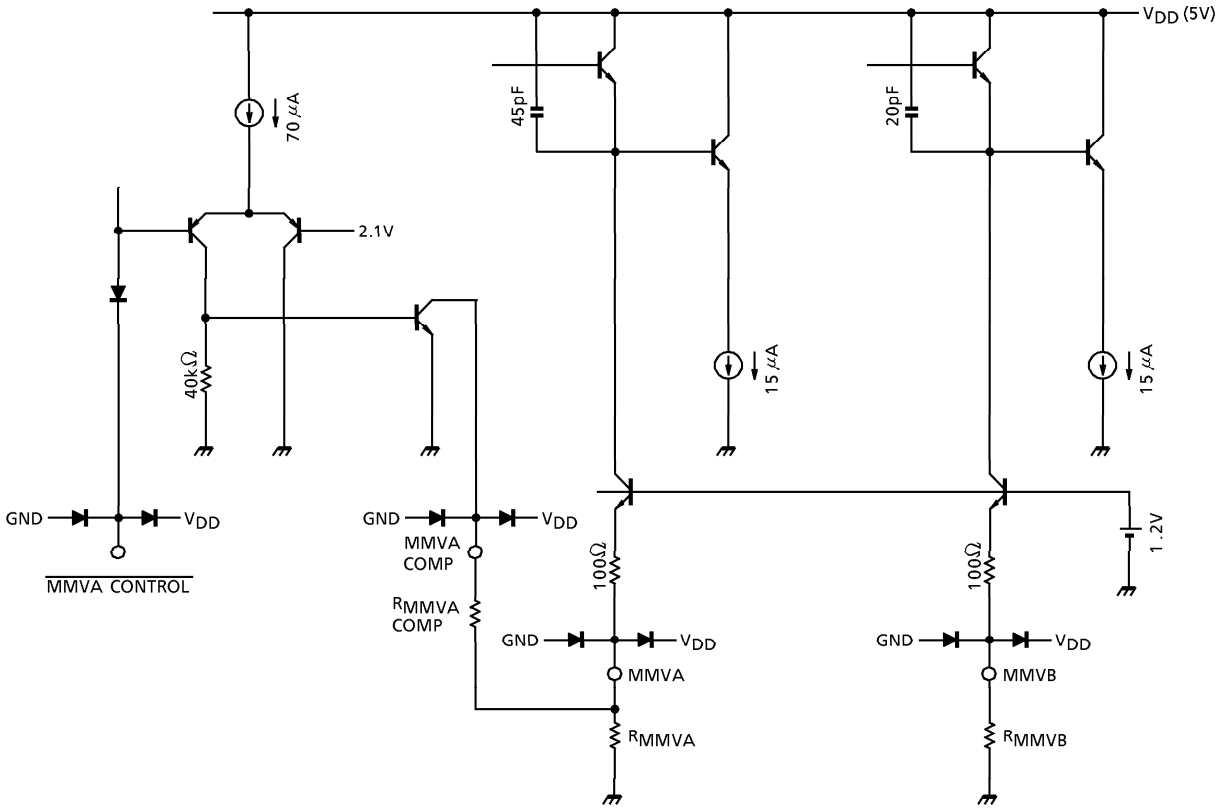
2. Differentiator



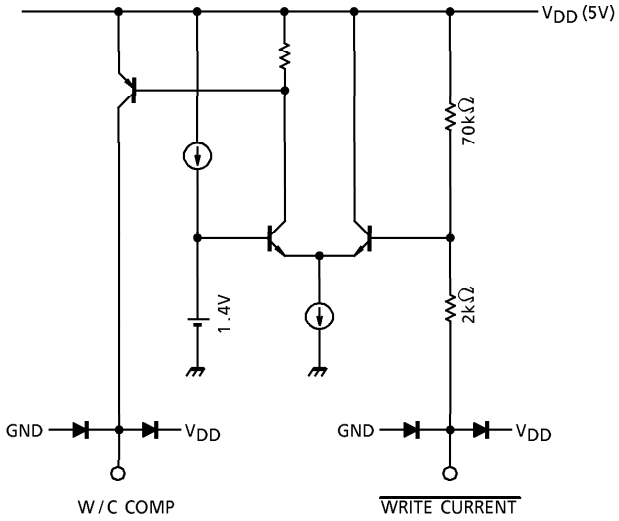
3. Comparator



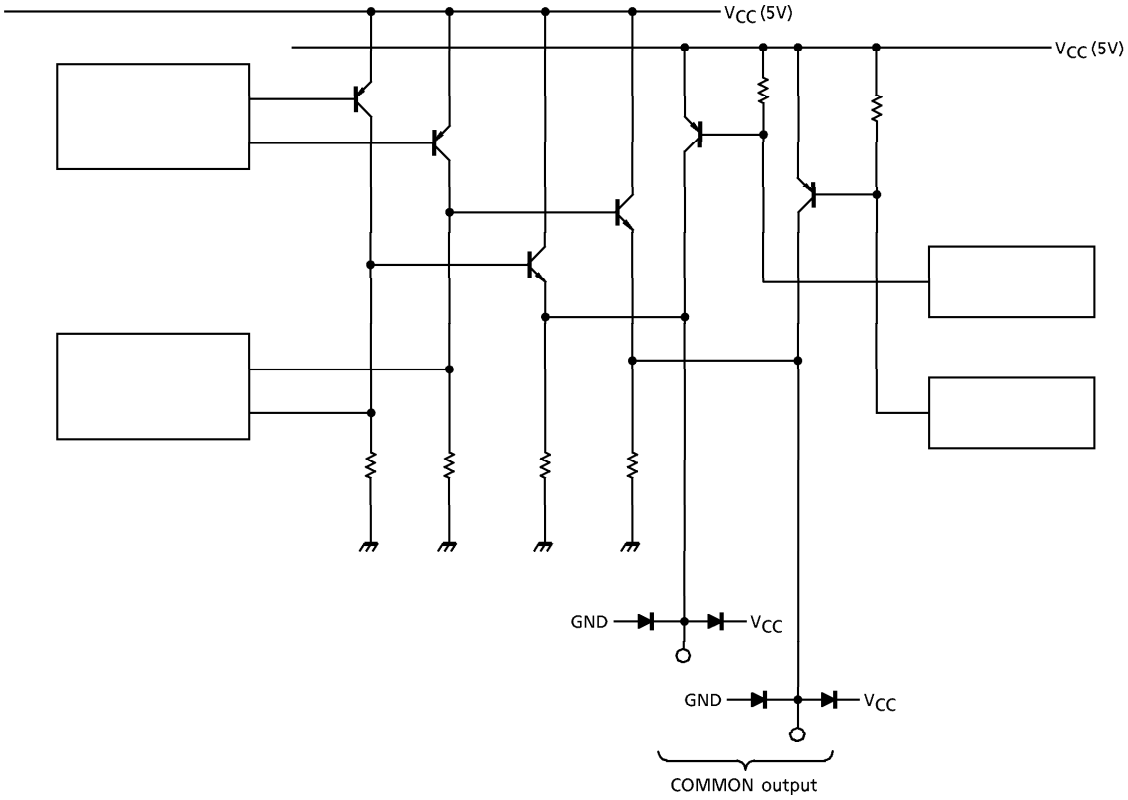
4. Time domain



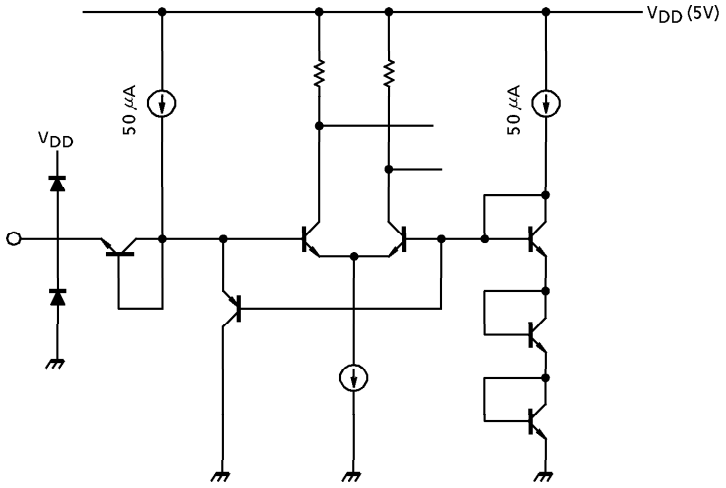
5. W / C control



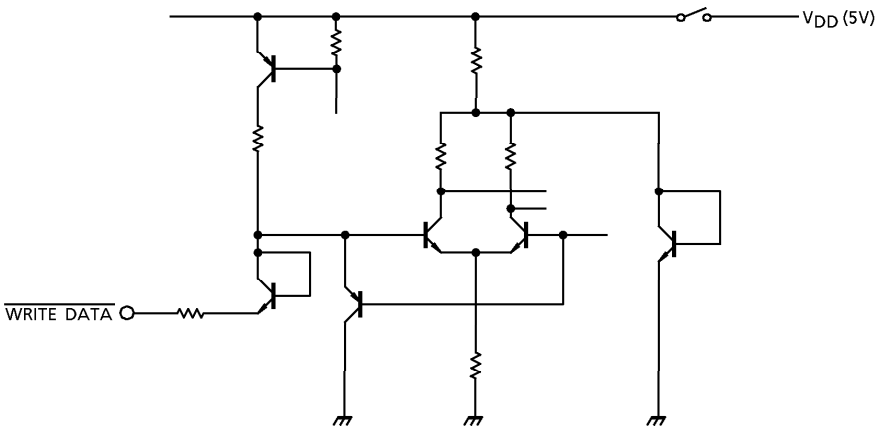
6. Common driver output



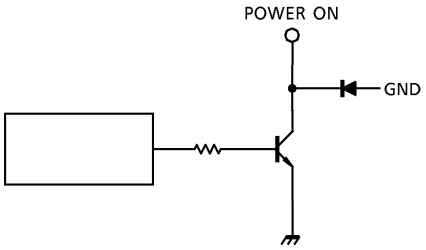
7. $\overline{\text{WRITE GATE}}$, $\overline{\text{ERASE GATE}}$, $\overline{\text{SIDE1}}$ interface pins



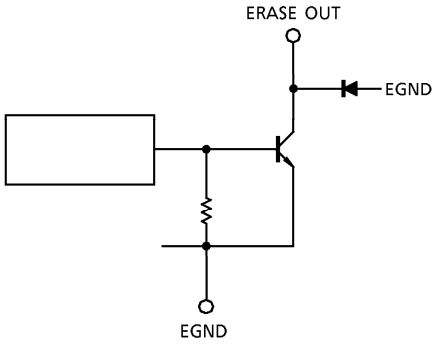
8. $\overline{\text{WRITE DATA}}$ interface pin



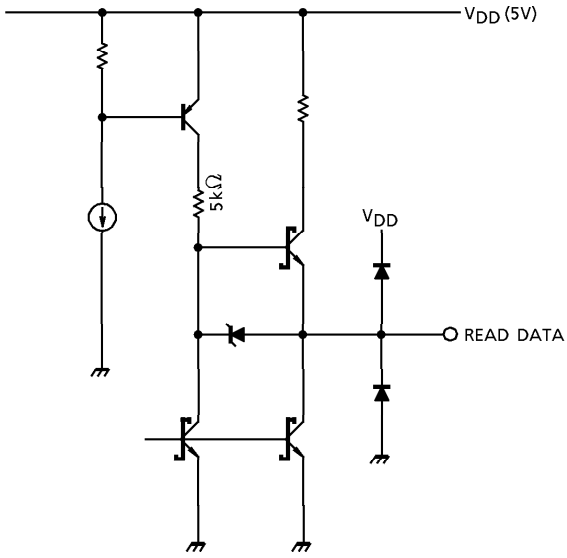
9. Power monitor output



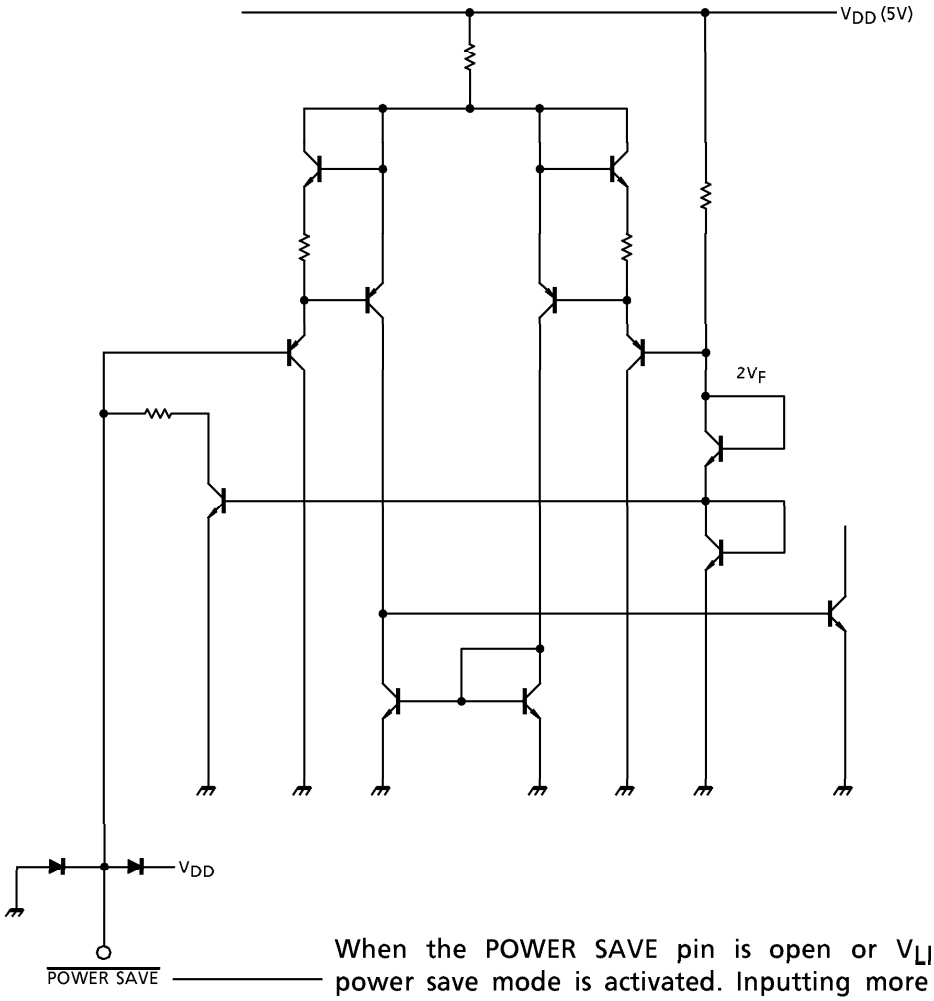
10. Erase output



11. Read data output



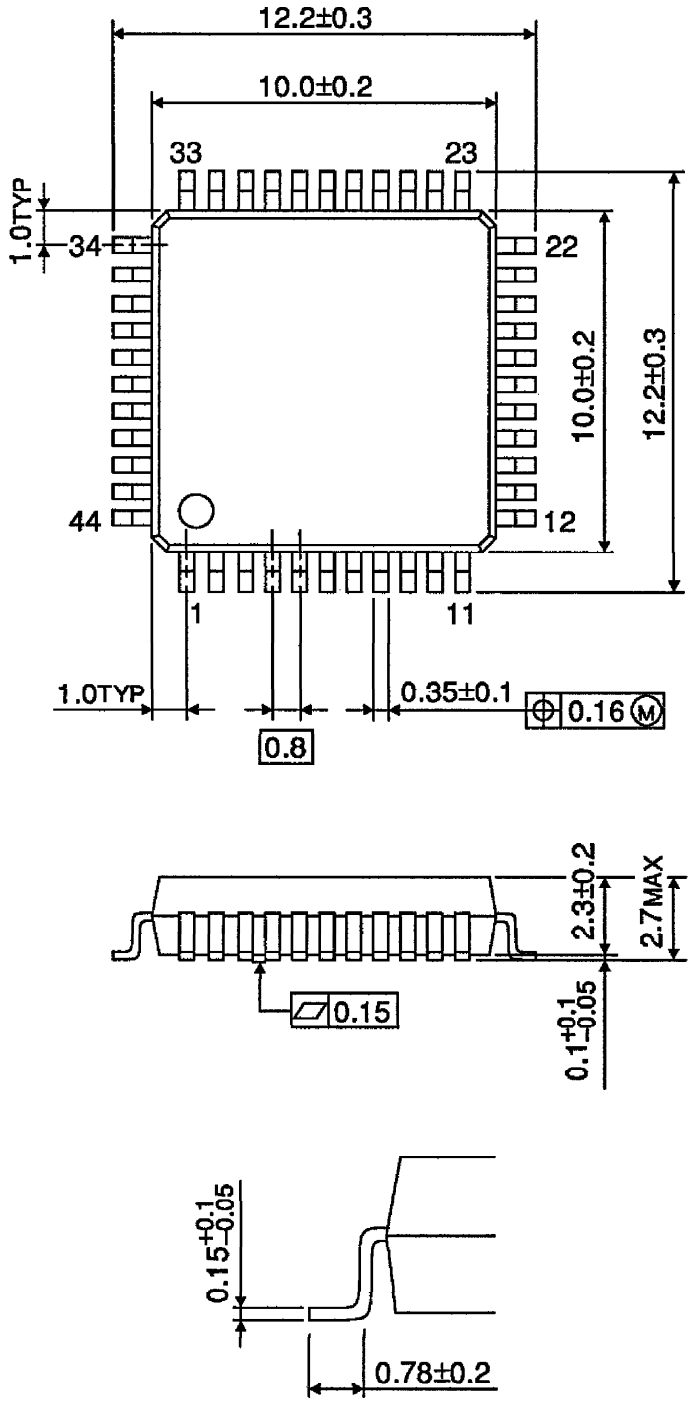
12. $\overline{\text{POWER SAVE}}$ interface pin



When the POWER SAVE pin is open or V_{LIN} or less V_{LIN} input, power save mode is activated. Inputting more than V_{HIN} deactivates power save mode.

PACKAGE DIMENSIONS

QFP44-P-1010-0.80B Unit : mm



Weight : 0.56g (Typ.)

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000707EBA

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