3 A, 2 MHz Buck-Regulating LED Driver

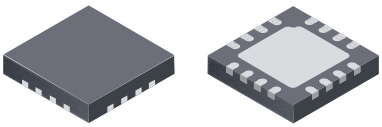
Features and Benefits

- User-configurable on-time, achieving switching frequencies up to 2.0 MHz
- Brightness control through PWM of DIS pin
- Minimal external components required
- No output capacitor required
- Wide input voltage range: 9 to 46 V
- Low 0.18 V sense voltage for higher efficiency
- Output Current: up to 3.0 A
- Low standby current <100 µA
- Thermal shutdown
- Supplied in a thermally-enhanced 4 mm QFN package

Applications:

- High brightness LEDs
- LED driver modules, power supplies and lamps, such as MR16 and MR11

Package 16-contact QFN (suffix EU):



4 mm × 4 mm × 0.75 mm

Description

The A6210 is a buck regulator that uses valley current-mode control. This control scheme allows very short switch on-times to be achieved, making it ideal for applications that require high switching frequencies combined with high input voltages and low output LED span voltages.

Low system cost is accomplished through high switching frequencies of up to 2.0 MHz, allowing smaller and lower value inductors and capacitors. In addition, few external components are required through high levels of integration. Optimal drive circuits minimize switching losses.

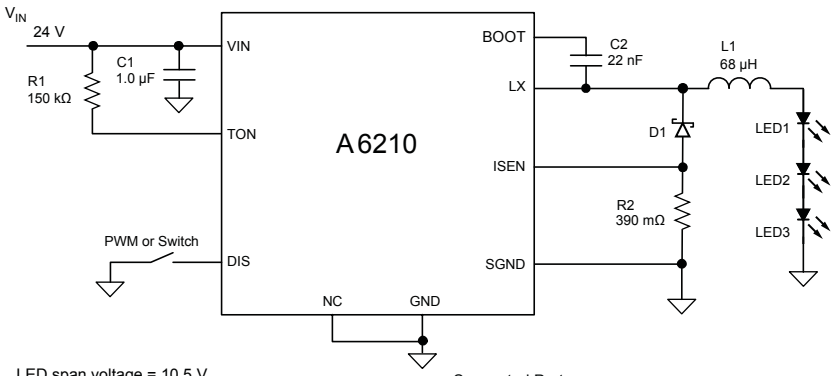
The switching frequency is maintained constant, as the on-time is modulated by the input voltage. This feed-forward control ensures excellent line correction. The on-time is set by an external resistor pulled-up to the input supply.

Internal housekeeping and bootstrap supplies are provided which require the addition of only one small ceramic capacitor. A top-off charge pump ensures correct operation at light loads.

Internal diagnostics provide comprehensive protection against input undervoltages and overtemperatures.

The device package is a 16-contact, 4 mm × 4 mm, 0.75 mm nominal overall height QFN, with exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte tin leadframe plating.

Typical Application



LED span voltage = 10.5 V
Average LED current = 500 mA
Peak to peak current = 60 mA
Switching frequency = 1.4 MHz
Efficiency = 90.5%

Suggested Parts

Name	Description	Manufacturer - Part Number
C1	1 µF, 25V, X5R or X7R ceramic, 1210	Taiyo Yuden, TDK
C2	22 nF, 50V, X5R or X7R ceramic, 0805	
D1	1 A, 30 V, Schottky diode	
L1	68 µH, 1 A inductor	Taiyo Yuden - NR 6045T 680M
R1	180 kΩ, 1%, 0805	
R2	390 mΩ, 1%, 0805	

Selection Guide

Part Number	Packing	Package
A6210GEUTR-T	1500 pieces per reel	16-contact 4 mm × 4 mm QFN with exposed thermal pad

Absolute Maximum Ratings (reference to GND)

Characteristic	Symbol	Notes	Rating	Units
VIN Pin Supply Voltage	V_{IN}		–0.3 to 50	V
LX Pin Switching Node Voltage	V_{LX}		–1 to 50	V
ISEN Pin Current Sense Voltage	V_{ISEN}		–1.0 to 0.5	V
DIS Pin Disable Voltage	V_{DIS}		–0.3 to 7	V
TON Pin On-Time Voltage	V_{TON}		–0.3 to 50	V
Operating Ambient Temperature	T_A	Range G	–40 to 105	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Recommended Operating Conditions

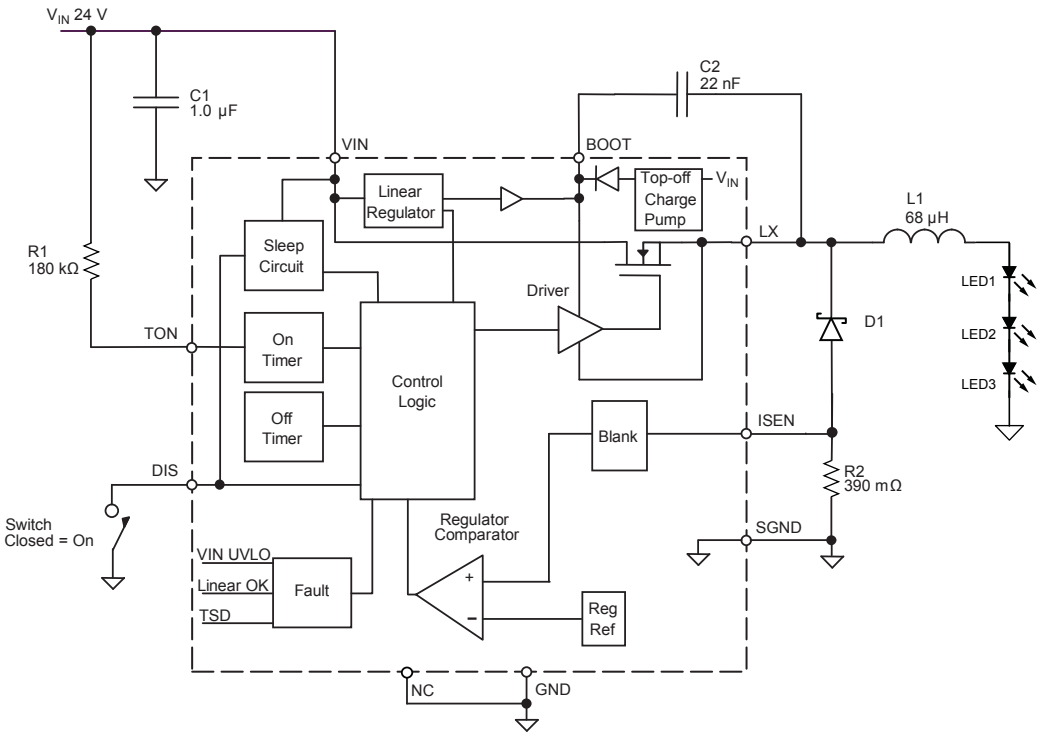
Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{IN}		9	–	46	V
Switching Node	V_{LX}		–0.7	–	46	V
Switching Frequency Range	f_{SW}	Continuous conduction mode	0.1	–	2.0	MHz
Operating Ambient Temperature	T_A		–40	–	105	ºC
Junction Temperature	T_J		–40	–	125	ºC

Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	36	ºC/W
Package Thermal Resistance, Junction to Pad	$R_{\theta JP}$	On 4-layer PCB based on JEDEC standard	2	ºC/W

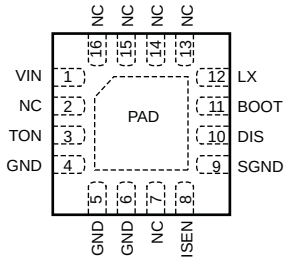
*Additional thermal information available on the Allegro website.

Functional Block Diagram



Switching Frequency = 1.4 MHz
All capacitors are X5R or X7R ceramic
Resistor R2 should be surface mount, low inductance type, rated at 250 mW at 70°C

Pin-out Diagram



(Top View)

Terminal List Table

Number	Name	Function
1	VIN	Input supply
2, 7, 13, 14, 15, 16	NC	No connection; tie to GND
3	TON	Terminal for on-time setting with external resistor
4, 5, 6	GND	Ground terminal
8	ISEN	Current sense input
9	SGND	Current sense ground reference
10	DIS	Disable/enable logic input; active high
11	BOOT	Bootstrap supply node
12	LX	Switch node
–	PAD	Exposed thermal pad; connect to ground plane (GND) by through-hole vias

ELECTRICAL CHARACTERISTICS* valid at T_J = 25°C, V_{IN} = 9 to 46 V, unless otherwise noted

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Units
General						
V_{IN} Quiescent Current	I_{VINOFF}	DIS = high, VIN = 46 V	–	–	100	µA
Current Sense Voltage	V_{SENSE}		176	183	190	mV
On-Time Tolerance	ΔT_{ON}	Based on selected value	–15	–	15	%
Minimum On-Time Period	$T_{on(min)}$		–	50	60	ns
Minimum Off-Time Period	$T_{off(min)}$		–	–	350	ns
Start-Up Time	t_{START}	Using application circuit on page 1; time from application of $\overline{DIS}$ (enable) to reaching target current	–	15	–	µs
Buck Switch On-Resistance	$R_{DS(on)}$	T_J = 25°C, I_{LOAD} = 3 A	–	350	–	mΩ
		T_J = 125°C, I_{LOAD} = 3 A	–	550	–	mΩ
Input						
DIS Input Voltage Threshold	V_{DIS}	Device enabled	–	–	1	V
DIS Open-Circuit Voltage	V_{DISOC}	Device disabled	2	–	7	V
DIS Input Current	I_{IN}	DIS = 0 V	–10	–	–1	µA
Protection						
VIN Undervoltage Shutdown Threshold	V_{INUV}	Voltage rising	6.3	–	7.5	V
VIN Undervoltage Shutdown Hysteresis	$V_{INUV(hys)}$		0.7	–	1.1	V
Overtemperature Shutdown Threshold	T_{JTSD}	Temperature rising	–	165	–	°C
Overtemperature Shutdown Hysteresis	$T_{JTSD(hys)}$	Recovery = $T_{JTSD} - T_{JTSD(hys)}$	–	15	–	°C

*Specifications over the junction temperature range of –40°C to 125°C are assured by design and characterization.

Functional Description

Basic Operation

The A6210 is a buck regulator that utilizes valley current mode control. The on-time is set by the amount of current that flows into the TON pin. This is determined by the value of the TON resistor chosen (R1 in the Functional Block diagram) and the magnitude of the input voltage, V_{IN}. Under a specific set of conditions, an on-time can be set that then dictates the switching frequency. This switching frequency remains reasonably constant throughout load and line conditions as the on-time varies inversely with the input voltage.

At the beginning of the switching cycle, the buck switch is turned on for a fixed period that is determined by the current flowing into TON. Once the current comparator trips, a one-shot monostable, the On Timer, is reset, turning off the switch. The current through the inductor then decays. This current is sensed through the external sense resistor (R2), and then compared against the current-demand signal. After the current through the sense resistor decreases to the valley of the current-demand signal, the On Timer is set to turn the buck switch back on again and the cycle is repeated.

Disable/Enable The regulator is enabled by pulling the DIS pin low. To disable the regulator, the DIS pin can simply be disconnected (open circuit).

Shutdown The regulator is disabled in the event of either an overtemperature event, or an undervoltage on VIN (V_{INUV}) or on an internal housekeeping supply.

As soon as any of the above faults have been removed and assuming DIS = 0, the output is restored.

Switch On Time and Switching Frequency The switch on-time effectively determines the operating frequency of the converter. To minimize the size of the power inductor and input filtering it is recommended to run with as high a frequency as possible. The MOSFET drivers are optimized to minimize switching losses.

An important consideration in selecting the switching frequency is to ensure that the on time (60 ns) and off time (350 ns) limitations are not reached under extreme conditions:

- the minimum on time occurs at maximum input voltage
- the minimum off time occurs at minimum input voltage

The following table takes into account the above maximum off time figure and outlines the typical switching frequencies that can be achieved for a given number of LEDs and input voltage. Note that it is highly recommended that worst case values are used when considering any design.

Switching Frequency (MHz)	Input Voltage					
	12 V		24 V		36 V	
	Quantity of LEDs	LED Span Voltage (V)	Quantity of LEDs	LED Span Voltage (V)	Quantity of LEDs	LED Span Voltage (V)
2.0	1	3.5	2	7.0	3	10.5
1.7	1	3.5	3	10.5	4	14.0
1.0	2	7.0	4	14.0	6	21.0
0.300	3	10.5	6	21.0	9	31.5

The switch on time is programmed by the current flowing into the TON pin. The current is determined by the input voltage, V_{IN}, and the resistor, R1. The on time, T_{on}, can be found:

$$T_{on} = \frac{R_1}{V_{IN} \times 2.05 \times 10^{10}} + 10 \times 10^{-9} \quad . \qquad (1)$$

To calculate the actual switching frequency, f_{sw}, the T_{on} from the above calculation can be used in conjunction with the transfer function of the converter, as follows:

$$f_{SW} = \frac{V_{OUT} + V_f}{V_{IN} + V_f} \times \frac{1}{T_{on}} \quad . \qquad (2)$$

A simplified approach to selecting the T_{on} resistor (R1), to accomplish an approximate switching frequency, can be found from the following formula:

$$R_1 = \frac{V_{IN} \times 2.05 \times 10^{10}}{f_{SW}} \quad . \qquad (3)$$

Figure 1 illustrates a range of switching frequencies that can be achieved with a given resistor and LED voltage. Each LED is assumed to have a voltage drop of 3.5 V.

High Brightness LED Driving

The A6210 can be configured as a very simple, low cost, high brightness LED driver. The solution can drive high brightness LEDs up to more than 3 A, while achieving very high efficiencies, in excess of 90%.

The solution uses valley current mode control. This architecture is optimized for high switching frequencies, allowing the use

of physically small, low value inductors. An output capacitor is not necessary either to reduce the ripple current or to close the control loop.

High efficiencies are achieved via drive circuits optimized to minimize switching losses and the current sense voltage has a typical voltage drop of only 183 mV. The current in the LED string can be pulse width modulated (PWM) via the DIS (Disable/Enable) pin. See figure 4.

The actual current control is maintained on the valley of the current ripple. The average LED current is the valley level plus half the inductor ripple current, as shown in figure 2.

To avoid potential mistriggering issues, it is recommended that the ripple current that flows through the sense resistor (R2) does not develop a ripple voltage of less than 20 mV.

The average LED current can be found from:

$$I_{av} = I_{VALLEY} + \frac{I_{RIPPLE}}{2} \quad , \tag{4}$$

substituting values:

$$I_{av} = \frac{183\ mV}{R2} + \left(\frac{1}{2} \times \frac{V_{IN} - V_{LED}}{L} \times t_{on} \right) \quad , \tag{5}$$

where:

$$t_{on} = \frac{V_{LED} + V_f}{V_{IN} + V_f} \times \frac{1}{f_{SW}} \quad . \tag{6}$$

Note: V_f is the forward voltage drop of the recirculation diode and sense resistor (R2). The valley current is determined by the sense voltage (183 mV) divided by the sense resistor.

Worked example

This example uses the brief specification outlined in the typical application circuit on page 1. The following information is used as a starting point:

V_{IN} = 24 V ,

3 LEDs producing V_{LED} = 12 V ,

I_{LED} = 500 mA, and

LED ripple current, I_{RIPPLE} = 60 mA .

The duty cycle can be found initially. Assume the forward voltage drop of the re-circulation diode is 400 mV, and that the sense resistor is 183 mV. Then:

$$D = \frac{V_{LED} + V_f}{V_{IN} + V_f} = \frac{12 + 0.58}{24 + 0.58} = 0.39 \quad . \tag{7}$$

One of the objectives is to maximize the switching frequency to minimize the inductor value. When driving at very high switching frequencies, the duty cycle may be limited due to the minimum

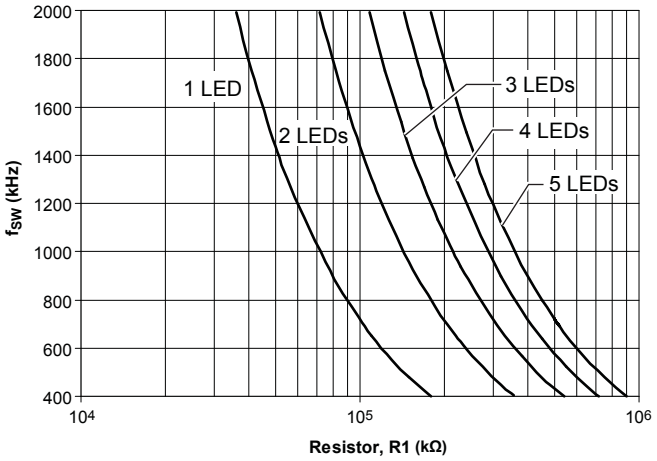


Figure 1. Switching frequency versus value of external resistor R1 on the TON pin.

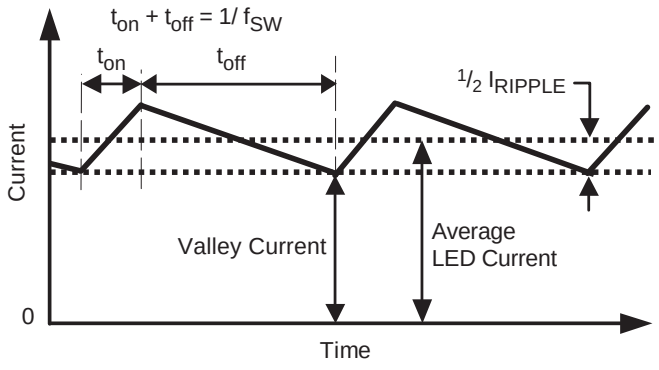


Figure 2. Current control

off-time of 350 ns. A minimum off-time is required to ensure the bootstrap supply operates correctly. It can be shown that:

$$f_{SW} = \frac{1 - D}{t_{off}\,(\text{min})} \quad , \tag{8}$$

where t_{off} is 350 ns maximum.

Therefore:

$$f_{SW} = \frac{1 - 0.51}{350 \times 10^{-9}} = 1.4 \text{ MHz} \quad .$$

The t_{on} resistor (R1) value can be found:

$$R_1 = \frac{V_{LED} \times 2.051 \times 10^{10}}{f_{SW}} = \frac{12 \times 2.051 \times 10^{10}}{1.4 \times 10^{6}} = 176 \times 10^{3} \quad . \tag{9}$$

Choose R1 = 180 kΩ.

The inductor (L1) can now be found using the target LED ripple current of 60 mA:

$$L_1 = \frac{(V_{IN} - V_{LED}) \times D}{I_{RIPPLE} \times f_{SW}} = \frac{(24 - 12) \times 0.51}{60 \times 10^{-3} \times 1.4 \times 10^{6}} = 72 \times 10^{-6} \quad . \tag{10}$$

Choose L1 = 68 µH.

The inductor current rating should exceed the average current plus half of the ripple current. In addition, it is recommended that a margin of at least 20% be allowed. In this example, the inductor current rating, I_L, should be:

$$I_L \geq 1.2 \times (500 \times 10^{-3} + 60 \times 10^{-3} / 2) = 636 \text{ mA} \quad .$$

The valley control current is simply the average LED current minus half the ripple current. Therefore:

$$I_{VALLEY} = I_{av} - \frac{I_{RIPPLE}}{2} = 500 \times 10^{-3} - \frac{60 \times 10^{-3}}{2} = 470 \text{ mA} \quad . \tag{11}$$

The sense resistor (R3) value can be found:

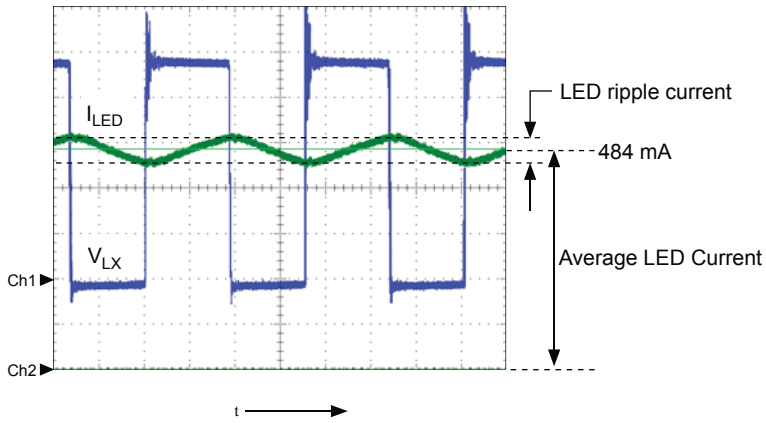
$$R_3 = \frac{V_{SENSE}}{I_{VALLEY}} = \frac{183 \times 10^{-3}}{470 \times 10^{-3}} = 0.36 \quad . \tag{12}$$

Choose R3 = 390 mΩ.

The ripple voltage developed across the sense resistor (R2) is 60 mA × 390 mΩ = 23 mV, which is greater than the minimum required value of 20 mV.

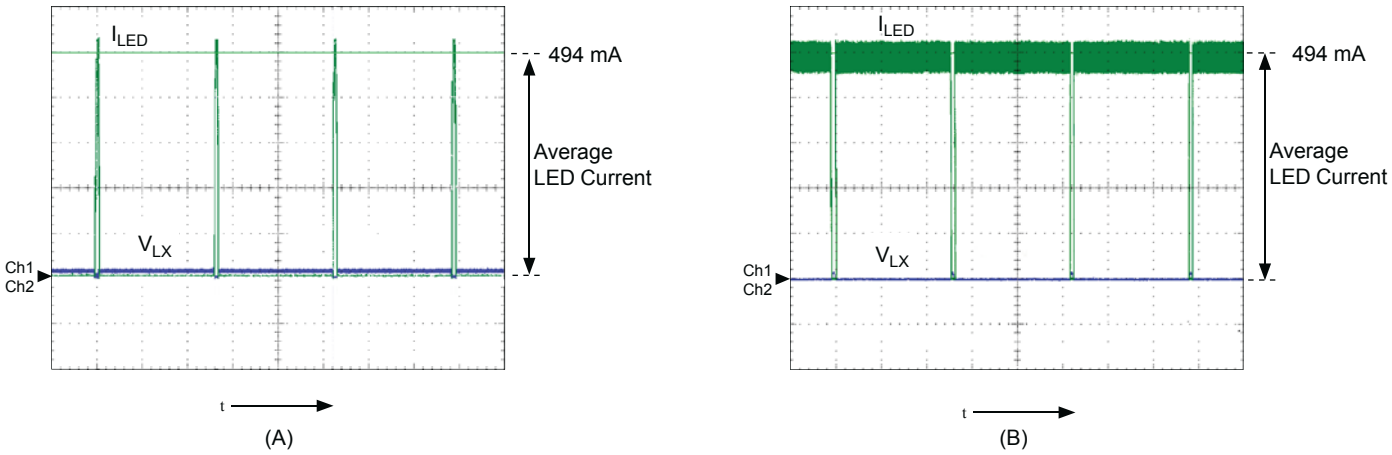
Measured switching waveforms

From figure 3, it can be seen that the average current through the LED string is 484 mA. This represents an error of 3.2% with respect to the target current of 500 mA.



Symbol	Parameter	Units/Division
Ch1	V_{LX}	5 V
Ch2	I_{LED}	100 mA
t	time	200 ns

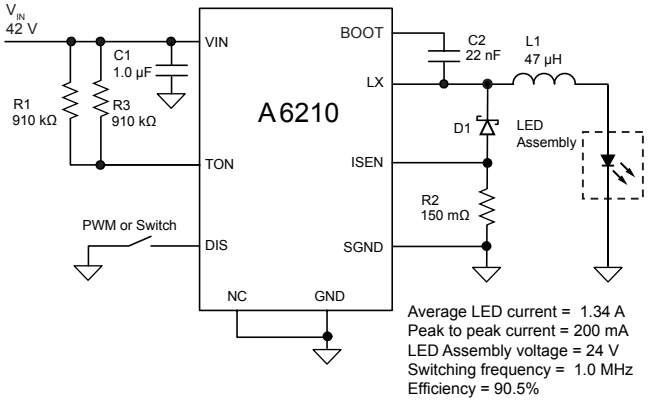
Figure 3. Switching voltage versus current through L1 and LED string



Symbol	Parameter	Units/Division
Ch1	V_{LX}	5 V
Ch2	I_{LED}	100 mA
t	time	1 ms

Figure 4. PWM on DIS pin at 400 Hz: (A) narrow duty cycle, (B) wide duty cycle.

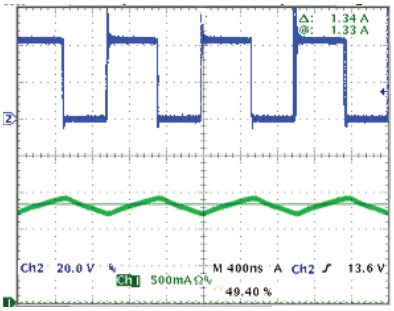
Other Application Circuits
Application Circuit 1



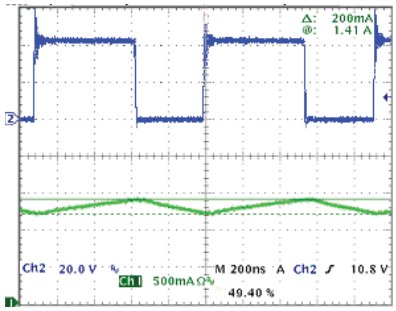
Suggested Parts

Name	Description	Manufacturer - Part Number
C1	1 µF, 25V, X5R or X7R ceramic, 1210	Taiyo Yuden, TDK
C2	22 nF, 50V, X5R or X7R ceramic, 0805	
D1	3 A, 60 V, Schottky diode	
L1	47 µH, 1.4 A inductor	Taiyo Yuden - NR 8040T 470M
R1, R3	910 kΩ, 1%, 0603	
R2	150 mΩ, 1%, 1206	

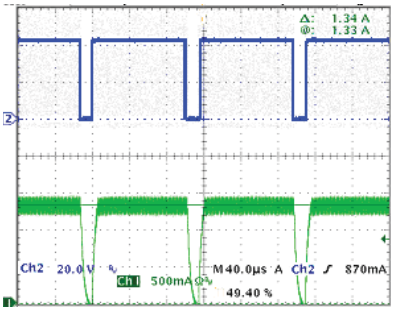
Channel 1 – Current through inductor and LED Assembly, Channel 2 – Main switching voltage (LX node)



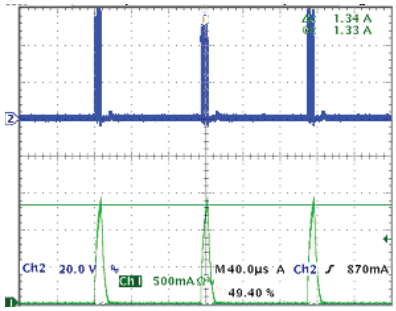
Plot 1. Average current = 1.34 A



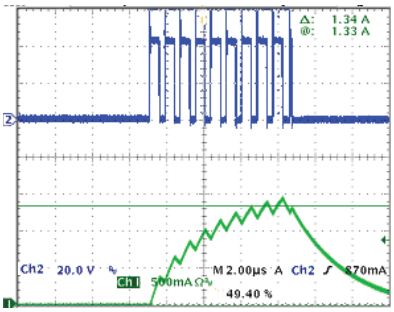
Plot 2. Peak to peak current = 200 mA



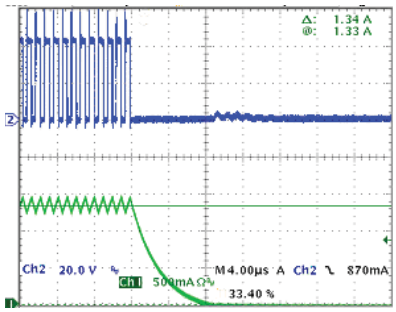
Plot 3. PWM frequency = 10 kHz, maximum duty cycle



Plot 4. PWM frequency = 10 kHz, minimum duty cycle

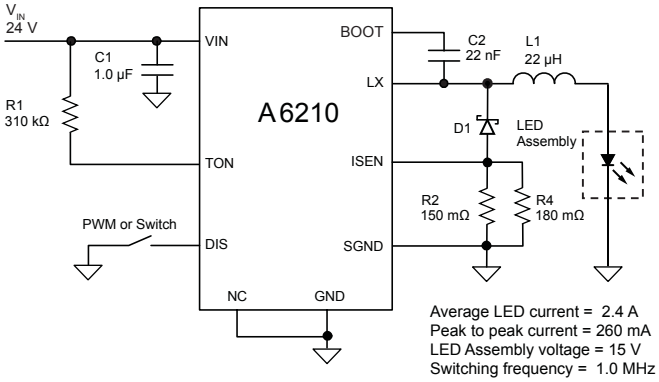


Plot 5. Plot 4 with expanded time scale



Plot 6. PWM frequency = 10 kHz, turn off

Application Circuit 2

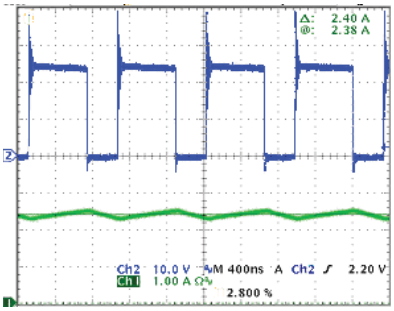


Average LED current = 2.4 A
Peak to peak current = 260 mA
LED Assembly voltage = 15 V
Switching frequency = 1.0 MHz
Efficiency = 94%

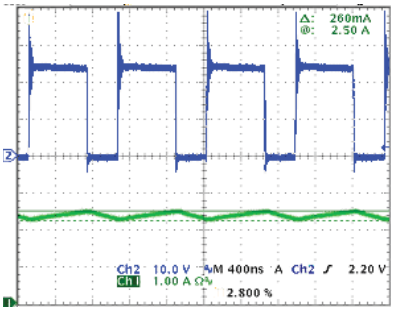
Suggested Parts

Name	Description	Manufacturer - Part Number
C1	1 µF, 25V, X5R or X7R ceramic, 1210	Taiyo Yuden, TDK
C2	22 nF, 50V, X5R or X7R ceramic, 0805	
D1	3 A, 60 V, Schottky diode	
L1	22 µH, 2.8 A inductor	Coilcraft - MSS1048-223ML
R1	310 kΩ, 1%, 0603	
R2	150 mΩ, 1%, 0805	
R4	180 mΩ, 1%, 0805	

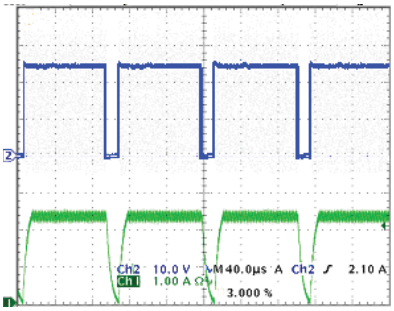
Channel 1 – Current through inductor and LED Assembly, Channel 2 – Main switching voltage (LX node)



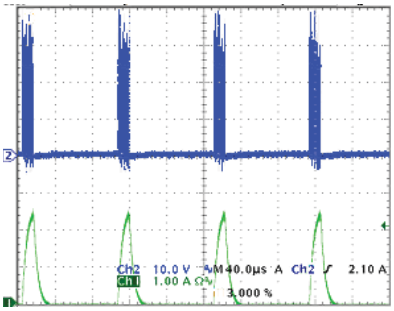
Plot 1. Average current = 2.4 A



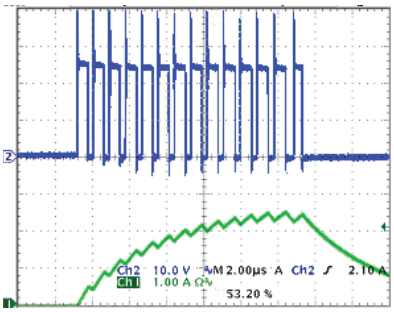
Plot 2. Peak to peak current = 260 mA



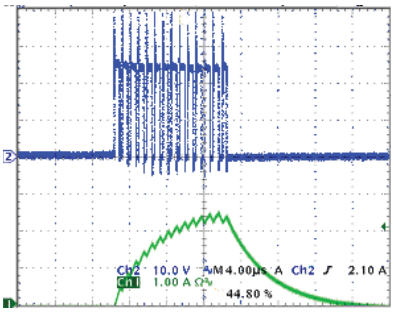
Plot 3. PWM frequency = 10 kHz, maximum duty cycle



Plot 4. PWM frequency = 10 kHz, minimum duty cycle

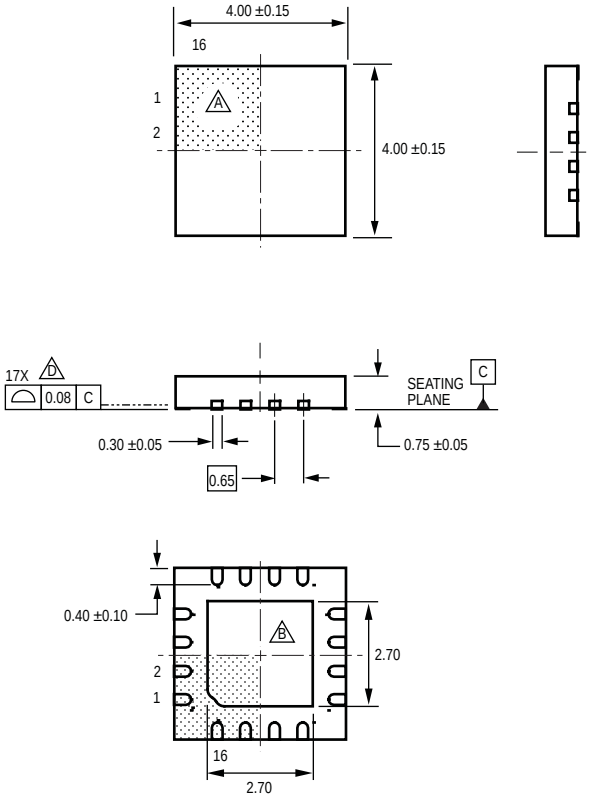


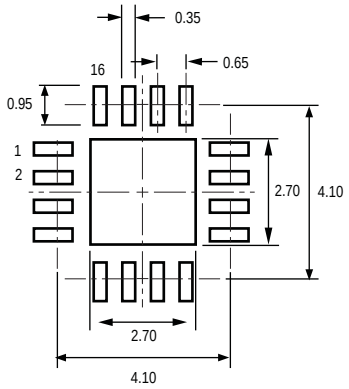
Plot 5. Plot 4 with expanded time scale



Plot 6. PWM frequency = 10 kHz, turn off

Package EU, 16-Contact QFN





C PCB Layout Reference View

For Reference Only
(reference JEDEC MO-220WGGC)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN65P400X400X80-17W2M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Revision History

Revision	Revision Date	Description of Revision
Rev. 2	May 2, 2011	Minor edit

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