

# DATA SHEET

**PSMN005-55B; PSMN005-55P**

N-channel logic level

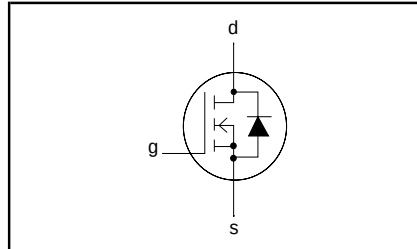
TrenchMOS<sup>(TM)</sup> transistor

Product specification

October 1999

**SiliconMAX****N-channel logic level TrenchMOS<sup>(TM)</sup> transistor****PSMN005-55B;  
PSMN005-55P****FEATURES**

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Low thermal resistance

**SYMBOL****QUICK REFERENCE DATA**

$$V_{DSS} = 55 \text{ V}$$

$$I_D = 75 \text{ A}$$

$$R_{DS(ON)} \leq 5.8 \text{ m}\Omega \text{ (} V_{GS} = 10 \text{ V)}$$

$$R_{DS(ON)} \leq 6.3 \text{ m}\Omega \text{ (} V_{GS} = 5 \text{ V)}$$

**GENERAL DESCRIPTION**

SiliconMAX products use the latest Philips Trench technology to achieve the lowest possible on-state resistance in each package at each voltage rating.

**Applications:-**

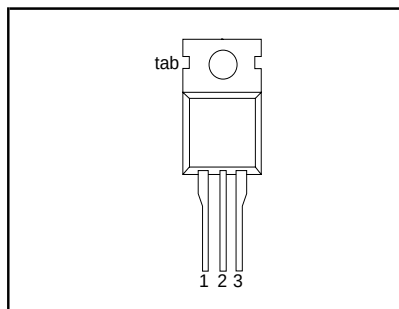
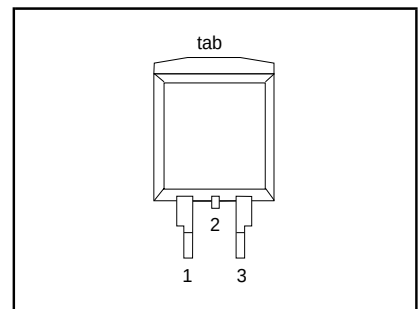
- d.c. to d.c. converters
- switched mode power supplies

The PSMN005-55P is supplied in the SOT78 (TO220AB) conventional leaded package.

The PSMN005-55B is supplied in the SOT404 surface mounting package.

**PINNING**

| PIN | DESCRIPTION        |
|-----|--------------------|
| 1   | gate               |
| 2   | drain <sup>1</sup> |
| 3   | source             |
| tab | drain              |

**SOT78 (TO220AB)****SOT404 (D<sup>2</sup>PAK)****LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL         | PARAMETER                                  | CONDITIONS                                                                      | MIN. | MAX.            | UNIT             |
|----------------|--------------------------------------------|---------------------------------------------------------------------------------|------|-----------------|------------------|
| $V_{DSS}$      | Drain-source voltage                       | $T_j = 25^\circ\text{C}$ to $175^\circ\text{C}$                                 | -    | 55              | V                |
| $V_{DGR}$      | Drain-gate voltage                         | $T_j = 25^\circ\text{C}$ to $175^\circ\text{C}$ ; $R_{GS} = 20 \text{ k}\Omega$ | -    | 55              | V                |
| $V_{GS}$       | Continuous gate-source voltage             |                                                                                 | -    | $\pm 15$        | V                |
| $V_{GSM}$      | Peak pulsed gate-source voltage            | $T_j \leq 150^\circ\text{C}$                                                    | -    | $\pm 20$        | V                |
| $I_D$          | Continuous drain current                   | $T_{mb} = 25^\circ\text{C}$ ; $V_{GS} = 5 \text{ V}$                            | -    | 75 <sup>2</sup> | A                |
|                |                                            | $T_{mb} = 100^\circ\text{C}$ ; $V_{GS} = 5 \text{ V}$                           | -    | 75 <sup>2</sup> | A                |
| $I_{DM}$       | Pulsed drain current                       | $T_{mb} = 25^\circ\text{C}$                                                     | -    | 240             | A                |
| $P_D$          | Total power dissipation                    | $T_{mb} = 25^\circ\text{C}$                                                     | -    | 230             | W                |
| $T_j, T_{stg}$ | Operating junction and storage temperature |                                                                                 | - 55 | 175             | $^\circ\text{C}$ |

<sup>1</sup> It is not possible to make connection to pin:2 of the SOT404 package

<sup>2</sup> maximum current limited by package

**SiliconMAX**N-channel logic level TrenchMOS<sup>(TM)</sup> transistorPSMN005-55B;  
PSMN005-55P**THERMAL RESISTANCES**

| SYMBOL         | PARAMETER                                    | CONDITIONS                                                                   | TYP.     | MAX.   | UNIT       |
|----------------|----------------------------------------------|------------------------------------------------------------------------------|----------|--------|------------|
| $R_{th\ j-mb}$ | Thermal resistance junction to mounting base |                                                                              | -        | 0.65   | K/W        |
| $R_{th\ j-a}$  | Thermal resistance junction to ambient       | SOT78 package, in free air<br>SOT404 package, pcb mounted, minimum footprint | 60<br>50 | -<br>- | K/W<br>K/W |

**AVALANCHE ENERGY LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL   | PARAMETER                        | CONDITIONS                                                                                                                                                                                                                | MIN. | MAX. | UNIT |
|----------|----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|
| $E_{AS}$ | Non-repetitive avalanche energy  | Unclamped inductive load, $I_{AS} = 75\text{ A}$ ;<br>$t_p = 100\text{ }\mu\text{s}$ ; $T_j$ prior to avalanche = $25^\circ\text{C}$ ;<br>$V_{DD} \leq 15\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 5\text{ V}$ | -    | 268  | mJ   |
| $I_{AS}$ | Non-repetitive avalanche current |                                                                                                                                                                                                                           | -    | 75   | A    |

**ELECTRICAL CHARACTERISTICS** $T_j = 25^\circ\text{C}$  unless otherwise specified

| SYMBOL        | PARAMETER                        | CONDITIONS                                                                                                                                                                                                              | MIN.             | TYP.                 | MAX.                      | UNIT                                                 |
|---------------|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|----------------------|---------------------------|------------------------------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage   | $V_{GS} = 0\text{ V}$ ; $I_D = 0.25\text{ mA}$ ;<br>$T_j = -55^\circ\text{C}$                                                                                                                                           | 55<br>50         | -<br>-               | -<br>-                    | V<br>V                                               |
| $V_{GS(TO)}$  | Gate threshold voltage           | $V_{DS} = V_{GS}$ ; $I_D = 1\text{ mA}$ ;<br>$T_j = 175^\circ\text{C}$<br>$T_j = -55^\circ\text{C}$                                                                                                                     | 1.0<br>0.5<br>-  | 1.5<br>-<br>-        | 2.0<br>-<br>2.3           | V<br>V<br>V                                          |
| $R_{DS(ON)}$  | Drain-source on-state resistance | $V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$<br>$V_{GS} = 5\text{ V}$ ; $I_D = 25\text{ A}$<br>$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$<br>$V_{GS} = 5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 175^\circ\text{C}$ | -<br>-<br>-<br>- | 4.8<br>5.3<br>-<br>- | 5.8<br>6.3<br>6.7<br>13.2 | m $\Omega$<br>m $\Omega$<br>m $\Omega$<br>m $\Omega$ |
| $I_{GSS}$     | Gate source leakage current      | $V_{GS} = \pm 10\text{ V}$ ; $V_{DS} = 0\text{ V}$                                                                                                                                                                      | -                | 2                    | 100                       | nA                                                   |
| $I_{DSS}$     | Zero gate voltage drain current  | $V_{DS} = 55\text{ V}$ ; $V_{GS} = 0\text{ V}$ ;<br>$T_j = 175^\circ\text{C}$                                                                                                                                           | -                | 0.05                 | 10<br>500                 | $\mu\text{A}$<br>$\mu\text{A}$                       |
| $Q_{g(tot)}$  | Total gate charge                | $I_D = 75\text{ A}$ ; $V_{DD} = 44\text{ V}$ ; $V_{GS} = 5\text{ V}$                                                                                                                                                    | -                | 103                  | -                         | nC                                                   |
| $Q_{gs}$      | Gate-source charge               |                                                                                                                                                                                                                         | -                | 15                   | -                         | nC                                                   |
| $Q_{gd}$      | Gate-drain (Miller) charge       |                                                                                                                                                                                                                         | -                | 52                   | -                         | nC                                                   |
| $t_{d\ on}$   | Turn-on delay time               | $V_{DD} = 30\text{ V}$ ; $R_D = 1.2\text{ }\Omega$ ;<br>$V_{GS} = 5\text{ V}$ ; $R_G = 10\text{ }\Omega$                                                                                                                | -                | 45                   | -                         | ns                                                   |
| $t_r$         | Turn-on rise time                |                                                                                                                                                                                                                         | -                | 180                  | -                         | ns                                                   |
| $t_{d\ off}$  | Turn-off delay time              | Resistive load                                                                                                                                                                                                          | -                | 420                  | -                         | ns                                                   |
| $t_f$         | Turn-off fall time               |                                                                                                                                                                                                                         | -                | 235                  | -                         | ns                                                   |
| $L_d$         | Internal drain inductance        | Measured from tab to centre of die                                                                                                                                                                                      | -                | 3.5                  | -                         | nH                                                   |
| $L_d$         | Internal drain inductance        | Measured from drain lead to centre of die (SOT78 package only)                                                                                                                                                          | -                | 4.5                  | -                         | nH                                                   |
| $L_s$         | Internal source inductance       | Measured from source lead to source bond pad                                                                                                                                                                            | -                | 7.5                  | -                         | nH                                                   |
| $C_{iss}$     | Input capacitance                | $V_{GS} = 0\text{ V}$ ; $V_{DS} = 25\text{ V}$ ; $f = 1\text{ MHz}$                                                                                                                                                     | -                | 6500                 | -                         | pF                                                   |
| $C_{oss}$     | Output capacitance               |                                                                                                                                                                                                                         | -                | 1500                 | -                         | pF                                                   |
| $C_{rss}$     | Feedback capacitance             |                                                                                                                                                                                                                         | -                | 700                  | -                         | pF                                                   |



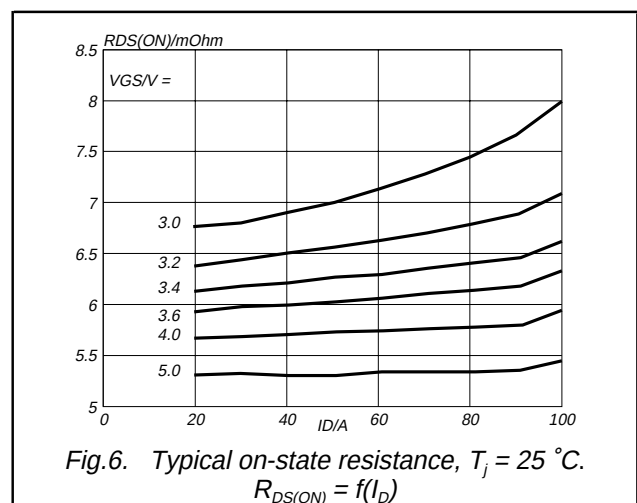
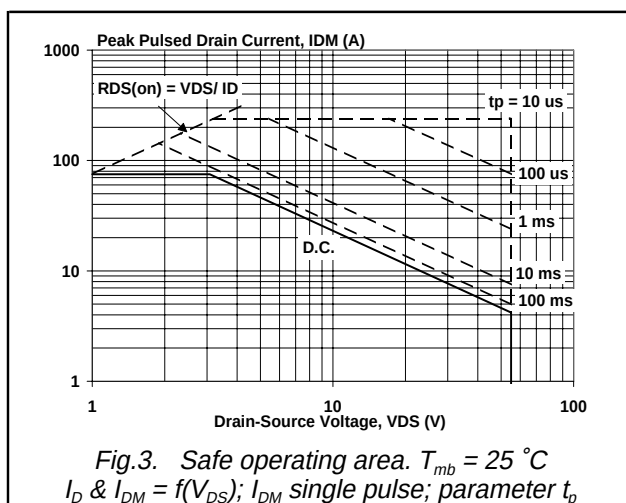
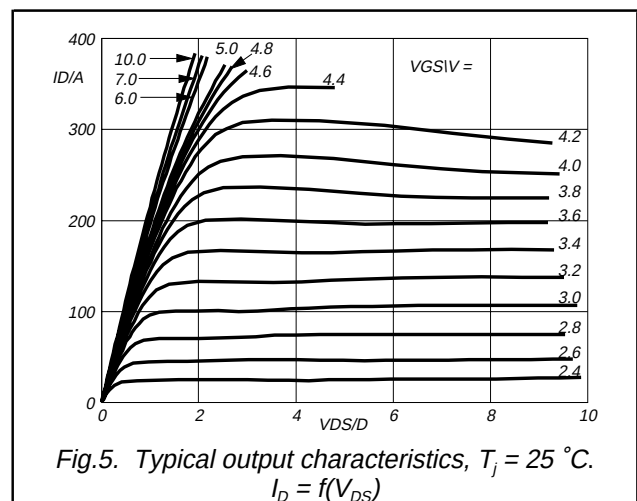
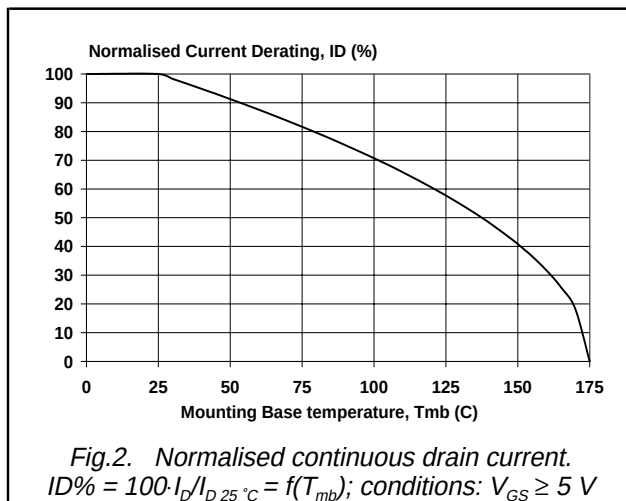
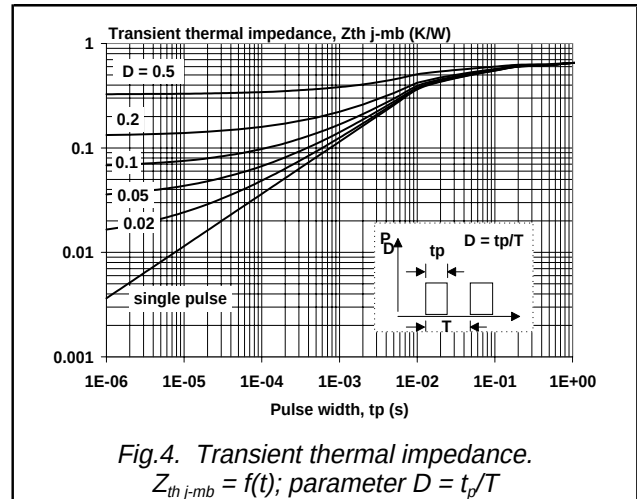
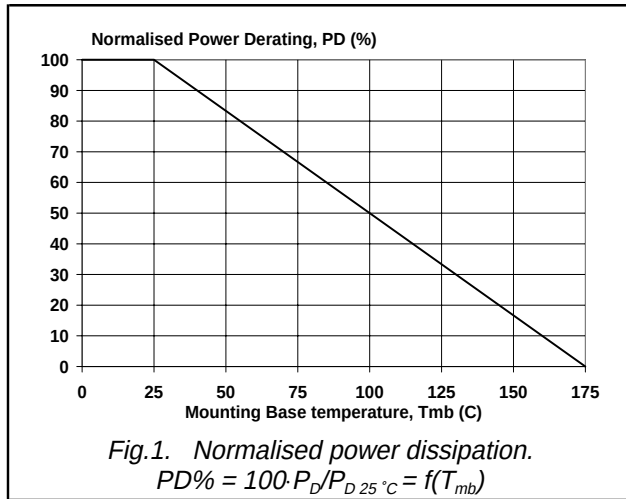
N-channel logic level TrenchMOS<sup>(TM)</sup> transistor

PSMN005-55B;  
PSMN005-55P

## REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25^\circ\text{C}$  unless otherwise specified

| SYMBOL   | PARAMETER                              | CONDITIONS                                                | MIN. | TYP. | MAX. | UNIT          |
|----------|----------------------------------------|-----------------------------------------------------------|------|------|------|---------------|
| $I_S$    | Continuous source current (body diode) |                                                           | -    | -    | 75   | A             |
| $I_{SM}$ | Pulsed source current (body diode)     |                                                           | -    | -    | 240  | A             |
| $V_{SD}$ | Diode forward voltage                  | $I_F = 25\text{ A}; V_{GS} = 0\text{ V}$                  | -    | 0.85 | 1.2  | V             |
|          |                                        | $I_F = 75\text{ A}; V_{GS} = 0\text{ V}$                  | -    | 1.1  | -    | V             |
| $t_{rr}$ | Reverse recovery time                  | $I_F = 20\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$ | -    | 80   | -    | ns            |
| $Q_{rr}$ | Reverse recovery charge                | $V_{GS} = 0\text{ V}; V_R = 30\text{ V}$                  | -    | 0.2  | -    | $\mu\text{C}$ |

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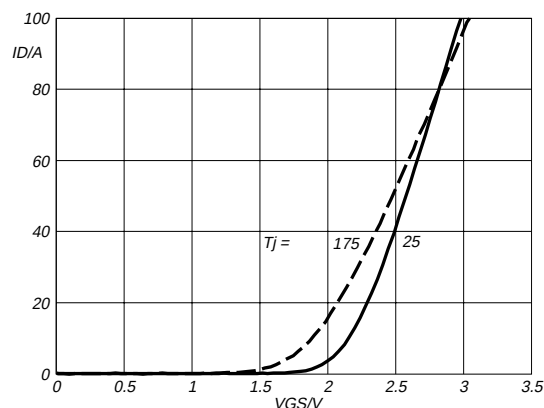
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PSMN005-55P

Fig. 7. Typical transfer characteristics.  
 $I_D = f(V_{GS})$

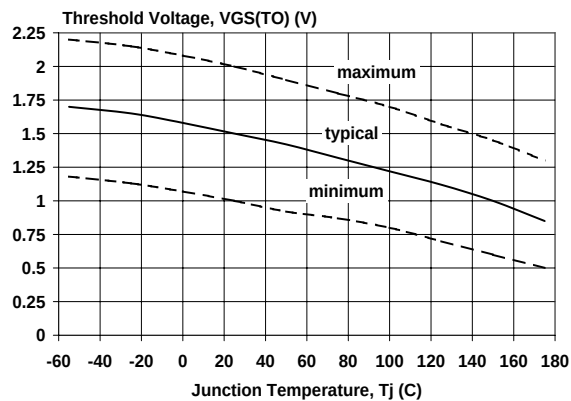


Fig. 10. Gate threshold voltage.  
 $V_{GS(TO)} = f(T_j)$ ; conditions:  $I_D = 1 \text{ mA}$ ;  $V_{DS} = V_{GS}$

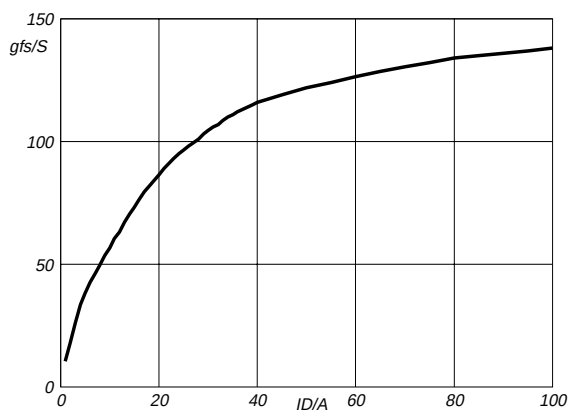


Fig. 8. Typical transconductance,  $T_j = 25 \text{ °C}$ .  
 $g_{fs} = f(I_D)$

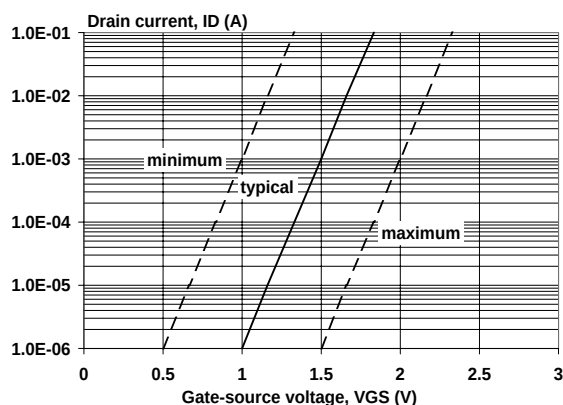


Fig. 11. Sub-threshold drain current.  
 $I_D = f(V_{GS})$ ; conditions:  $T_j = 25 \text{ °C}$ ;  $V_{DS} = V_{GS}$

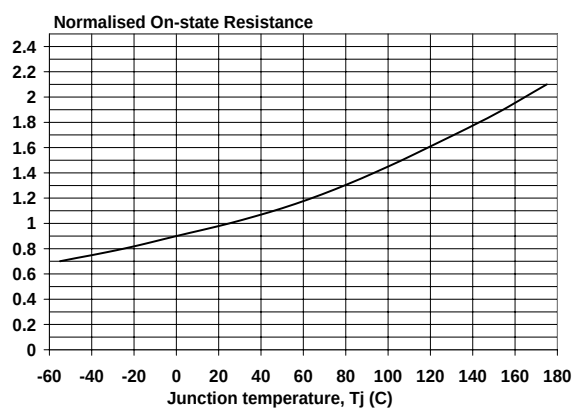


Fig. 9. Normalised drain-source on-state resistance.  
 $R_{DS(ON)}/R_{DS(ON)25 \text{ °C}} = f(T_j)$

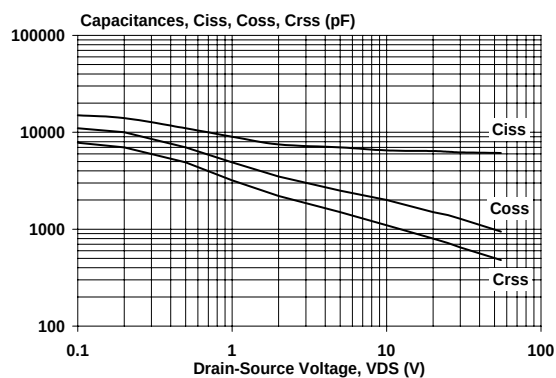


Fig. 12. Typical capacitances,  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$ .  
 $C = f(V_{DS})$ ; conditions:  $V_{GS} = 0 \text{ V}$ ;  $f = 1 \text{ MHz}$

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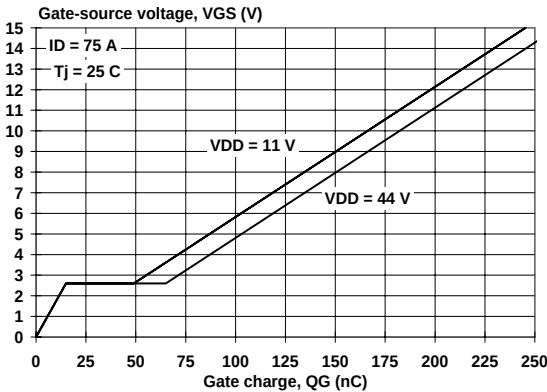


Fig.13. Typical turn-on gate-charge characteristics.  
 $V_{GS} = f(Q_G)$

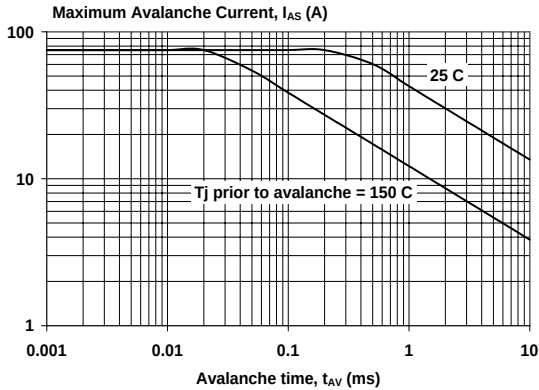


Fig.15. Maximum permissible non-repetitive  
avalanche current ( $I_{AS}$ ) versus avalanche time ( $t_{AV}$ );  
unclamped inductive load

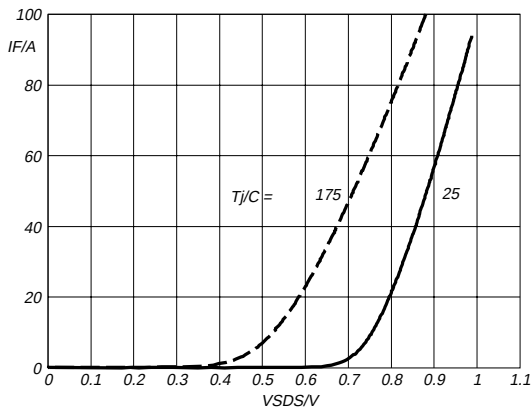


Fig.14. Typical reverse diode current.  
 $I_F = f(V_{SDS})$ ; conditions:  $V_{GS} = 0\text{ V}$ ; parameter  $T_j$



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MECHANICAL DATA

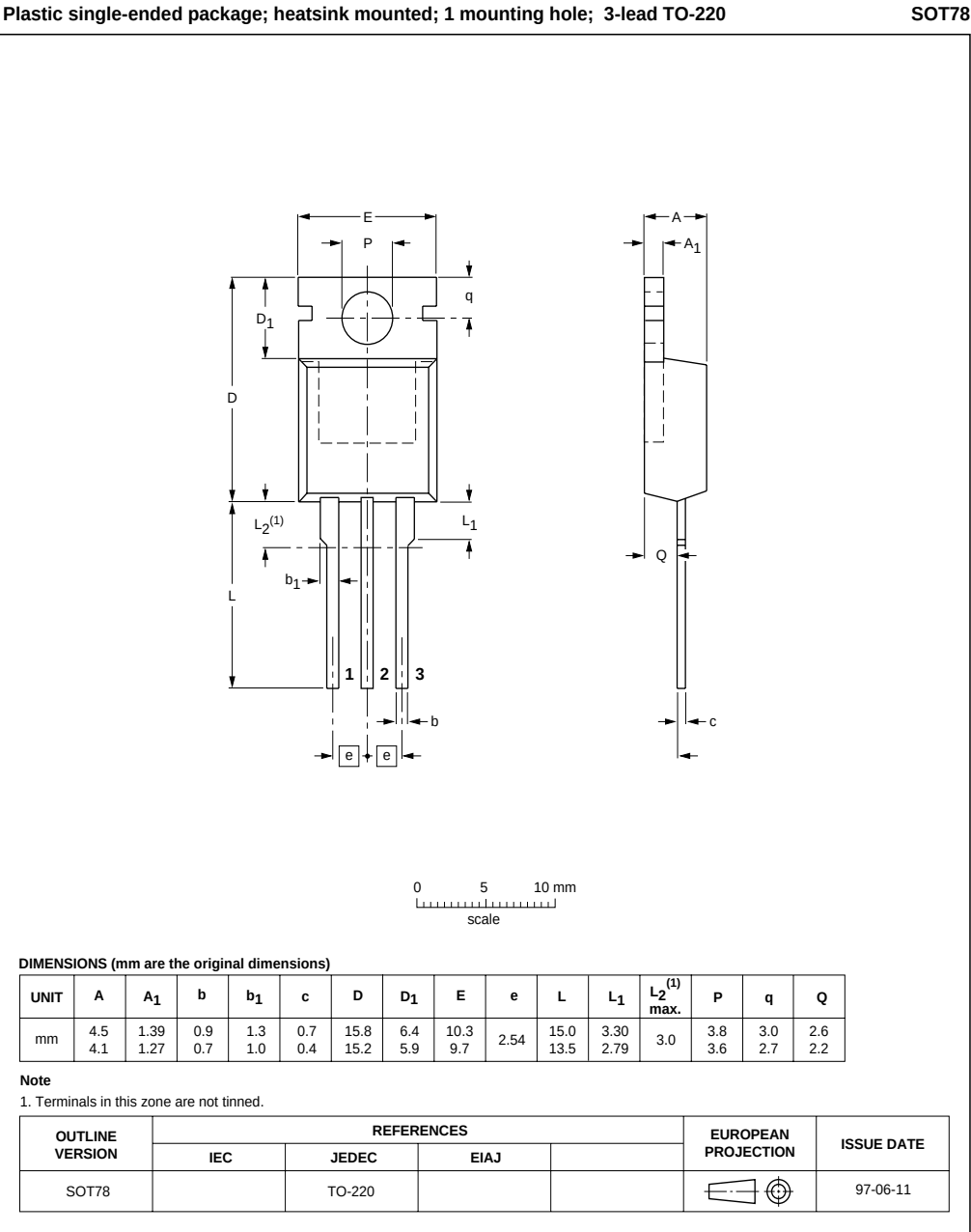


Fig.16. SOT78 (TO220AB); pin 2 connected to mounting base (Net mass:2g)

Notes

- 1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
- 2. Refer to mounting instructions for SOT78 (TO220AB) package.
- 3. Epoxy meets UL94 V0 at 1/8".





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MECHANICAL DATA

Plastic single-ended surface mounted package (Philips version of D<sup>2</sup>-PAK); 3 leads  
(one lead cropped)

SOT404

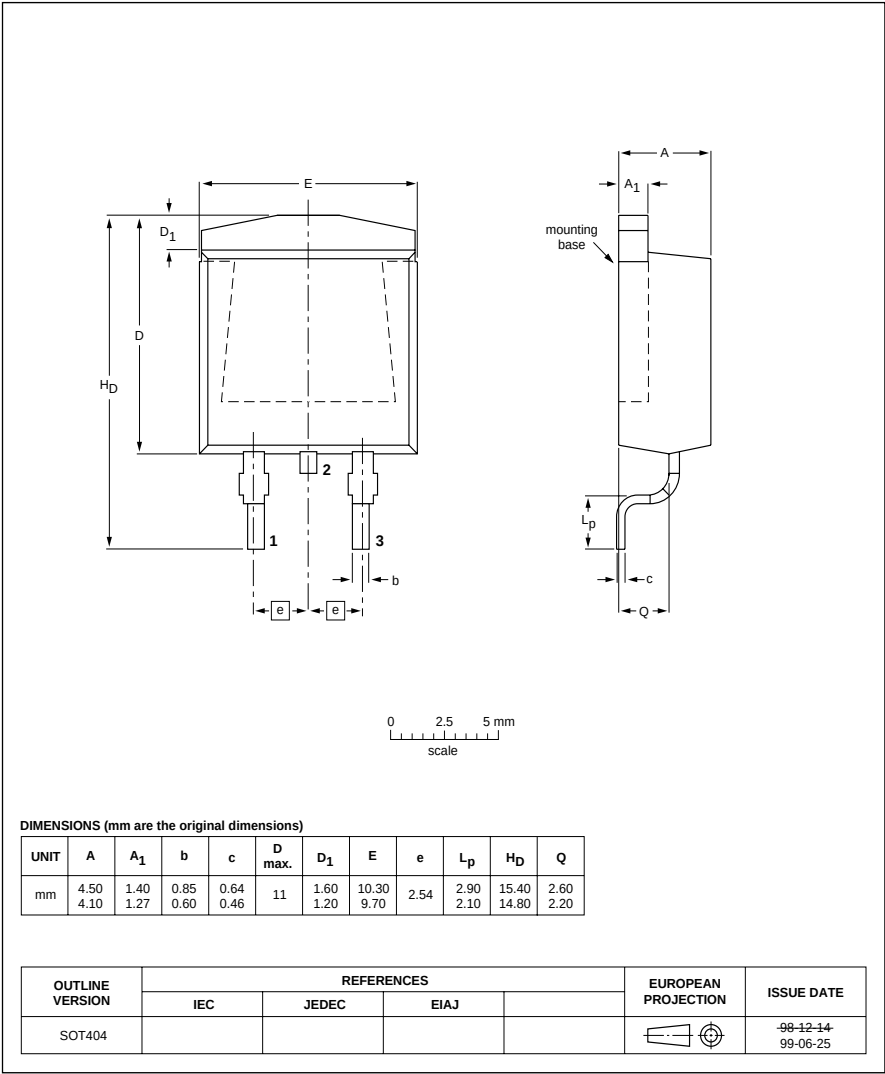


Fig.17. SOT404 surface mounting package. Centre pin connected to mounting base.

Notes

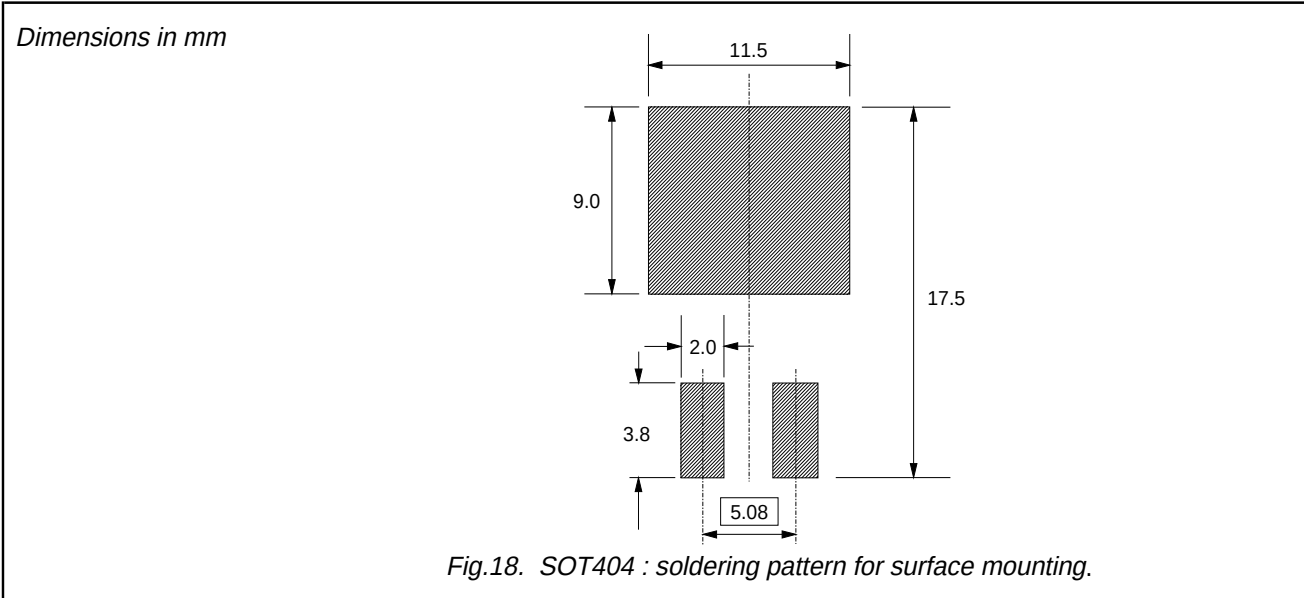
- 1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
- 2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
- 3. Epoxy meets UL94 V0 at 1/8".

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MOUNTING INSTRUCTIONS



DEFINITIONS

| Data sheet status                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                       |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Objective specification                                                                                                                                                                                                                                                                                                                                                                                                                                    | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification                                                                                                                                                                                                                                                                                                                                                                                                                                  | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification                                                                                                                                                                                                                                                                                                                                                                                                                                      | This data sheet contains final product specifications.                                |
| Limiting values                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                                                                       |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |                                                                                       |
| Application information                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                                                                       |
| Where application information is given, it is advisory and does not form part of the specification.                                                                                                                                                                                                                                                                                                                                                        |                                                                                       |
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**SiliconMAX**N-channel logic level TrenchMOS<sup>(TM)</sup> transistorPSMN005-55B;  
PSMN005-55P**NOTES**

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Printed in The Netherlands

603502/300/04/pp12

Date of release: October 1999

Document order number: 9397 750 06976

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