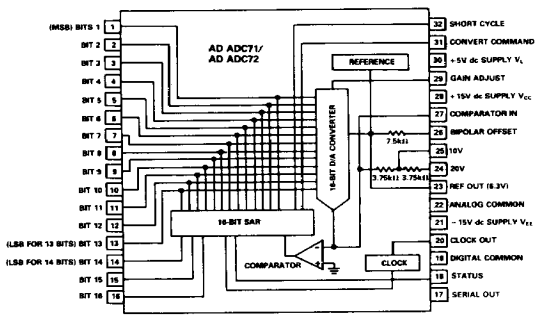
Complete, High Resolution 16-Bit A/D Converters

AD ADC71/AD ADC72

FEATURES

Complete 16-Bit Converter With Reference and Clock
±0.003% Maximum Nonlinearity
No Missing Codes to 14 Bits
Fast Conversion – 35μs (14 Bit)
Short Cycle Capability
Parallel and Serial Logic Outputs
Low Power: 645mW Typical
Industry Standard Pin Out

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD ADC71 and AD ADC72 are high resolution 16-bit hybrid IC analog-to-digital converters including reference, clock, and laser-trimmed thin-film components. The package is a compact 32-pin hermetic ceramic DIP. The thin-film scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V, and 0 to +20V.

Important performance characteristics of the devices are maximum linearity error of ±0.003% of FSR (AD ADC71K, AD ADC72K and B), and maximum conversion time of 50μs. This performance is due to innovative design and the use of proprietary monolithic D/A converter chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The AD ADC71 and AD ADC72 provide data in parallel form with corresponding clock and status outputs. The AD ADC71 also provides data in serial form. All digital inputs and outputs are TTL compatible.

APPLICATIONS

The AD ADC71 and AD ADC72 are excellent for use in applications requiring 14-bit accuracy over extended temperature ranges. Typical applications include medical and analytic instrumentation, precision measurement for industrial robots, automatic test equipment (ATE), multichannel data acquisition systems, servo control systems and anywhere that excellent stability and wide dynamic range in the smallest space is required.

PRODUCT HIGHLIGHTS

1. The AD ADC71 and AD ADC72 provide 16-bit resolution with maximum linearity error less than ±0.003% (±0.006% for J and A grades) at 25°C.
2. Conversion time is 35μs typical to 14 bits with short cycle capability.
3. Two binary codes are available on the AD ADC71 and AD ADC72 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary two's complement (CTC) coding may be obtained by inverting Pin 1 (MSB).
4. The proprietary chips used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.

ORDERING GUIDE

Model	Linearity Error (Max)	Specification Temp Range	Package Option*
AD ADC71JD	±0.006% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC71KD	±0.003% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC72JD	±0.006% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC72KD	±0.003% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC72AD	±0.006% of FSR	−25°C to +85°C	Ceramic (DH-32E)
AD ADC72BD	±0.003% of FSR	−25°C to +85°C	Ceramic (DH-32E)

*DH-32E = Bottom Brazed Ceramic DIP. See outline information see Package Information section.

This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

AD ADC71/AD ADC72—SPECIFICATIONS (typical at T_A = +25°C, V_S = ±15, +5 volts unless otherwise noted)

Model	AD ADC71JD/KD	AD ADC72JD/KD	AD ADC72AD/BD	Units
RESOLUTION	16 (max)	*	*	Bits
ANALOG INPUTS				
Voltage Ranges				
Bipolar	±2.5, ±5, ±10	*	*	Volts
Unipolar	0 to +5, 0 to +10, 0 to +20	*	*	Volts
Impedance (Direct Input)				
0 to +5V, ±2.5V	1.88	*	*	kΩ
0 to +10V, ±5.0V	3.75	*	*	kΩ
0 to +20V, ±10V	7.50	*	*	kΩ
DIGITAL INPUTS[1]				
Convert Command	Positive Pulse 50ns Wide (min) Trailing Edge Initiates Conversion			
Logic Loading	1 (max)	*	*	LSTTL Load
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error	±0.1[2] (±0.2 max)	*	*	%
Offset Error				
Unipolar	±0.05[2] (±0.1 max)	*	*	% of FSR[3]
Bipolar	±0.1[2] (±0.2 max)	*	*	% of FSR
Linearity Error (max)	±0.006 (J)	±0.006 (J)	±0.006 (A)	% of FSR
	±0.003 (K)	±0.003 (K)	±0.003 (B)	% of FSR
Inherent Quantization Error	±1/2	*	*	LSB
Differential Linearity Error	±0.003	*	*	% of FSR
No Missing Codes @ 25°C[4]	To 14 Bits (K Grade)	*	To 14 Bits (B Grade)	Guaranteed
POWER SUPPLY SENSITIVITY				
±15V dc	0.003	*	*	% of FSR/% ΔV_S
+5V dc	0.001	*	*	% of FSR/% ΔV_S
CONVERSION TIME[5] (14 BITS)	35 (50 max)	*	*	µs
WARM-UP TIME	5 (min)	*	*	Minutes
DRIFT				
Gain	±15 (max)	±10 (±20 max)	+7 (±15 max)	ppm/°C
Offset				
Unipolar	±2 (±4 max)	±2 (±4 max)	±2 (±4 max)	ppm of FSR/°C
Bipolar	±10 (max)	±8 (±10 max)	±5 (±10 max)	ppm of FSR/°C
Linearity	±2 (3 max)	±1.5 (2 max)	±1.0 (2 max)	ppm of FSR/°C
Guaranteed No Missing Code				
Temperature Range[4]				
71JD, 72JD, 72AD (13 Bits)	0 to 70	*	*	°C
71KD, 72KD, 72BD (14 Bits)				
DIGITAL OUTPUT[1]				
(All Codes Complementary)				
Parallel and Serial				
Output Codes[6]				
Unipolar	CSB	*	*	
Bipolar	COB, CTC[7]	*	*	
Output Drive	5	*	*	LSTTL Loads
Status	Logic "1" During Conversion			
Status Output Drive	5 (max)	*	*	LSTTL Loads
Internal Clock				
Clock Output Drive	5 (max)	*	*	LSTTL Loads
Frequency	400	*	*	kHz
INTERNAL REFERENCE VOLTAGE	6.3	*	*	V dc
Error	±5 max	*	*	%
Max External Current Drain				
With no Degradation of Specs	±200 max	*	*	µA
Temperature Coefficient	±10 max	*	±5 max	ppm/°C
POWER SUPPLY REQUIREMENTS				
Power Consumption	645 (850 max)	*	*	mW
Rated Voltage, Analog	±15 ±0.5 max	*	*	V dc
Rated Voltage, Digital	+5 ±0.25 max	*	*	V dc
Supply Drain +15V dc	+16	*	*	mA
Supply Drain −15V dc	−21	*	*	mA
Supply Drain +5V dc	+18	*	*	mA
TEMPERATURE RANGE				
Specification	0 to +70	*	−25 to +85	°C
Operating (Derated Specs)	−25 to +85	*	−25 to +125	°C
Storage	−55 to +125	*	*	°C

NOTES
[1] Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V max. Logic "1" = 2.4V min.
[2] Adjustable to zero.
[3] Full Scale Range.
[4] For definition of "No Missing Codes," refer to Theory of Operation (full data sheet.)
[5] Conversion time may be shortened with "Short Cycle" set for lower resolution.
[6] CSB – Complementary Straight Binary. COB – Complementary Offset Binary. CTC – Complementary Twos Complement.
[7] CTC coding obtained by inverting MSB (Pin 1).
*Specifications same as AD ADC71JD, KD.
Specifications subject to change without notice.