



CYPRESS

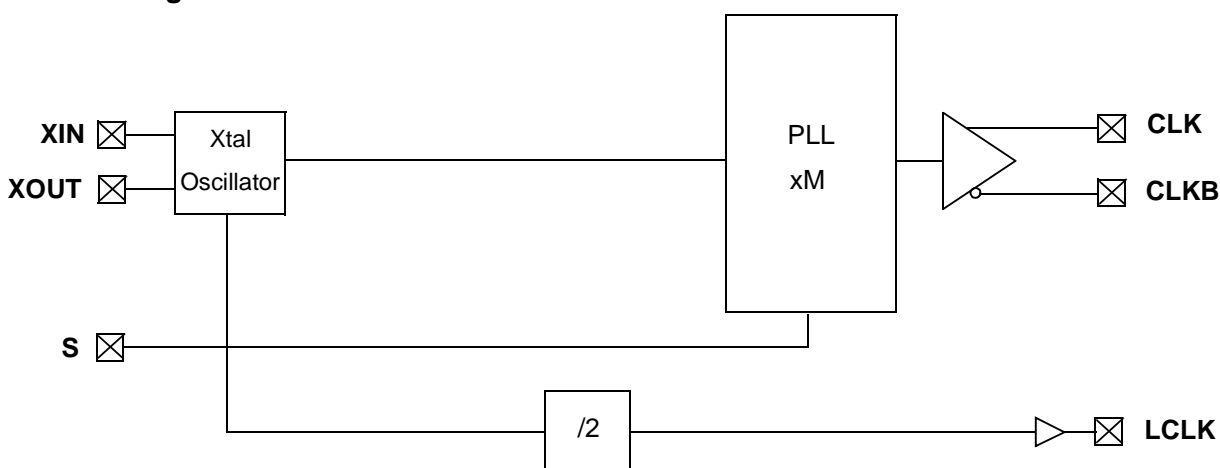
PRELIMINARY

CY2212

Direct Rambus™ Clock Generator (Lite)

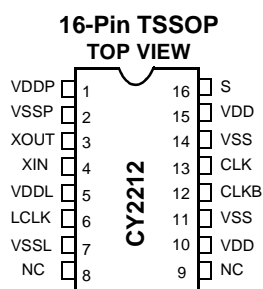
Features	Benefits
• Direct Rambus™ Clock Support	One pair of differential output drivers
• High Speed Clock Support	400 MHz maximum output frequency, 300 MHz minimum
• Input Select Option	PLL multiplier select
• Crystal Oscillator Divider Output	LCLK = XTAL/2, not driven by PLL
• Output edge-rate control	Minimize EMI
• 16-pin TSSOP	Space-saving, low-cost package

Logic Block Diagram



Xtal Value = 18.75 MHz

Pin Configuration



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Pin Summary

Name	Pin	Description
VDDP	1	3.3V Power Supply for PLL
VSSP	2	Ground for PLL
XOUT	3	Reference Crystal Feedback
XIN	4	Reference Crystal Input
VDDL	5	1.8V Power Supply for LCLK
LCLK	6	LVC MOS Output, x1/2 Crystal Frequency
VSSL	7	Ground for LCLK
NC	8	No Connect (Reserved for Test Mode)
NC	9	No Connect (Reserved for Test Mode)
VDD	10	3.3V Power Supply
VSS	11	Ground
CLKB	12	Output Clock (complement), Connect to Rambus Channel
CLK	13	Output Clock, Connect to Rambus Channel
VSS	14	Ground
VDD	15	3.3V Power Supply
S	16	PLL Multiplier Select Input, Pull-Up Resistor Internal

Select Function Table

S	M (PLL Multiplier)	CLK,CLKB	LCLK
0	16	300 MHz	9.375 MHz
1	64/3	400 MHz	9.375 MHz

Absolute Maximums

The following table reflects stress ratings only, and functional operation at the maximums are not guaranteed.

Symbol	Parameter	Min.	Max.	Unit
$V_{DD,ABS}$	Max voltage on VDD, VDDP, or VDDL with respect to ground	-0.5	4.0	V
$V_{I,ABS}$	Max voltage on any pin with respect to ground	-0.5	VDD+0.5	V
$V_{IL,ABS}$	Max voltage on LCLK with respect to ground	-0.5	VDDL+0.5	V

Crystal Requirements

These are the requirements for the recommended crystal to be used with the CY2212 DRCG Lite clock source. The crystal type is TBD. The mode is fundamental. Internal capacitors will

not be implemented in the crystal oscillator circuit. External capacitors will be needed.

Symbol	Parameter	Min.	Max.	Unit
X_F	Frequency	14.0625	18.75	MHz
X_{FTOL}	Frequency Tolerance ^[1]	-15	15	ppm
X_{EQRES}	Equivalent Resistance ^[2]		100	Ω
X_{TEMP}	Temperature Drift ^[3]		10	ppm
X_{DRIVE}	Drive Level	0.01	1500	μW
X_{MI}	Motional Inductance	20.7	25.3	mH
X_{IR}	Insulation Resistance	500		M Ω
X_{SAR}	Spurious Attenuation Ratio ^[4]	3		dB
X_{OS}	Overtone Spurious	8		dB

Notes:

1. At 25°C \pm 3°C.
2. CL = 10 pF.
3. -10°C to 75°C.
4. At $X_F \pm 500$ kHz.

DC Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply voltage	3.04	3.56	V
V_{DDL}	LCLK Supply voltage	1.7	2.1	V
T_A	Ambient operating temperature	0	70	°C
V_{IL}	Input signal low voltage at pin S		0.35	VDD
V_{IH}	Input signal high voltage at pin S	0.65		VDD
R_{PUP}	Internal pull-up resistance	10	100	k Ω

AC Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
$f_{XTAL,IN}$	Input frequency at crystal input ^[5]	14.0625	18.75	MHz
$C_{IN,CMOS}$	Input capacitance at S pin ^[6]		10	pF

DC Device Characteristics

Symbol	Parameter	Min	Max	Unit
V_{CM}	Differential output common-mode voltage	1.35	1.75	V
V_X	Differential output crossing-point voltage	1.25	1.85	V
V_{COS}	Output Voltage swing (p-p single-ended) ^[7]	0.4	0.7	V
V_{COH}	Output high voltage		2.1	V
V_{COL}	Output low voltage	1.0		V
r_{OUT}	Output dynamic resistance (at pins) ^[8]	12	50	Ω
V_{LOH}	LCLK Output high voltage at $I_{OH} = -10$ mA	VDDL-0.45V	VDDL	V
V_{LOL}	LCLK Output Low Voltage at $I_{OL} = 10$ mA	0	0.45	V

State Transition Characteristics

Specifies the maximum settling time of the CLK, CLKB, and LCLK outputs from device power-up. For VDD, VDDP, and VDDL any sequences are allowed to power-up and power-down the CY2212 DRCG-Lite.

From	To	Transition Latency	Description
VDD/VDDL/VDDP On	CLK/CLKB/LCLK Normal	3 ms	Time from VDD/VDDL/VDDP is applied and settled to CLK/CLKB/LCLK outputs settled

Notes:

5. Nominal condition with 18.75 MHz crystal.
6. Capacitance measured at Freq = 1 MHz, DC Bias = 0.9 V, and VAC < 100 mV.
7. $V_{COS} = V_{OH} - V_{OL}$.
8. $r_{OUT} = \Delta V_O / \Delta I_O$. This is defined at the output pins, not at the measurement point of Figure 3.

AC Device Characteristics

Symbol	Parameter	Min	Max	Unit
t_{CYCLE}	Clock cycle time	2.5	3.33	ns
t_{J}	Jitter over 1–6 clock cycles at 400 MHz ^[9]		100	ps
	Jitter over 1–6 clock cycles at 300 MHz ^[9]		140	ps
t_{JL}	Long-term jitter at 400 MHz		300	ps
	Long-term jitter at 300 MHz		400	ps
DC	Long-term average output duty cycle	45%	55%	t_{CYCLE}
$t_{\text{DC,ERR}}$	Cycle-cycle duty cycle error at 400 MHz		50	ps
	Cycle-cycle duty cycle error at 300 MHz		70	ps
$t_{\text{CR}}, t_{\text{CF}}$	Output rise and fall times (measured at 20%–80% of output voltage)	250	500	ps
$t_{\text{CR, CF}}$	Difference between output rise and fall times on the same pin of a single device (20%–80%)		100	ps
BW_{LOOP}	PLL Loop Bandwidth	50 kHz (–3 dB)	8 MHz (–20 dB)	
$t_{\text{CYCLE,L}}$	LCLK Clock cycle time	106.6	142.2	ns
$t_{\text{LR}}, t_{\text{LF}}$	LCLK output rise and fall time		1	ns
$t_{\text{JC,L}}$	LCLK cycle jitter ^[10]	–0.8	0.8	ns
$t_{\text{J10,L}}$	LCLK 10-cycle jitter ^[10,11]	$-1.1 * t_{\text{JC,L}}$	$1.1 * t_{\text{JC,L}}$	ns
DC_{L}	LCLK output duty cycle	40%	60%	$t_{\text{CYCLE,L}}$

Notes:

9. Output short-term jitter specification is peak-peak and defined in Figure 10.
10. LCLK cycle jitter and 10-cycle jitter are defined as the difference between the measured period and the nominal period as defined on page 10.
11. LCLK 10-cycle jitter specification is based on the measured value of LCLK cycle jitter as defined on page 10.

Functional Specifications

This section gives the detailed functional specifications of the device physical layer. These specifications refer to the logical and physical interfaces.

Crystal Input

The CY2212 receives its reference from an external crystal. Pin XIN is the reference crystal input, and pin XOUT is the reference crystal feedback. The parameters for the crystal are given on page 3 of this data sheet. The oscillator circuit does not implement internal capacitors. External capacitors with value TBD will be needed.

Select Input

There is only one select input, pin S. This pin selects the frequency multiplier in the PLL, and is a standard LVCMOS input. The S pin has an internal pull-up resistor. The multiplier selection is given on page 2 of this data sheet.

LCLK Output Driver

In addition to the Rambus clock driver outputs, there is another clock output driver. The LCLK driver is a standard LVCMOS output driver. Figure 1 below shows the LCLK output driver load circuit.

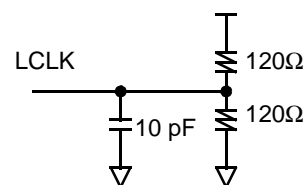


Figure 1. LCLK Test Load Circuit

RSL Clock Output Driver

Figure 2 shows the clock driver equivalent circuit.

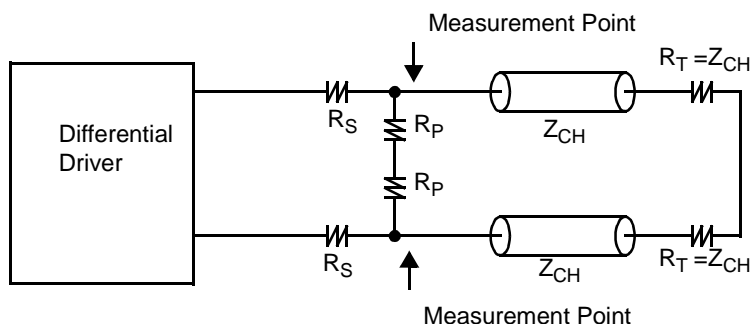


Figure 2. Equivalent Circuit

The differential driver has a low output impedance in the range of about 20 ohms. The driver also produces a specified voltage swing on the channel. The nominal value of the channel impedance, Z_{CH} , is 28 ohms. Series resistor R_S and parallel resistor R_P are used to set the voltage swing on the channel. The driver output characteristics are defined together with the external components, and the output clock is specified at the measurement point indicated in *Figure 2*. The complete set of external components for the output driver, including edge-rate filter capacitors required for system operation, are shown in *Figure 3*. The values for the external components are given in *Table 1*.

The output clocks drive transmission lines, potentially long lines. Since circuit board traces will act as lossy, imperfectly-terminated transmission lines with some discontinuities, there will be reflections generated which will travel back to the DRCG-Lite output driver. If the output impedance does not match Z_{CH} , secondary reflections will be generated that will add to position-dependent timing uncertainty. Therefore, the CY2212 not only provides proper output voltage swings, but also provides a well-matched output impedance. The driver impedance, R_{OUT} , is in series with R_S , and the combination is in parallel with R_P .

The clock driver is specified as a black-box at the packaged pins. The output characteristics are measured after the series resistance, R_S . The outputs are terminated differentially, with no applied termination voltage.

Figure 3 below shows the clock driver implemented as a push-pull driver. When stimulating the output driver, the transmis-

sion lines shown in *Figure 3* can be replaced by a direct connection to the termination resistors, R_T . The values for the external components are given in *Table 1*.

As mentioned previously, the clock driver's output impedance matches the channel impedance. To accomplish this, each of the output driver devices are sized to have an R_{OUT} of about 20 ohms when fully turned on. R_{OUT} is the dynamic output resistance, and is defined in the DC Device Characteristics Table on page 4 of this data sheet. Since R_{OUT} is in series with R_S , and that combination is in parallel with R_P , the effective output impedance is given by:

$$R_P(R_S + R_{OUT}) / (R_P + R_S + R_{OUT})$$

This calculation results in an effective output impedance of about 27 ohms for the values listed in *Table 1*. Since the total impedance is dominated by the external resistors, a large possible range of R_{OUT} is allowed. When the output is transitioning, the impedance of the CMOS devices increases dramatically. The purpose of R_P is to limit the maximum output impedance during output transitions.

In order to control signal attenuation and EMI, clock signal rise/fall times must be tightly controlled. Therefore, external filter capacitors C_F are used to control the output slew rate. In addition, the capacitor C_{MID} is used to provide AC ground at the mid-point of the R_P resistors.

Table 1 gives the nominal values of the external components and their maximum acceptable tolerance, assuming $Z_{CH} = 28$ ohms.

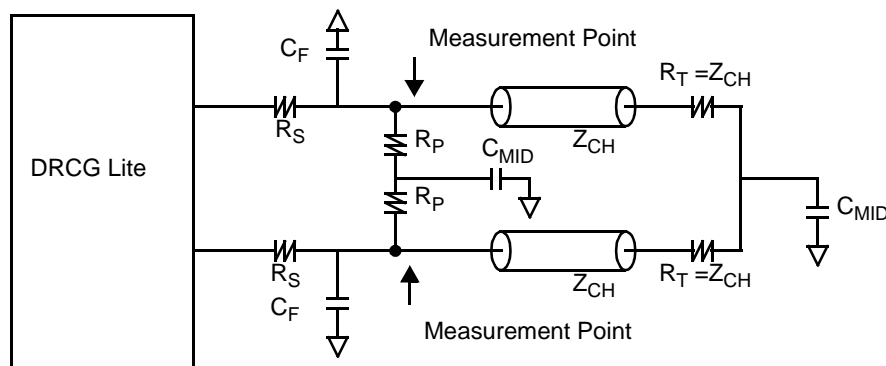
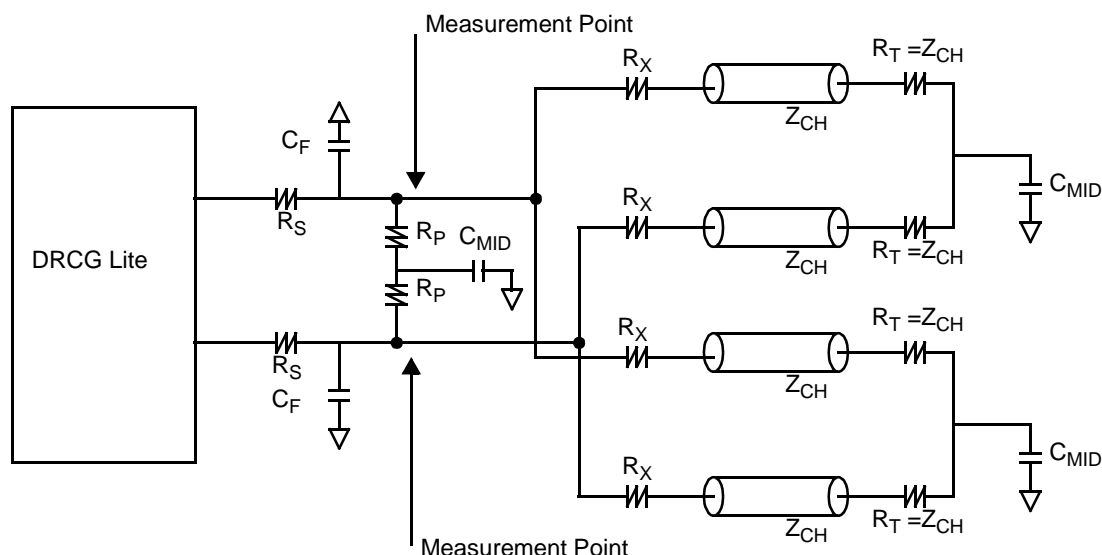


Figure 3. Output Driver

Table 1. External Component Values

Symbol	Parameter	Value	Tolerance	Unit
R_S	Series Resistor	68	$\pm 5\%$	ohm
R_P	Parallel Resistor	39	$\pm 5\%$	ohm
C_F	Edge-Rate Filter Capacitor	15	$\pm 10\%$	pF
C_{MID}	AC Ground Capacitor	0.01	$\pm 20\%$	μF


Figure 4. Output Driving Two Channels

Dual-Channel Output Driver

Figure 4 shows the clock driver driving two high-impedance channels. The purpose of the series resistors R_X is to de-couple the two-channels, and prevent noise from one channel from coupling onto the second channel. With $Z_{CH} = 40$ ohms and the series resistor set to $R_X = 16$ ohms, the channel becomes an effective 56 ohm channel. The two channels in parallel can be treated as a single 28 ohm channel, and all of the external component values listed in Table 1 can be used.

Signal Waveforms

A physical signal which appears at the pins of the device is deemed valid or invalid depending on its voltage and timing relations with other signals. This section defines the voltage and timing waveforms for the input and output pins of the CY2212. The Device Characteristics tables list the specifications for the device parameters that are defined here.

Input and Output voltage waveforms are defined as shown in Figure 5. Both rise and fall times are defined between the 20% and 80% points of the voltage swing, with the swing defined as $V_H - V_L$. For example, the output voltage swing $V_{COS} = V_{OH} - V_{OL}$.

The device parameters defined according to Figure 5 are:

Table 2. Definition of Device Parameters

Parameter	Definition
V_{OH}, V_{OL}	Clock output high and low voltages
V_{COS}	Clock output swing $V_{COS} = V_{OH} - V_{OL}$
V_{CM}	Common-mode voltage $V_{CM} = (V_{OH} + V_{OL})/2$
V_{IH}, V_{IL}	Vdd LVC MOS input high and low voltages
t_{CR}, t_{CF}	Clock output rise and fall times
t_{CR}, C_F	Clock output rise/fall time delta $t_{CR,CF} = t_{CR} - t_{CF}$

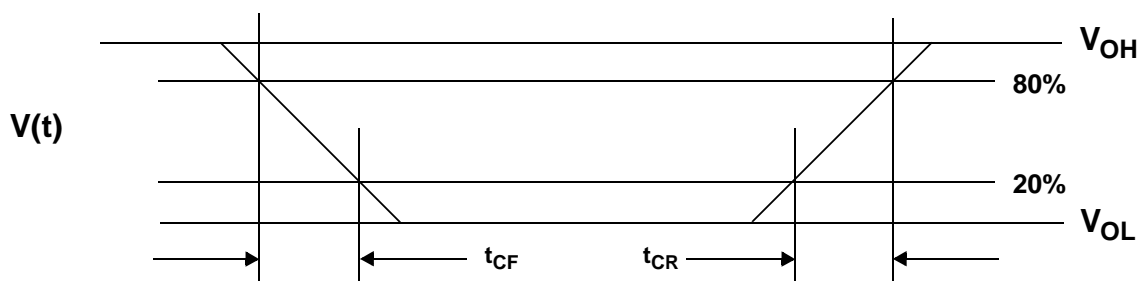


Figure 5. Voltage Waveforms

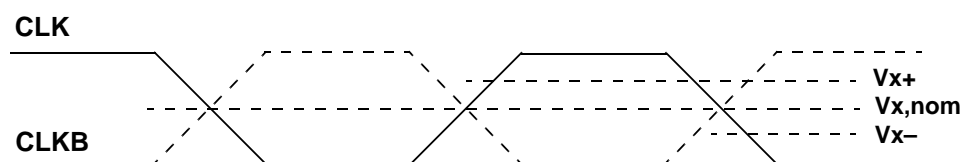


Figure 6. Crossing-point Voltage

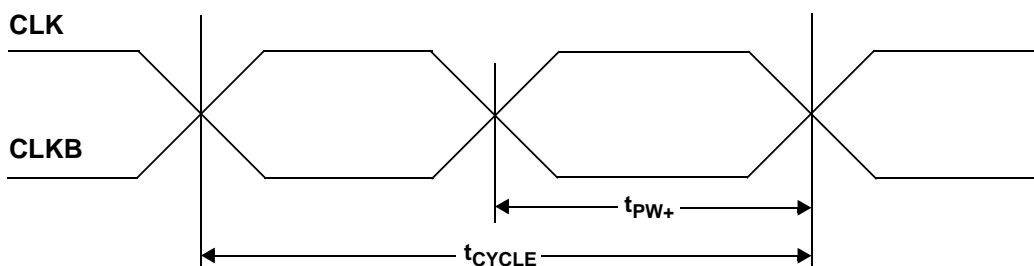
Figure 6 shows the definition of output crossing point. The nominal crossing point between the complementary outputs is defined to be at the 50% point of the DC voltage levels. There are two crossing points defined, V_{x+} at the rising edge of CLK and V_{x-} at the falling edge of CLK. For some clock waveforms, both V_{x+} and V_{x-} might be below $V_{x, \text{nom}}$ (for example, if t_{CR} is larger than t_{CF}). V_x is defined as the differential output crossing point voltage.

Figure 7 shows the definition of long-term duty cycle, which is simply the waveform high-time divided by the cycle time (defined at the crossing point). Long-term duty cycle is the average over many (>10,000) cycles. Short-term duty cycle is de-

fined in the next section. DC is defined as the output clock long-term duty cycle.

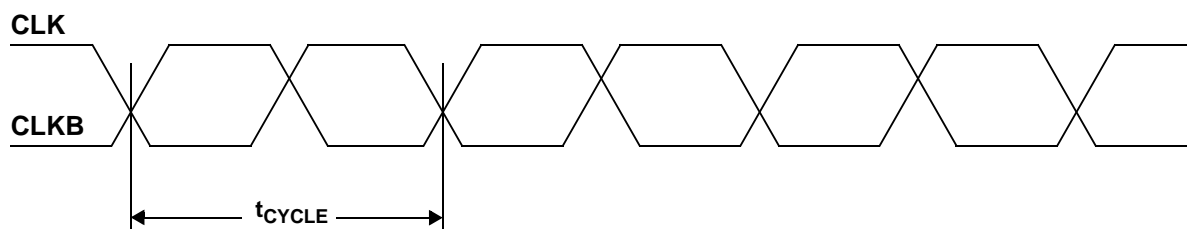
Jitter

This section defines the specifications that relate to timing uncertainty (or jitter) of the input and output waveforms. Figure 8 shows the definition of long-term jitter with respect to the falling edge of the CLK signal. Long-term jitter is the difference between the minimum and maximum cycle times. Equal requirements apply for rising edges of the CLK signal. t_{JL} is defined as the output long-term jitter.



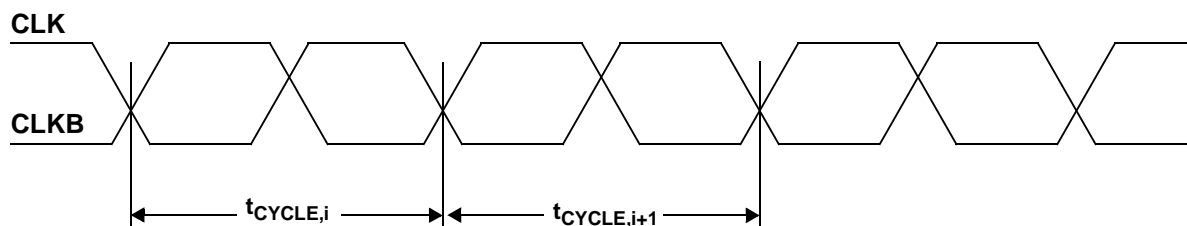
$$DC = t_{PW+} / t_{CYCLE}$$

Figure 7. Duty Cycle



$$t_{JL} = t_{CYCLE,max} - t_{CYCLE,min} \text{ over } 10000 \text{ cycles}$$

Figure 8. Long-term Jitter



$$t_J = t_{CYCLE,i} - t_{CYCLE,i+1} \text{ over } 10000 \text{ consecutive cycles}$$

Figure 9. Cycle-to-cycle Jitter

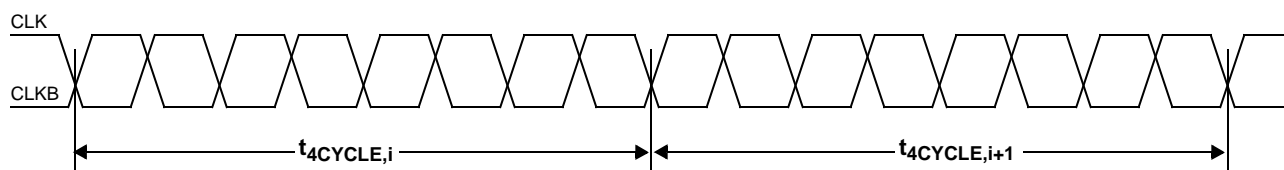
Figure 9 shows the definition of cycle-to-cycle jitter with respect to the falling edge of the CLK signal. Cycle-to-cycle jitter is the difference between cycle times of adjacent cycles. Equal requirements apply for rising edges of the CLK signal. t_J is defined as the clock output cycle-to-cycle jitter.

Figure 10 shows the definition of 4-cycle short-term jitter. Short-term jitter is defined with respect to the falling edge of the CLK. 4-cycle short-term jitter is the difference between the cumulative cycle times of adjacent 4 cycles. Equal requirements apply for rising edges of the CLK signal. Equal requirements also apply for 2-cycle short-term jitter and 3-cycle short-term jitter, and for 5-cycle short-term jitter and 6-cycle short-term jitter. t_J is defined as the clock output short-term jitter over 2, 3, 4, 5, or 6 cycles.

The purpose of this definition of short-term jitter is to define errors in the measured time (for example, $t_{4CYCLE,i}$) vs. the expected time. The purpose for measuring the adjacent time

$t_{4CYCLE,i+1}$ is only to help determine the expected time for $t_{4CYCLE,i}$. Alternate methods of determining t_J are possible, including comparing the measured time to an expected time based on a local cycle time, $t_{CYCLE,LOCAL}$. This local cycle time could be determined by taking the rolling average of a group of cycles (5–10 cycles) proceeding the measured cycles. However, it is important to differentiate this rolling average from the average cycle time, $t_{CYCLE,AVG}$, which is the average cycle time over the 10,000 cycles. Using a long-term average instead of a rolling average would define t_J as a long-term jitter instead of a short-term jitter, and would normally give overly pessimistic results.

Figure 11 shows the definition of cycle-to-cycle duty cycle error. Cycle-to-cycle duty cycle error is defined as the difference between high-times of adjacent cycles. Equal requirements apply to the low-times. $t_{DC,ERR}$ is defined as the clock output cycle-to-cycle duty cycle error.



$$t_J = t_{4CYCLE,i} - t_{4CYCLE,i+1} \text{ over } 10000 \text{ consecutive cycles}$$

Figure 10. Short-term Jitter

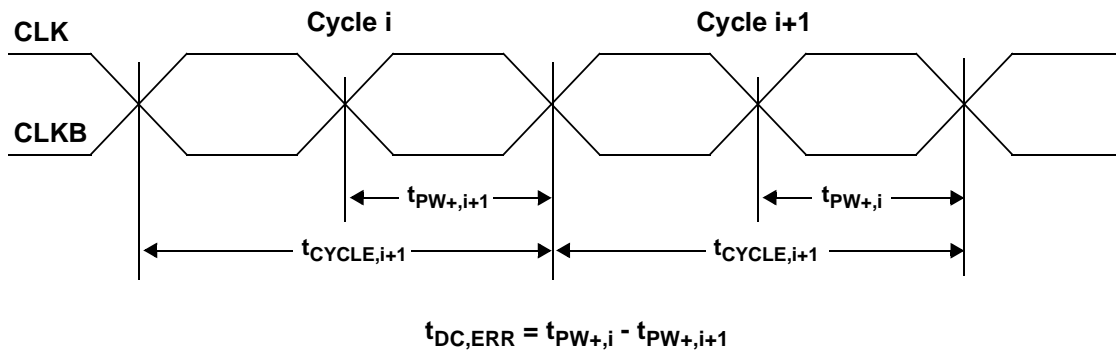


Figure 11. Cycle-to-cycle Duty Cycle Error

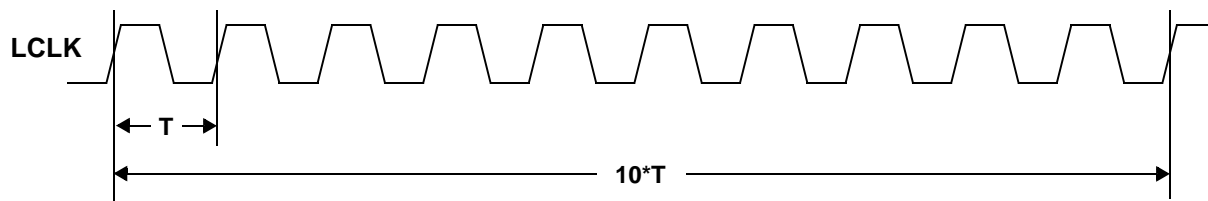


Figure 12. LCLK Jitter

Figure 12 shows the definition of LCLK cycle jitter and LCLK 10-cycle jitter. These parameters apply to the LCLK output, and not to the Rambus channel clock outputs.

LCLK cycle jitter is the variation in the clock period, T , over a continuous set of clock cycles. The difference between the maximum period and the nominal period in the set of clock cycles measured would be compared to the max spec listed in the AC Device Characteristics Table on page 5. LCLK cycle jitter is measured between rising edges at 50% of the output voltage, and is measured continuously over 30,000 cycles.

LCLK 10-cycle jitter is the variation in the time of 10 clock cycles, $10 \cdot T$, where T is the clock period. The difference between the maximum 10-cycle period and the nominal 10-cycle period in the set of clock cycles measured would be compared to the max spec listed in the AC Device Characteristics Table on page 5. Note that the specification for LCLK 10-cycle jitter is defined based on the measured value of LCLK cycle jitter. LCLK 10-cycle jitter is measured between the first rising edge and the 10th rising edge at 50% of the output voltage, and is measured over 30,000 continuous cycles. $t_{JC,L}$ is defined as

the LCLK output cycle jitter, and $t_{J10,L}$ is defined as the LCLK output jitter over 10 cycles.

Measurement

The short-term jitter specification (over one to six cycles) for the clock source is given as t_j , as previously shown. Jitter should be measured using a jitter measurement system that has the flexibility of measuring cycle-to-cycle jitter as a function of cycle count. It is important that the short-term jitter be measured over consecutive cycles in order to prevent long-term drift from causing overly-pessimistic results. When measured over 10,000 consecutive cycles, the short-term jitter measurements generate large amounts of data which can be viewed in a histogram. Figure 13 shows an example histogram of data from a 4-cycle short-term jitter measurement, with results that are within spec lines for t_j . Note that the jitter is specified as peak-to-peak, so the center of the histogram need not be exactly zero.

Further details of jitter measurement methodologies are given in the Rambus DRCG-Lite Specification Appendix A published by Rambus, Inc.

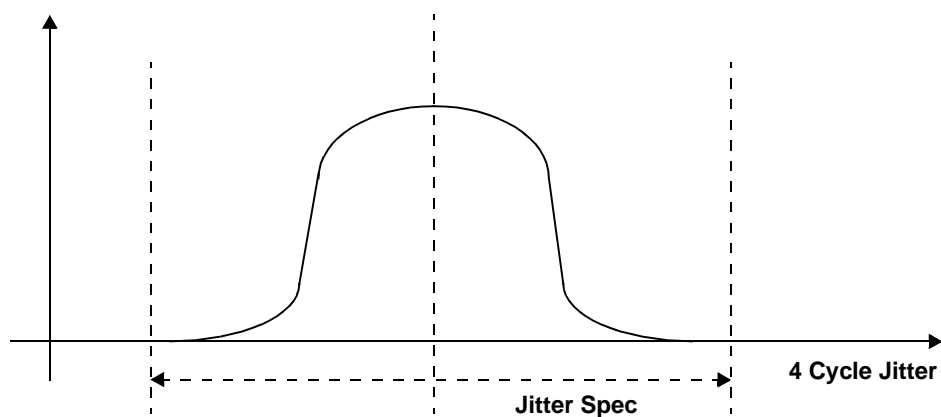


Figure 13. Example Jitter Measurement Histogram

The actual CY2212 Jitter Histogram taken from the characterization board will appear here when the part is available.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2212ZC-1	Z16	16-Lead TSSOP	Commercial

Document #: 38-00

Package Diagram

16-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16

