

STRUCTURE	Silicon Monolithic Integrated Circuit
TYPE	High-Side Current-Sense Amplifier
PRODUCT SERIES	BD3181FVM
FEATURES	<ul style="list-style-type: none"> •Input bias current < 100 μ A Max. •High accurate output voltage gain (GV:50 \pm2%)

○ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limit	Unit
Supply Voltage 1	VCC	30	V
Supply Voltage 2	VPOS,VNEG	30	V
Supply Voltage 3	VBIAS	7	V
Standby Voltage	VST	30	V
Power Dissipation 1	Pd1	587.5 ^{*1}	mW
Power Dissipation 2	Pd2	387.5 ^{*2}	mW
Operating Temperature Range	Topr	-30~+85	°C
Storage Temperature Range	Tstg	-55~+125	°C
Maximum Junction Temperature	Tjmax	+150	°C

*1 Reduced by 4.7mW for each increase in Ta of 1°C over 25°C (When mounted on a board 70mm × 70mm × 1.6mm Glass-epoxyPCB)

*2 Reduced by 3.1mW for each increase in Ta of 1°C over 25°C (With no heat sink)

○ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT			UNIT
		MIN	TYP	MAX	
Supply Voltage	VCC	3	5	28	V
Common Mode Input Voltage Range	Vicm	1.8	-	28	V
Differential Input Voltage Range	Vidf	-200	-	200	mV
BIAS Voltage Range	Vbias	1.2	-	Vcc-1.2	V
OUT pin Output Current	Iout	-	-	10	mA

Status of this document

The Japanese version of this document is the official specification.

This translated version is intended only as a reference, to aid in understanding the official version.

If there are any differences between the original and translated versions of this document, the official Japanese language version takes priority.

OELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25°C ,VCC=V_{ST}=5V,V_{BIAS}=2.5V,V_{POS}-V_{NEG}=ΔVin)

PARAMETER	SYMBOL	LIMIT			UNIT	PARAMETER
		MIN	TYP	MAX		
【General Specifications】						
Supply Voltage	VCC	3	5	30	V	
Quiescent Current	ISC	-	0.0	1.0	μA	VST=0V
Input bias Current	Icc	-	60	100	μA	ΔVin=0V
Voltage Gain (Gv=50)	Gv	49.0	50.0	51.0	mV/mV	Ta=-30~85℃ *3
【NEG, POS】						
Input Offset Voltage	Voff	-0.5	0.0	0.5	mV	ΔVin=0V
Common Mode Input Voltage Range	Vicm	1.8	-	30.0	V	
Differential Input Voltage Range	Vidf	-200	-	200	mV	
Input Bias Current	Ib	-	1.2	1.6	μA	ΔVin=0V POS, NEG=2.5V
Input Impedance	Zi	100	-	-	kΩ	
【BIAS】						
BIAS Voltage Range	VBIAS	1.2	-	VCC-12	V	
BIAS Sink Current	IBIAS	-	0.0	0.1	uA	
【ST】						
ST Sink Current	IST	-	1.5	10.0	uA	
ST Threshold Voltage	VST	0.3	1.0	2.7	V	
【OUT】						
Output Voltage H	VOUTH	VCC-0.1	VCC	-	V	
Output Voltage L	VOU TL	-	0.0	0.1	V	VCC=3V, VBIAS =1.2V
Output Source Current	Isrc	0.5	1.0	-	mA	VOUT=VCC-0.1V
Output Sink Current	Isink	-	-1.0	-0.5	mA	VOUT=0.1V

©This product is not designed for protection against radioactive rays.

*3 Design Guarantee

The drawing shows the MSOP8 package with the following dimensions and features:

- Top View:**
 - Overall width: 2.9 ± 0.1 mm
 - Overall height: 4.0 ± 0.2 mm
 - Pin 1 location: 2.8 ± 0.1 mm from the left edge, 0.475 mm from the bottom edge.
 - Pin 8 location: 0.475 mm from the left edge, $0.145^{+0.05}_{-0.03}$ mm from the bottom edge.
 - Pin 5 location: $0.145^{+0.05}_{-0.03}$ mm from the right edge, 0.6 ± 0.2 mm from the bottom edge.
 - Pin 4 location: $0.145^{+0.05}_{-0.03}$ mm from the right edge, 0.29 ± 0.15 mm from the bottom edge.
 - Pin 3 location: $0.145^{+0.05}_{-0.03}$ mm from the right edge, 0.29 ± 0.15 mm from the bottom edge.
 - Pin 2 location: $0.145^{+0.05}_{-0.03}$ mm from the right edge, 0.29 ± 0.15 mm from the bottom edge.
 - Pin 7 location: $0.145^{+0.05}_{-0.03}$ mm from the right edge, 0.29 ± 0.15 mm from the bottom edge.
 - Pin 6 location: $0.145^{+0.05}_{-0.03}$ mm from the right edge, 0.29 ± 0.15 mm from the bottom edge.
 - Pin 1 Mark: A circle with the number 1 inside, located near pin 1.
 - Lot No.: A circle with the text "Lot No." inside, located near pin 1.
- Side View:**
 - Maximum height: 0.9 Max. mm
 - Pin height: 0.75 ± 0.05 mm
 - Pin thickness: 0.08 ± 0.05 mm
 - Pin pitch: $0.22^{+0.05}_{-0.04}$ mm
 - Pin width: 0.08 (M) mm
- Detail View:**
 - Pin width: 0.65 mm
 - Pin thickness: 0.08 mm
 - Pin shape: S

(UNIT:mm)
MSOP8

Pin number	Pin name
1	ST
2	NEG
3	POS
4	GND
5	BIAS
6	OUT
7	VCC
8	VCC

ONOTES FOR USE

- (1) Absolute maximum range
Although the quality of this product is rigorously controlled, and circuit operation is guaranteed within the operation ambient temperature range, the device may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because the failure mode (such as short mode or open mode) cannot be identified in this instance, it is important to take physical safety measures such as fusing if a specific mode in excess of absolute rating limits is considered for implementation.
- (2) Ground potential
Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode, including transient conditions.
- (3) Thermal Design
Provide sufficient margin in the thermal design to account for the allowable power dissipation (P_d) expected in actual use.
- (4) Using in the strong electromagnetic field
Use in strong electromagnetic fields may cause malfunctions.
- (5) ASO
Be sure that the output transistor for this IC does not exceed the absolute maximum ratings or ASO value.
- (6) GND pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.
- (7) When designing the external circuit, provide sufficient margins in the choice of external components by taking worst case of the IC characteristics and external component's characteristics into consideration, including not only during steady state operation, but also during transient operation.
- (8) It is recommended that bypass capacitor be added between VCC and GND as close to each pin as possible.
- (9) Do not connect VCC, GND, and each output with reverse polarity. Please add a protection diode when a large inductance component is connected to the output terminal.

(Example)

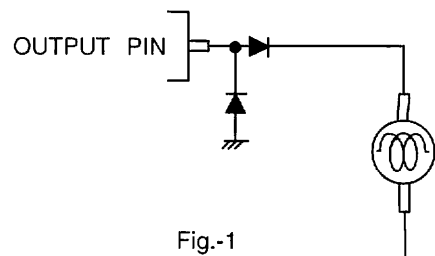


Fig.-1

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