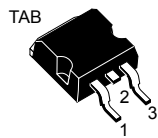
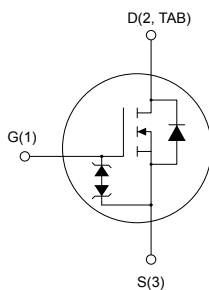


N-channel 800 V, 1.3 Ω typ., 4.5 A MDmesh K5 Power MOSFET in a D²PAK package


D²PAK


AM01476v1_tab


Product status link
[STB6N80K5](#)
Product summary

Order code	STB6N80K5
Marking	6N80K5
Package	D ² PAK
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STB6N80K5	800 V	1.6 Ω	4.5 A

- Very low FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	4.5	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	2.8	
$I_{DM}^{(1)}$	Drain current (pulsed)	18	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	85	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		$^{\circ}\text{C}$

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 4.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.47	$^{\circ}\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	30	$^{\circ}\text{C}/\text{W}$

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	1.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	85	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	800			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			50	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2\text{ A}$		1.3	1.6	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	270	-	pF
C_{oss}	Output capacitance		-	25	-	pF
C_{rss}	Reverse transfer capacitance		-	0.7	-	pF
$C_{o(tr)}^{(1)}$	Equivalent output capacitance time related	$V_{DS} = 0\text{ to }640\text{ V}$, $V_{GS} = 0\text{ V}$	-	38	-	pF
$C_{o(er)}^{(2)}$	Equivalent output capacitance energy related	$V_{DS} = 0\text{ to }640\text{ V}$, $V_{GS} = 0\text{ V}$	-	16	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	7.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 640\text{ V}$, $I_D = 4.5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	13	-	nC
Q_{gs}	Gate-source charge		-	2.1	-	nC
Q_{gd}	Gate-drain charge		-	9.6	-	nC

1. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

2. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 2.25\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	16	-	ns
t_r	Rise time		-	7.5	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	28.5	-	ns
t_f	Fall time		-	16	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		18	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 4.5\text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 4.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	280		ns
Q_{rr}	Reverse recovery charge		-	2.2		μC
I_{RRM}	Reverse recovery current		-	15.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 4.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	450		ns
Q_{rr}	Reverse recovery charge		-	3.15		μC
I_{RRM}	Reverse recovery current		-	14		A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

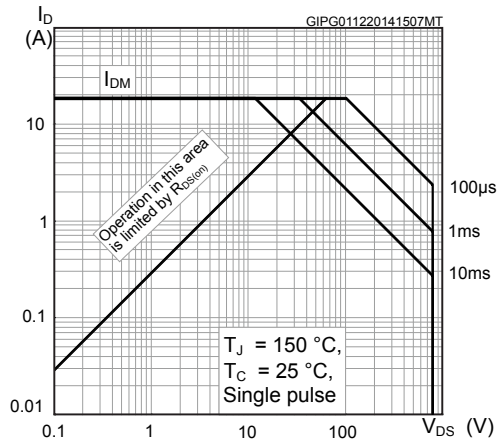
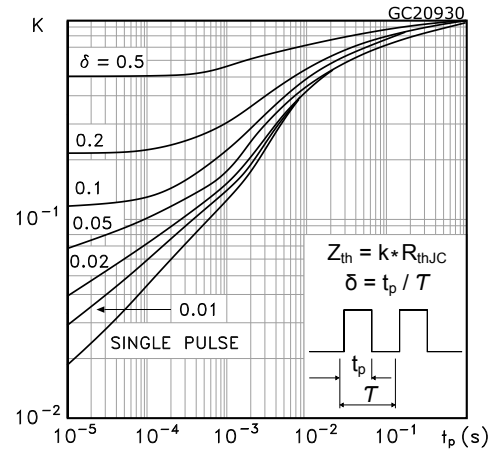
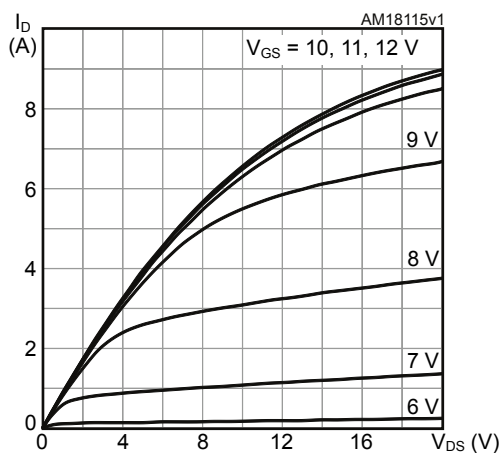
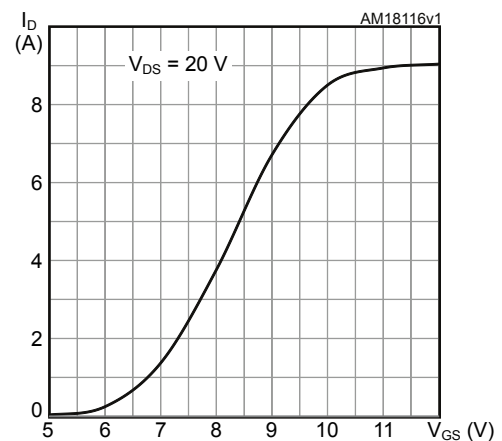
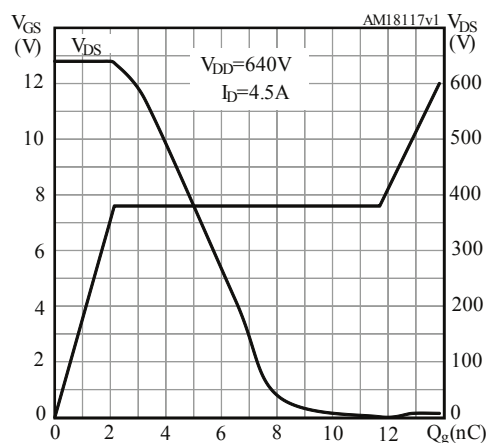
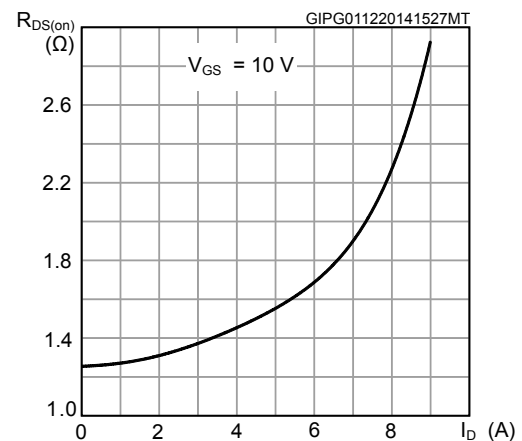
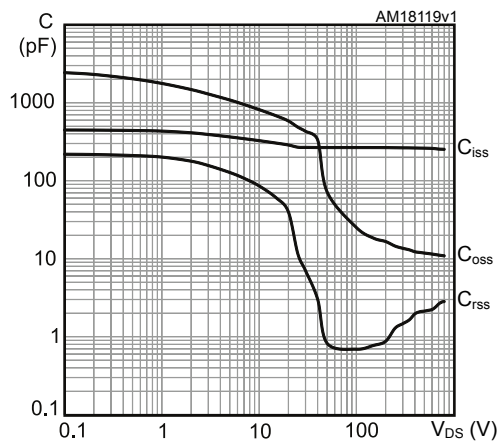
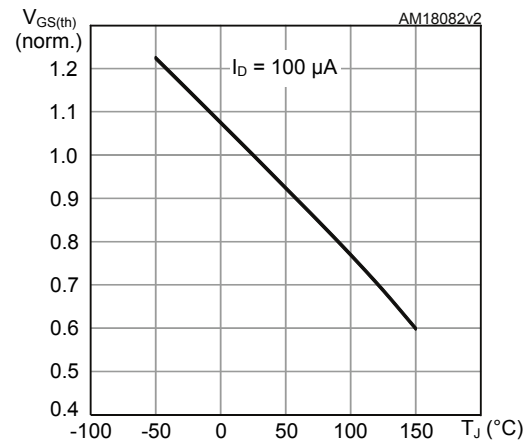
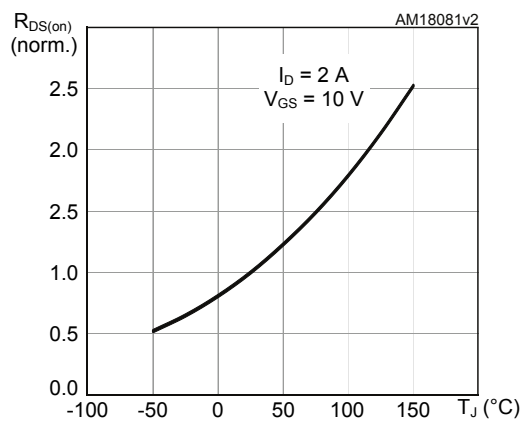
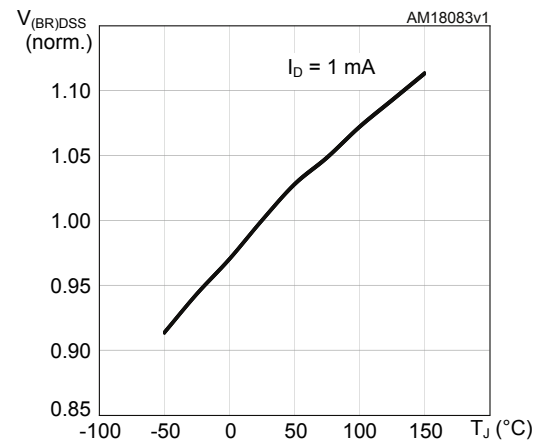
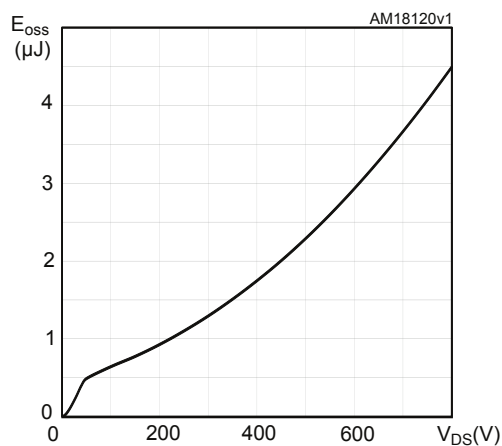
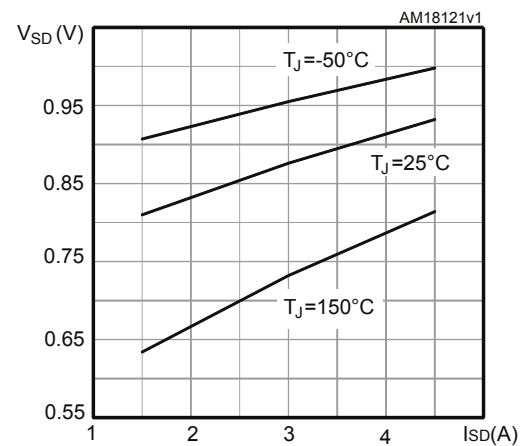
Figure 1. Safe operating area

Figure 2. Normalized transient thermal impedance

Figure 3. Typical output characteristics

Figure 4. Typical transfer characteristics

Figure 5. Typical gate charge characteristics

Figure 6. Typical drain-source on-resistance


Figure 7. Typical capacitance characteristics

Figure 8. Normalized gate threshold vs temperature

Figure 9. Normalized on-resistance vs temperature

Figure 10. Normalized breakdown voltage vs temperature

Figure 11. Typical output capacitance stored energy

Figure 12. Typical reverse diode forward characteristics


3 Test circuits

Figure 13. Test circuit for resistive load switching times



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Figure 14. Test circuit for gate charge behavior



AM01469v1

Figure 15. Test circuit for inductive load switching and diode recovery times



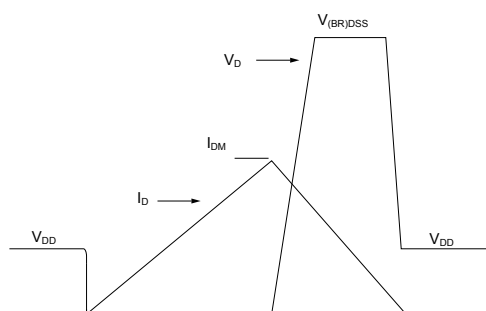
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Figure 16. Unclamped inductive load test circuit



AM01471v1

Figure 17. Unclamped inductive waveform



AM01472v1

Figure 18. Switching time waveform



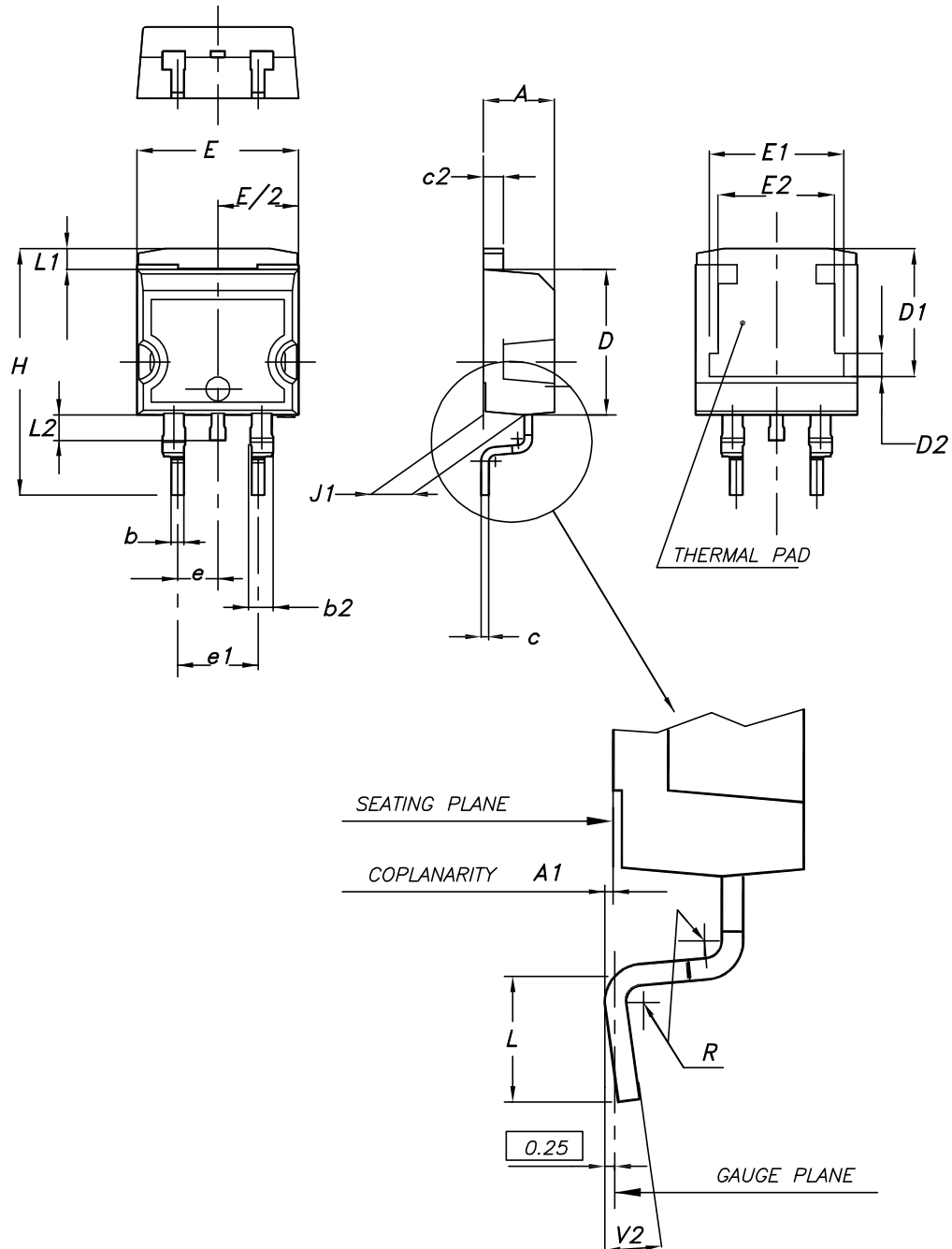
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 19. D²PAK (TO-263) type A package outline



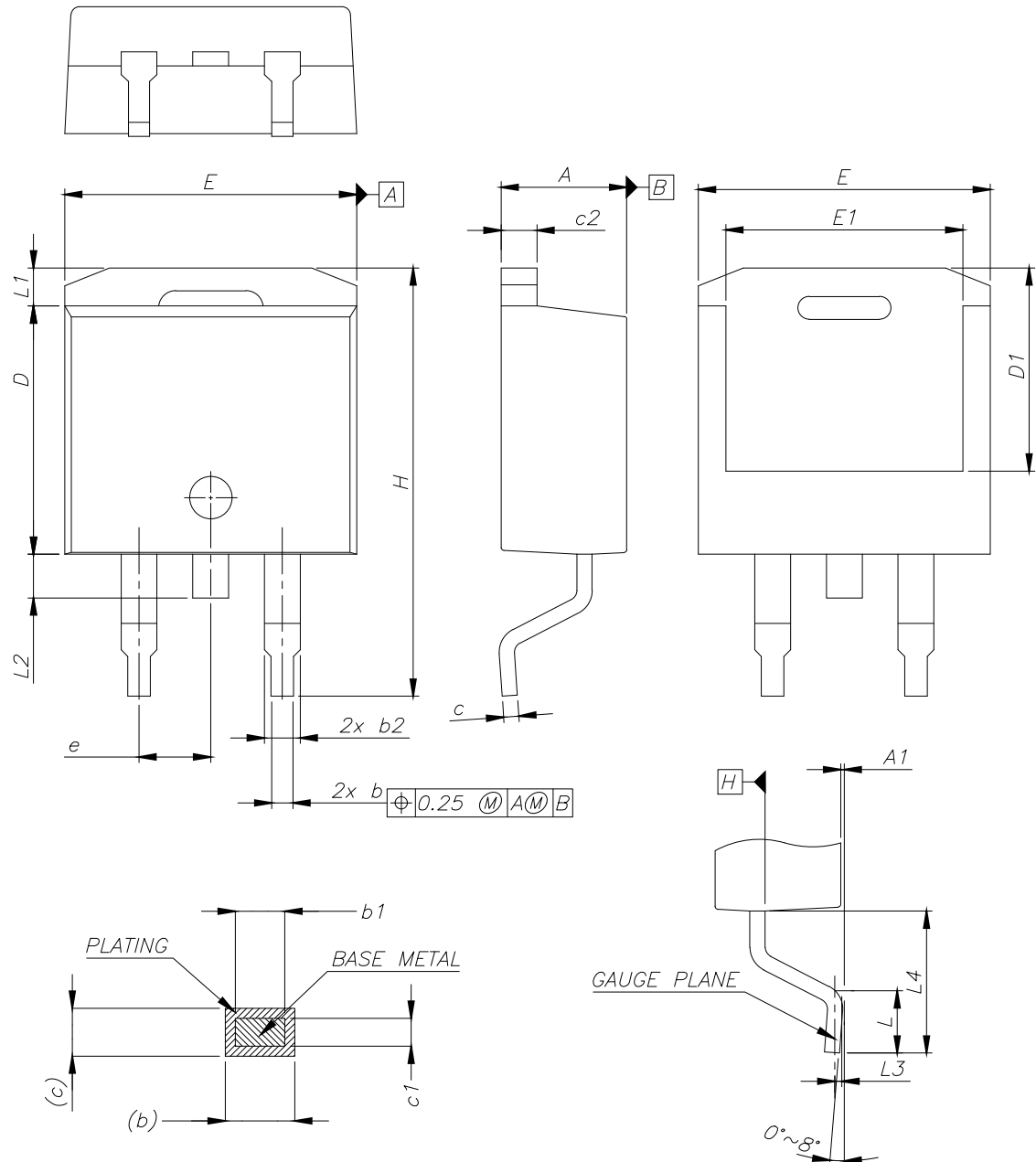
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Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

4.2 D²PAK (TO-263) type B package information

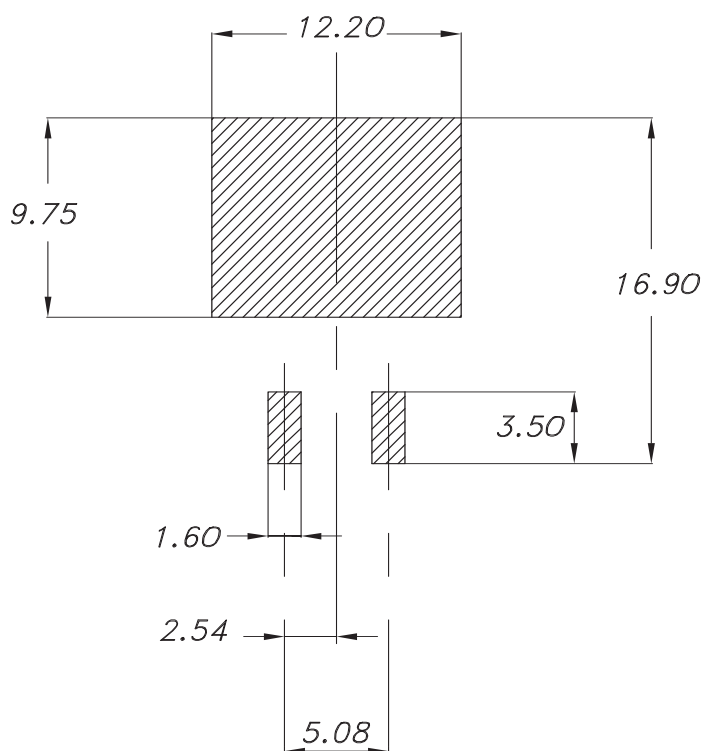
Figure 20. D²PAK (TO-263) type B package outline



0079457_27_B

Table 9. D²PAK (TO-263) type B mechanical data

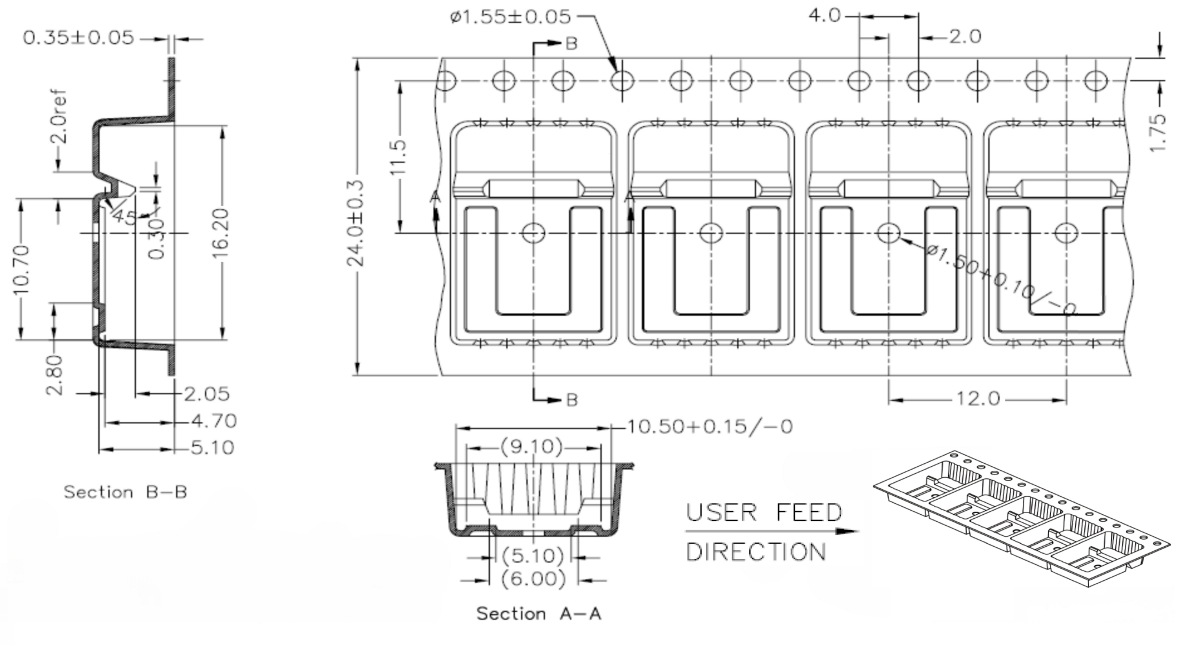
Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0.00		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

Figure 21. D²PAK (TO-263) recommended footprint (dimensions are in mm)


0079457_Rev27_footprint

4.3 D²PAK packing information

Figure 22. D²PAK tape drawing (dimensions are in mm)



DM01095771_2

Revision history

Table 10. Document revision history

Date	Revision	Changes
15-Jun-2023	1	First release. The part number STB6N80K5 was previously inserted in the DS9676.
22-Aug-2025	2	Updated <i>Section 4: Package information</i> . Minor text changes.
16-Oct-2025	3	Minor text changes.

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