Document No.: 1	M01-00-E-03
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PODICE SPECIFICATION

PRODUCT:	<u>MULTILAYER</u>	CERAMIC	<u>CAPACITOR</u>
TYPE:	CHII	P CAPACI'	ГOR

APPROVED	BY	CUSTOMER	

PAN OVERSEAS ELECTRONIC CO., LTD.

TAIWAN HEAD OFFICE: PAN OVERSEAS (GUANG ZHOU):

TAIWAN FACTORY: PAN OVERSEAS (KUN SHAN):

TEL: 06-6982143, 06-6982331 TEL: 86-512-57707888 FAX: 06-6983400,(QA:06-6993898) FAX: 86-512-57711076

QUALITY ASSURANCE DEPARTMENT					
CHECKED	PREPARED				

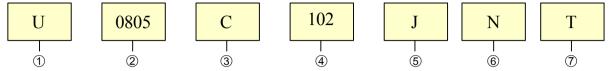
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■TAIWAN GUANG ZHOU KUN SHAN

1. SCOPE

This specification is applicable to Pan Overseas multilayer ceramic capacitors.

2. CODE CONSTRUCTION:

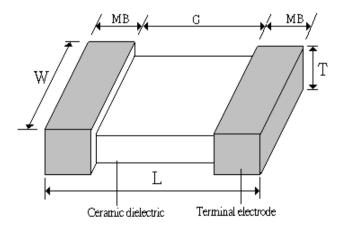


① Rated Voltage:

Code	Rated								
	voltage								
K	6.3V	T	25V	G	200V	D	630V	M3	3000V
N	10V	U	50V	H	250V	M	1000V	M4	4000V
В	16V	A	100V	C	500V	M2	2000V	M5	5000V

② Part Dimension: Unit: mm

	Length (L)	Width (W)	Dimension Thickness (T)	MB(Min)	G(Min)	
0402	1.0±0.05	0.5±0.05	0.5±0.05	0.10	0.30	6.3∼ 50V
0603	1.6±0.1	0.8±0.1	0.8±0.1	0.20	0.40	6.3~250V
0805	2.0±0.2	1.25±0.1	1.40 max.	0.25	0.70	6.3~500V
1206	3.2±0.2	1.60±0.2	1.52 max.	0.25	1.40	6.3~1KV
1210	3.2±0.3	2.5±0.3	1.8 max.	0.25	1.40	6.3~1KV
1808	4.5±0.35	2.0±0.3	2.0 max.	0.25	2.15	6.3~5KV
1812	4.5±0.35	3.2±0.3	1.8 max.	0.25	2.15	16∼5KV
2220	5.7±0.4	5.0±0.4	1.8 max.	0.25	3.30	16~5KV
2225	5.7±0.4	6.3±0.4	1.8 max.	0.25	3.30	16~5KV
3640	9.2±0.5	10.16±0.5	2.0 max.	0.50	2.70	16~5KV
5550	14.0±0.5	12.7±0.5	2.5 max.	0.50	10.5	16~5KV
8060	20.3±0.5	15.24±0.5	2.5 max.	0.50	16.8	16∼5KV



3 Temperature Characteristics Code:

Code	Temp. Coefficient	Operation Temp.	Capacitance Change
C	NP0 (Class I)	-55°C ∼ +125°C	$0 \pm 30 \text{ ppm/°C}$
R	X7R (Class II)	-55°C ∼ +125°C	± 15%
X	X5R (Class II)	-55°C ∼ +85°C	± 15%
F	Y5V (Class II)	-30°C ∼ +85°C	+22% ∼ -82%
E	Z5U (Class II)	+10°C ∼ +85°C	+22% ~ -56%

Code	Capacitano	ce(pF)	Code	Capacita	nce(pF)
010	1 *		102	1000	*
1R5	1.5		222	2200	*
100	10		47 <mark>2</mark>	4700	*
101	100	*	103	10000	*

⑤ Tolerance Code:

Code	Tolerance	Code	Tolerance
В	± 0.1pF	J	±5%
С	±0.25pF	K	±10%
D	±0.50pF	M	±20%
F	± 1%	Z	+80%/-20%
G	± 2%		

PS: 1. * -- Two significant digits followed by no. of zeros

2. Temperature coefficient (T.C.) vs. Proper tolerance applied:

NPO: For all tolerance

X7R · X5R: K · M Tolerance Y5V · Z5U: M · Z Tolerance

© Termination Code :

Code	N
Termination Type	Nickel

⑦ Packaging Code:

Code	В	T
Packaging Type	Bulk	Tape & Reel

3. STANDARD TEST CONDITIONS:

Tests shall, unless otherwise specified, be carried out at 15 to 35°C and RH 45 to 75%.

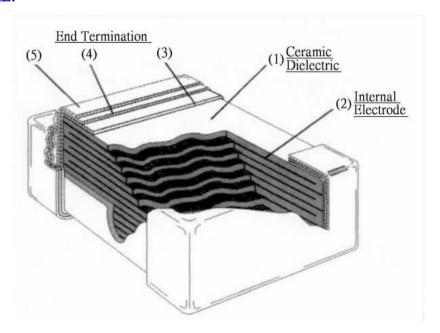
If any doubt and argument has been encounter in judgement, the final test shall be done at 25 ± 2 °C,RH45 to 55% and $860\sim1060$ mbar. (Based on JIS standard)

4. DISPOSITION

If question to the measuring result in judgement, take the capacitor under a specified temperature for 30 minutes at least before measurement.

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5. STRUCTURE:



Ag / Pd SERIES:

NO	Specifications	Material	Termination
1	Ceramic dielectric	Ceramic	Plating
2	Internal Electrode	Ag-Pd	thickness
3		Ag layer	40μ m min
4	End Terminal	Ni layer	$1.5 - 3.5 \mu$ m min
5		Sn-Pb layer or Sn layer	3-8 μ m min

BME SERIES:

NO	Specifications	Material	Termination
1	Ceramic dielectric	Ceramic	Plating
2	Internal Electrode	Ni	thickness
3		Cu layer	40μ m min
4	End Termination	Ni layer	$1.5 - 3.5 \mu$ m min
5		Sn-Pb layer or Sn layer	$3-8 \mu \text{ m min}$

6. STORING CONDITION AND TERM

Recommends the storing of products within 6 months at temperature $15\sim35^{\circ}$ C and humidity 70%RH max. If the product stored over 6 months, please reconfirm its solderability before use.

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NO.	Item	Performance	Test or Inspection method				
(1)	External Appearance	No defects which may affect performance.	Visual inspection & Dimension measurement				
(2)	Voltage Proof	of Withstand test voltage without Insulation breakdown or other		DC Tested voltage shall be applied for $1 \sim 5$ sec. Charge/discharge current shall not exceed 50 mA. (PS: Ra – Rated Voltage)			
			Rated	DO	C Tested vol	tage	
			voltage	NPO	X7R/X5R	Y5V	
			≤200V		2.5Ra		
			250V		2.0Ra		
			500V/630V		1.5Ra		
			≥1K V	1.5Ra	1.25Ra		
(3)	Insulation Resistance	Apply DC tested voltage for 60± 5 minute. (PS: Ra – Rated Voltage)					
		(Whichever is smaller) X7R, X5R, Y5V, Z5U:	Rated voltage DC Tested voltage				
		$10,000 \mathrm{M}\Omega \mathrm{\ Min}$ or $\mathrm{R} \cdot \mathrm{C} \geq 1,000 \Omega \cdot \mathrm{F}$	<1KV 1.0 Ra				
		(Whichever is smaller)	≥1KV	-	1KV		
(4)	Capacitance (Cap.)	Within the specified tolerance that refers on page 2	Measuring to Z5U \ Y5V	-	-	± 50Hz。	
(5)	Dissipation	NPO:	NPO: > 10	000pF : 1	KHz± 50Hz	7 0	
	Factor (D. F.)	$\geq 30 \text{pF}: Q \geq 1000$		-	MHz± 100K	Hz	
		< 30pF : Q≥400+20C	Measuring v	•			
		PS: C: Nominal Capacitance (pF) X7R \ X5R \ Y5V & Z5U \ (Max. value)	Z5U: 0.5 V NPO · X7R		V5V:10+	0.2 Vrms	
		$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	THE TANK	72010	10 (1.0_	o.2 viiiis	

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NO.		Item		Perform	nance	Test	or Inspection method
(6)	Temper		T		Coefficient	determine	perature coefficient is ed using the capacitance
	Charac Capacit	teristic of	T.C.	Operating	Change (A C)	Test the	in step 3 as a reference. specimen from step 1
	Сиристинос		NPO	Temperature -55~+125°C	Change(Δ C) 0±30(ppm/°C)	be within	the specified tolerance for citance coefficient and
			X7R	-55~+125°C	± 15%		re change as left table. Temperature(°C)
			X5R	-55~+85°C	± 15%	1	Base Temp.(25°C)± 2 °C
			Y5V	-30~+85°C	+22%~- 82%	3	Min. Operation Temp.± 2 °C Base Temp.(25°C)± 2 °C
			Z5U	+10~+85°C	+22%~ -56%	5	Max. Operation Temp.± 2 °C Base Temp.(25°C)± 2 °C
(7)	Soldera	ibility		solder to ovenation	er 95% of	solder at spe a. For Tin-L 235±5°(b. For Lea	soak both terminal electrodes in ecified temperature for 3±0.5 sec.: lead Sn/Pb) Termination product: ad-free (Pure Sn) Termination 245±5°C
(8)	Leachir	ng		solder to ovenation	er 95% of	Completely soak both terminal electrodes in solder at 270±5°C for 40±1 sec.	
(9)	Solder-	External appearance	No mechanical damage.		Completely immerse both terminations in solder at 270±5°C for		
	ing to	Cap. change	NPO		± 0.25 pF max.	10±3 sec.	
	Heat	$(\Delta C/C)$	X7R/X Z5U Y5V	±7.5% ±20%	chever is larger)		e capacitors in ambient n for 24± 2 hours before
		D.F.	NPO	: C≥30pF C <30pF	: Q≥1000 : Q≥400+20*C Capacitance (pF)	measurem *Precondi	ent. tioning: (only for Class 2):
			X7R/ X7R/ X5R	X5R, ¥5V25 ≦50¥5V25	$\frac{75 \text{U}}{16} = \frac{100}{100}$ $\frac{75 \text{U}}{16} = \frac{100}{100}$ $\frac{75 \text{U}}{100} = \frac{100}{100}$	Perform a heat treatment at 150 +(
			Z5U Y5V	4.0% 5.0% 7.5°	 % 9.0% 12.5%	24 ± 2 hours at room temperature. Perform the initial measurement.	
		I.R.	R • (Wh X7R \ 10,0 R •	$0.000M\Omega$ Min. $C \ge 1,000$ nichever is small $X5R \cdot Y5V \cdot 0.000M\Omega$ Min $C \ge 1,0000$ hichever is small $0.000M\Omega$	Ω · F aller) · Z5U: or ⊇ · F		

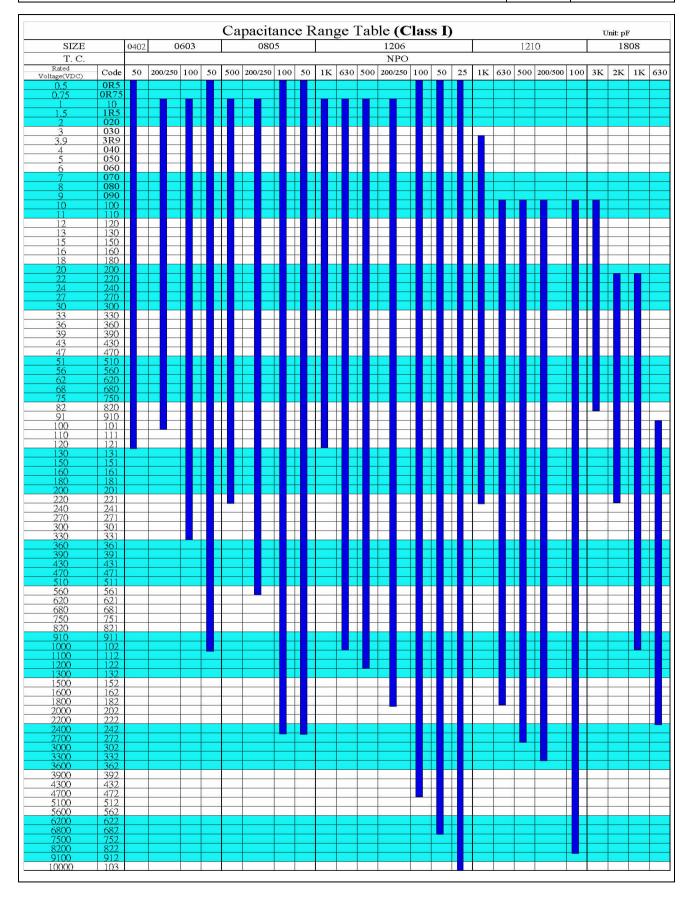
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NO.	It	em	Performance	Test or Inspection method
(10)	Humidity (Steady	External appearance	No mechanical damage.	A. Humidity load: (Not apply for the product with rated voltage ≥ 250V):
	state) & Humidity load	Cap. change $(\Delta C/C)$	NPO: ±5% or ±0.5 pFmax. (Whichever is larger) X7R/ X5R: ± 12.5% Y5V: ±30% Z5U: ±30%	Apply the rated voltage at temperature 40±2°C and humidity 90 to 95%RH for 1000+48/−0 hours. Leave the capacitors in ambient
		D.F.	NPO: $C \ge 30 \text{pF}$: $Q \ge 350$ $10 \text{pF} \le C < 30 \text{pF}$: $Q \ge 100 + 2.5 * C$ C < 10 pF: $200 + 10 * CPS: C: Nominal Capacitance (pF)X7R/ X5R: Less than 2 timesof initial valueY5V & Z5U: Less than 1.5$	condition for the following time before measurement. Class 1: 1~2 hours. Class 2: 24± 2 hours. * Charge / discharge current shall. not exceed 50 mA. * Preconditioning: (only for Class 2): Apply the rated DC voltage for 1hour at 40±2°C. Remove and let sit for 48±4 hours at room temperature. Perform initial measurement.
		I.R.	times of initial value $500M\Omega$ min. or $25\Omega*F$ (Whichever is smaller)	B. Humidity (Steady state): The test procedure is same as that in Humidity load but only without rated voltage applied.
(11)	Load Life	External appearance Cap. change (\(\Delta\) C/C) D.F.	No mechanical damage. NPO: ±3% or ±0.3pFmax. (Whichever is larger) X7R/X5R: ± 12.5% Y5V: ±30% Z5U: ±30% NPO: C≥30pF: Q≥350 30pF>C≥10pF: Q≥275+2.5*C C<10pF: Q≥200+10*C PS: C: Nominal Capacitance (pF) X7R/X5R: Less than 2 times of initial value Y5V & Z5U: Less than 1.5 times of initial value	Apply 2× rated voltage at maximum operating temperature ±2°C for 1000 +48/-0 hours. Leave the capacitors in ambient condition for the following time before measurement. Class I: 1~2 hours Class II: 24± 2 hours * Charge / discharge current shall. not exceed 50 mA. * Preconditioning: (only for Class 2): Apply 200% of the rated DC voltage for 1 hour at the maximum operating temperature ± 3°C. Remove and let sit for 24±2 hours at room temperature. Perform initial measurement.
		I.R.	1000MΩ min. or $50Ω*F$ (Whichever is smaller)	1 errorm minum medourement.

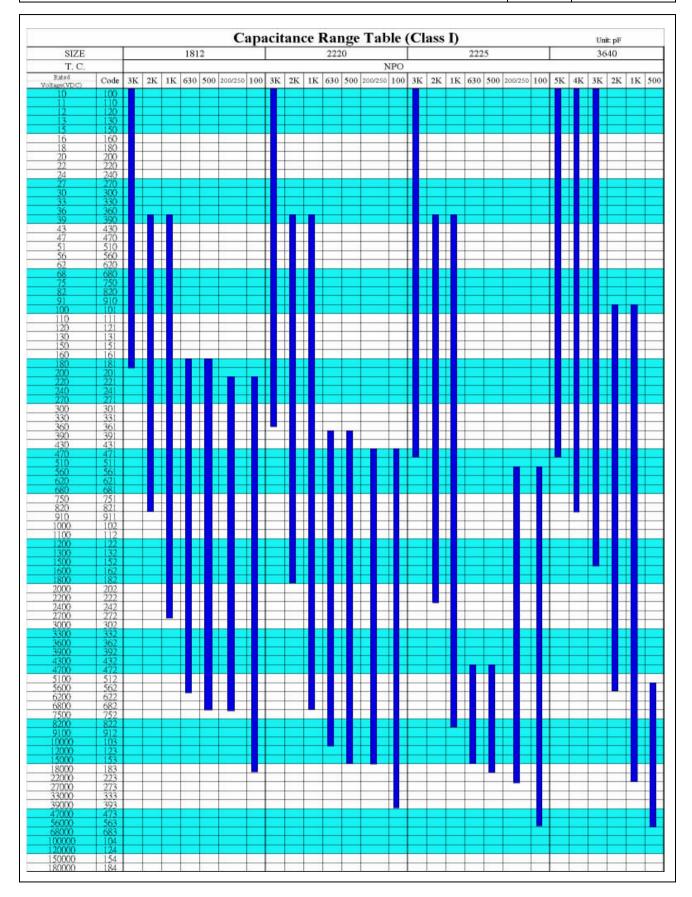
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NO.	Ite	em	Performance	Test or Inspection method
(12	Vibration	External appearance Cap. change $(\Delta \text{ C/C})$	Without distinct damage NPO: ±2.5% or ±0.25pF max. (Whichever is larger) X7R/ X5R: ± 7.5% Y5V \ Z5U: ±20% NPO: C≥30pF: Q≥1000 C <30pF: Q≥400+20*C PS: C: Nominal Capacitance (pF)	(Not apply for 0402 product) Solder the capacitors to the test jig as shown in figure below with IR-Reflow method. The capacitor shall be subjected to a simple harmonic motion with the entire frequency range, from 10 to 55 Hz and return to 10 Hz ,shall be transverse in 1 min. Amplitude(total excursion):1.5mm Amplitude tolerance:± 15% This motion shall be applied for a period of 2 hours in each of 3 mutually perpendicular
			$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	directions (a total of 6 hours)
(13	Deflectio n		No cracking or marking defects shall occur	200 50 584 5 : misses
		Bending strength Cap. change (\(\Delta \text{C/C} \)	Flexure ≥ 1 mm NPO: ±5% or±0.5pFmax. (Whichever is larger) X7R/ X5R: ±12.5% Y5V: ±30%	93 = 6 2 lm 2 + 2 + 2 q 45 45
(14	Temperatur	External	No mechanical damage.	(Not apply for 0402 product)
)	e cycle	appearance Cap. change $(\Delta C/C)$	NPO: ±2.5% or ±0.25pFmax. (Whichever is larger) X7R / X5R: ± 7.5% Y5V: ± 20% NPO: C≥30pF: Q≥1000	The capacitor shall be subject 5 cycles according to four heat treatments listed in the following table. Then Leave the capacitors in ambient condition for the following time before measurement. Class II: 2 ~ 24 hours
			$C \le 30 \text{pF} : Q \le 1000$ $C < 30 \text{pF} : Q \ge 400 + 20 \text{*C}$	Step Temperature (°C) Duration (min.)
			$X7R \cdot X5R \ Y5V\&Z5U: (Max. value)$ $T.C. \ge 50V \ 25V \ 16V \le 10V$ $X7R/ \ X5R \ 2.5\% \ 3.0\% \ 3.5\% \ 5.0\%$ $Z5U \ 4.0\% \ \ \ Y5V \ 5.0\% \ 7.5\% \ 9.0\% \ 12.5\%$	1 Min. Operation Temp.±3 30±3 2 Room Temp. (25°C) 2 ~ 5 3 Max. Operation Temp.±3 30±3 4 Room Temp. (25°C) 2 ~ 5 *Preconditioning: (only for Class 2): Perform a heat treatment at 150 +0-10°C for one hour and then let sit
		I.R.	10000MΩ min. or $500\Omega*F$ (Whichever is smaller)	for 24±2 hours at room temperature. Perform the initial measurement.

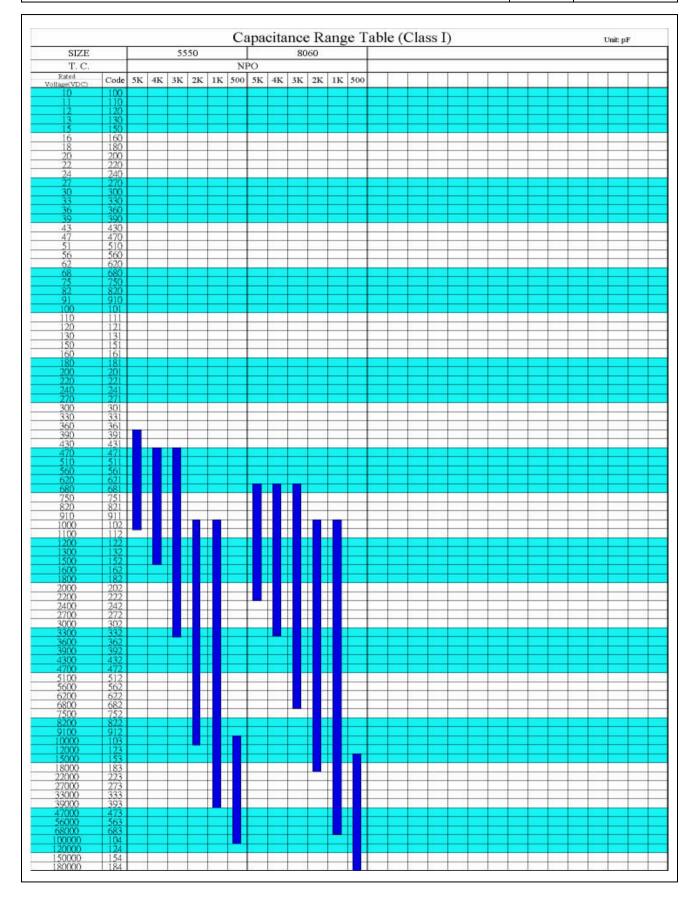
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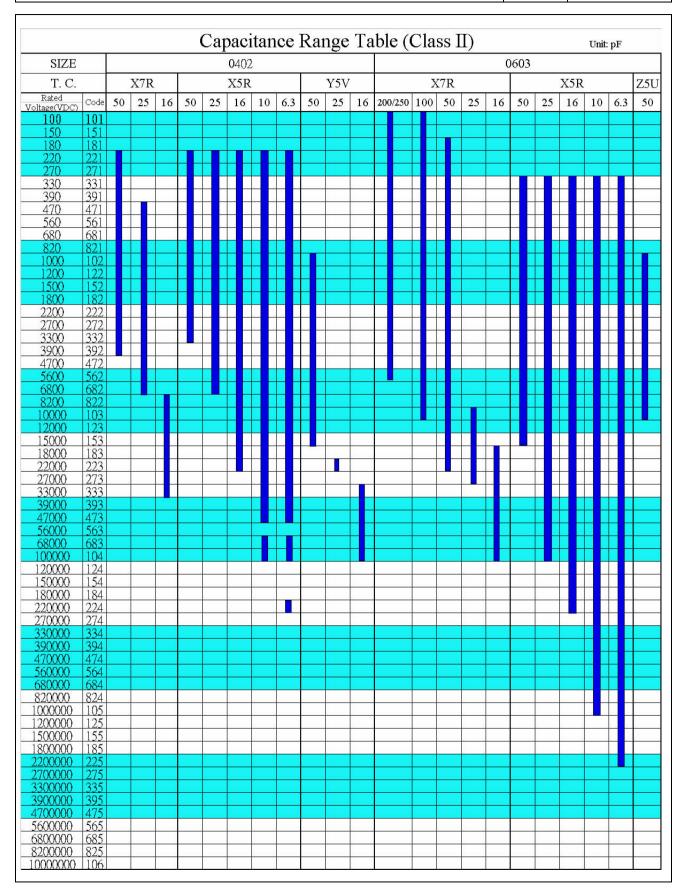
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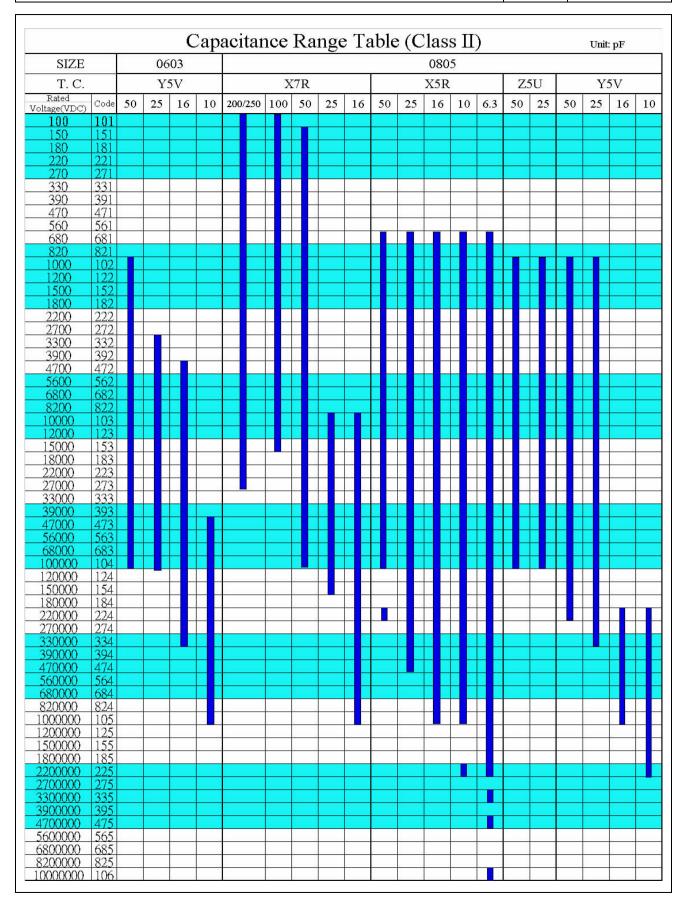
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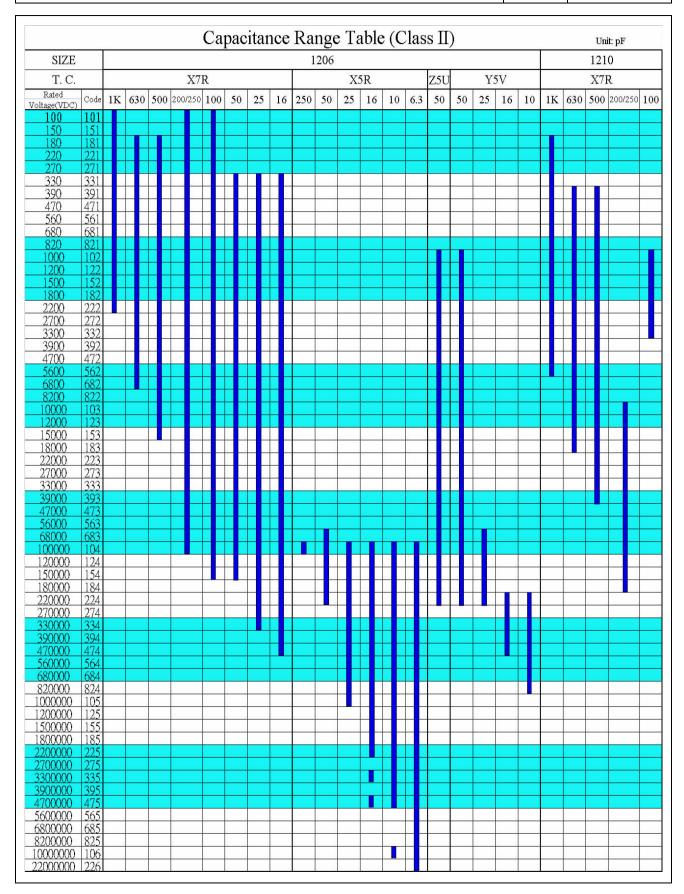
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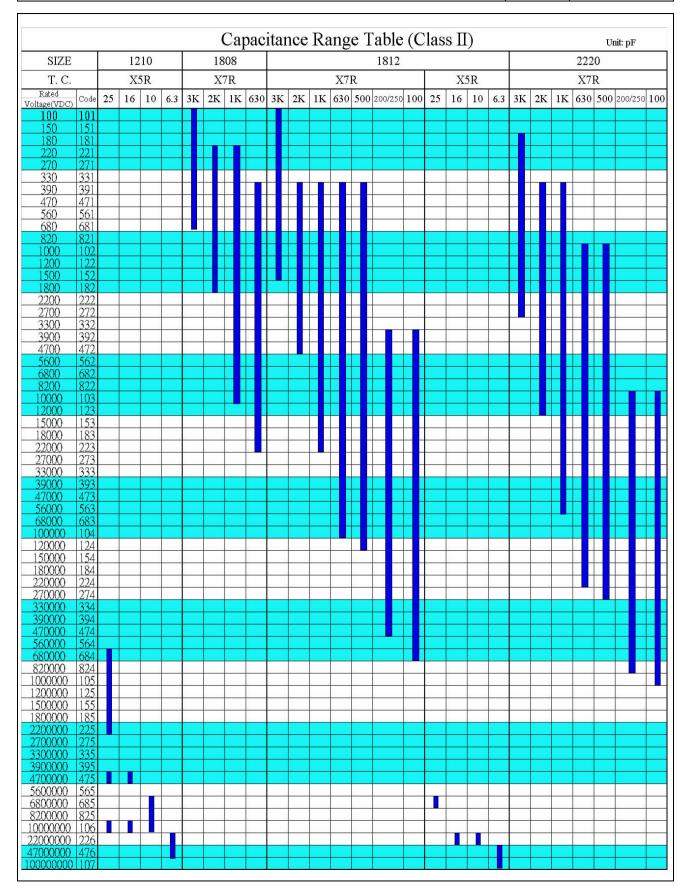
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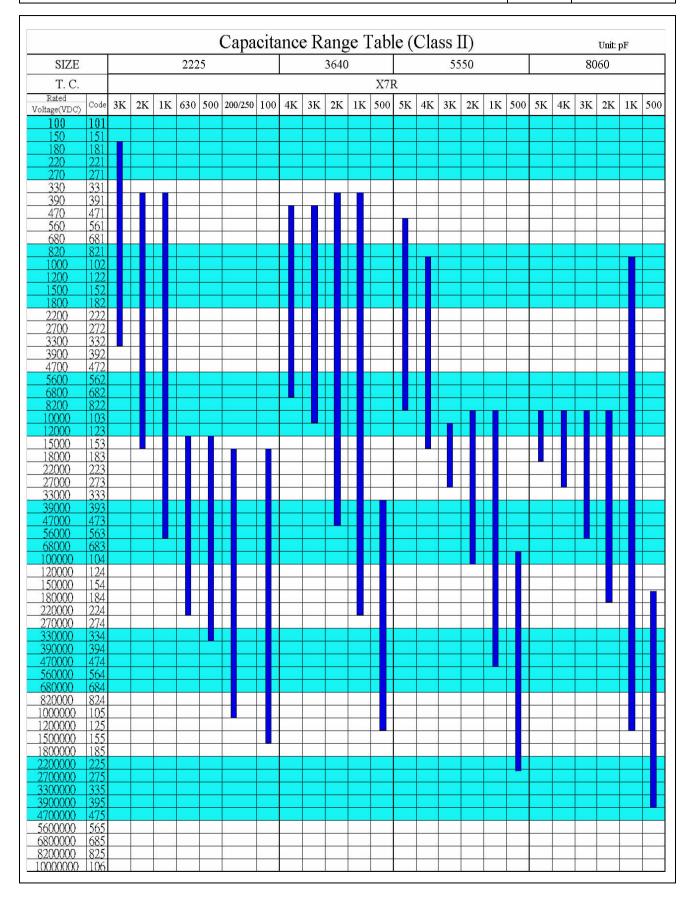
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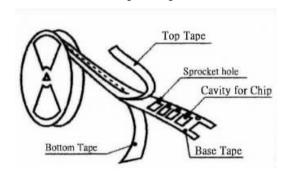


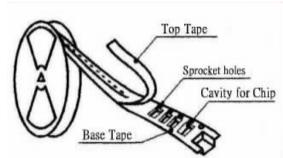
10. Packaging:

(1)Reel specification: Standard reel diameter is 7" and 13"

Paper Tape







Packed Chips
Pitch Hole

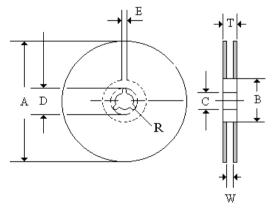
Component

Taping condition

(2) Quantity for each reel

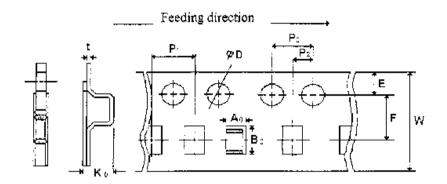
Ch	ip Size	0402	0603	0805	1206	1210	1808	1812	2220	2225	3640	5550	8060
Reel	7"	10000	4000	3000	2500	2000	2000	1000	1000	1000	N/A	N/A	N/A
Size	13"	50000	16000	12000	10000	8000	8000	4000	4000	4000	N/A	N/A	N/A
Tape	wide(mm)	8	8	8	8/12	8/12	8/12	8/12	8/12	8/12	N/A	N/A	N/A

(3) Dimension of Reel:



Dimens	sion	A	В	C	D	E	T	W
D 10.	7"	178±2	50 :	12.0.5	13±0.5 21±0.8	20.05	12±2.0	10±1.5
Reel Size	13"	330 max	50 min.	13±0.5		2.0±0.5	18.4max.	12.4 +1.5/-0

(4) Tape Dimension:



Unit: inch (mm)

Symbol	Description	8 mm tape	12 mm tape			
W	Wide of Tape	8(0.135)±0.2(0.008)	12(0.472)±0.2(0.008)			
F	Distance between drive hole center and cavity center	3.5(0.138)±0.05(0.002)	5.5(0.213)±0.05(0.002)			
Е	Distance between drive hole center and tape edge	r 1.75(0.069)±0.1(0.004)				
\mathbf{P}_1	Distance between cavity center	4(0.156)±0.1(0.004)	8(0.135)±0.1(0.004)			
P ₂	Axial distance between drive hole center and cavity center	2(0.079)±0.05(0.002)				
P_0	Axial distance between drive hole	4(0.156)±0.1(0.004)			
D_0	Drive hole diameter	1.5(0.059)+0.1(0.004)-0				
t_1	Base tape thickness	0.3(0.012)±0.1(0.004)	0.4(0.016)±0.1(0.004)			
t_2	Total tape thickness	0.1(0.004) max.				

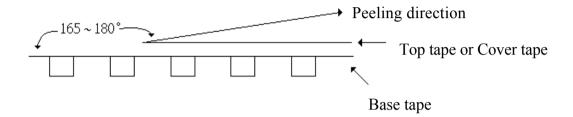
	0402	0603	0805	1206	1210 and above
A ₀ (Wide of Cavity)	0.65±0.1	1.05±0.1	1.55±0.15	2.0±0.2	Dependent on chip size to
B ₀ (Length of Cavity)	1.15±0.1	1.85±0.1	2.3±0.15	3.6±0.2	minimize rotation

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(5) Peeling off strength of Top tape

The angle between top tape and base tape is $165 \sim 180^{\circ}$, and the peeling speed is control in $300\pm~10$ mm/min, and the peeling force as follows:

- a. 8mm tape or base tape : $10 \sim 100$ grams $(0.1 \sim 1.0 \text{N})$
- b. 12mm tape or base tape: $10 \sim 130$ grams $(0.1 \sim 1.3\text{N})$



PRECAUTION FOR HANDLING

The multi-layer ceramic chip capacitors, may fall in a short circuit mode or in an open-circuit mode when subjected to severe conditions of electrical, environmental and/or mechanical stress beyond the specified "Ratings" and specified "Condition" in the Catalog and the Specifications, resulting in burnout, flaming or glowing in the worst case. So some common sense of application by customer is necessary. Here the following article are some key points that need to take attention in application for customer reference only:

1. Operating Conditions and Circuit Design

1.1 Operating temperature range

The specified "Operating Temperature Range" in the catalog is absolute maximum and minimum temperature rating. So in any case, each the Capacitor shall be operated within the specified "Operating Temperature Range".

1.2 Design of Voltage Applications

The capacitors shall not be operated exceeding the specified "Rated Voltage" in the catalog. If voltage ratings are exceeded the Capacitors could result in failure of damage. In case of application of DC and AC voltage to the capacitors, the designed peak voltage shall be within the specified "Rated Voltage".

1.3 Charging and Discharging Current

The capacitors shall not be operated beyond the specified "Maximum Charging / Discharging Current Rated" in the specification, Application to a low impedance circuit such as a "secondary power circuit" are not recommended for safety.

1.4Temperature Rise by Dielectric Loss of the capacitor

The "Operating Temperature Range" mentioned above shall include a maximum surface temperature rise of 20°C, which is caused by the Dielectric loss of the Capacitor and applied electrical stress (such as voltage, frequency and wave form etc.)

It is recommended to measure and check "Surface temperature of the Capacitor" in your equipment at your estimated / designed maximum ambient temperature.

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1.5 Restriction on Environmental Conditions

The Capacitors shall not be operated and / or stored under following environmental conditions:

- (a) To be exposed directly to water or salt water.
- (b) To be exposed directly to sunlight.
- (c) Under conditions of dew formation.
- (d)Under conditions of corrosive atmosphere such as hydrogen sulfas, sulfurous acid, chlorine, or ammonia etc.
- (e)Under severe condition of vibrations or shock beyond the specified conditions in the Specifications.

1.6 Secular change in Capacitance

- (1) Peculiar characteristics of "Secular Changes in Capacitance" are observed in the Capacitors (Class 2 High Dielectric Constant Temperature Characteristics "X7R" and "Y5V". The "secular change" shall be considered in your circuit design.
- (2) The Capacitance change, due to the individual characteristics of ceramic dielectric materials applied, can be recovered to the each initial values at shipping by a heat treatment (140 to 150°C for 1 hour).

2. Design of Printed Circuit Board

2.1 Selection of Printed Circuit Boards

When the Capacitors are mounted and soldered on an "Aluminum's Substrate has influences on Capacitor's reliability against "Temperatures Cycles" and "Heat shock" because of difference of thermal expansion dose not deterioration the characteristics of the Capacitors.

There are some thermal expansion factor for different kink of PC board material as follows:

PC board material	Thermal expansion factor (mm/°C)
Glass epoxy	1.4×10 ⁻⁵
Paper phenol	2.2×10 ⁻⁵
Composite	2.2×10 ⁻⁵
Alumina	6.5×10 ⁻⁶

2.2 Design of Land Pattern

(1) Recommended Dimensions of Lands. As shown in Table 1 and Fig 1.

Note: * Too large land required excess amount of solder.

** The Dimensions shall be symmetrical.

Fig.1 Recommended Land Dimensions:

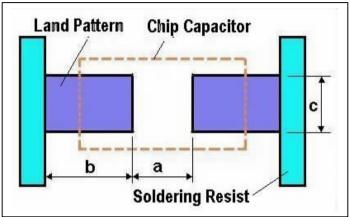


Table 1: Recommended Land Dimensions in mm.

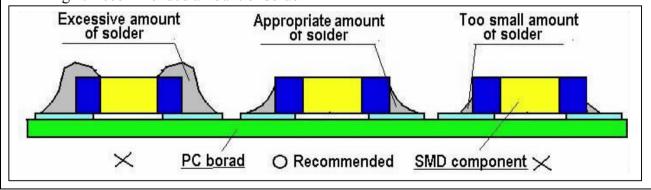
g:	Chip Dimension		Land Dimension		on
Size	L	W	a	b	c
0402	1.0	0.5	0.30~0.50	0.35~0.45	0.40~0.60
0603	1.6	0.8	0.70~1.00	0.80~1.00	0.60~0.80
0805	2.0	1.25	1.00~1.30	1.00~1.20	0.80~1.10
1206	3.2	1.6	2.10~2.50	1.10~1.30	1.10~1.30
1210	3.2	2.5	2.10~2.50	1.10~1.30	1.90~2.30
1808	4.5	2.0	2.50~3.20	1.80~2.30	1.50~1.80
1812	4.5	3.2	2.50~3.20	1.80~2.30	2.60~3.00
2220	5.7	5.0	4.20~4.70	2.00~2.50	4.20~4.70

(2) Recommend amount of solder:

Recommended amount of solder: As shown in Fig 2.

Excess amount of solder gives large mechanical stresses to the capacitors / Components.

Fig 2: Recommended amount of solder

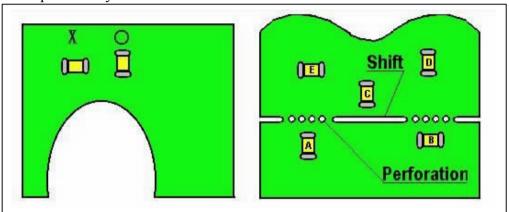


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2.3 Component Layout

When placing / mounting the capacitors / components near an area which is apt to bend or a grid groove on the PC board. It is advisable to have both electrodes subjected to uniform stresses, or to position the component electrodes at right angles to the grid groove or bending line.

Fig 3: Component Layout



Uneven mounting density

O: Proper ×: Improper

Probability at which the chip capacitor is broken by the stress on PC board break

$$A>B=C>D>E$$

2.4 Mounting Density and Spaces

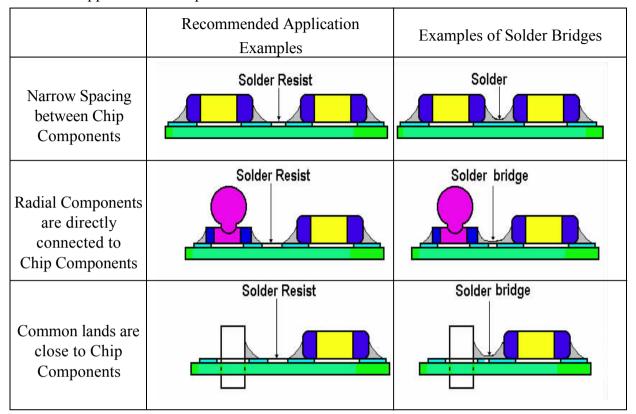
Placements in too narrow spaces between components may cause "Solder Bridges" during soldering. The minimum space between components shall be 0.5mm in view of the positioning tolerances of the mounting machines and the dimensional tolerances of the components and PC boards.

2.5 Applications of Solder Resist:

Application of Solder Resist are effective to prevent solder bridges and to control amounts of solder on PC boards (As shown in Table 2).

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Table 2: Application Examples of Solder Resist



3. Precautions for Assembly

3.1 Adhesives for Mounting

(1) Selection of adhesives

- a. The viscosity of a adhesive for mountings shall be such that the adhesive dose not flow off on the land during it's curing.
- b. If the adhesive is too low in its viscosity, mounted components may be out of alignment after or during soldering.
- c. The adhesives shall not be corrosive of chemically active to the mounted components and the PC boards.
- d. The amount of adhesive shall be such that the adhesive dose not flow off or be out of alignment.
- e. Adhesives for mountings can be cured by ultraviolet or infrared radiation. In order to prevent the terminal electrodes of the Capacitors The curing shall be done at conditions of 180°C max, for 2 minutes max.

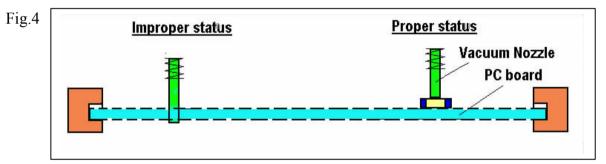
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3.2 Chip Mounting consideration

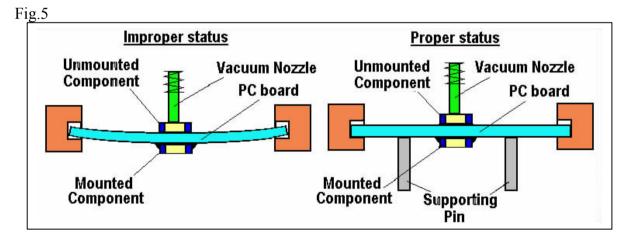
In mounting the Capacitors / components on a printed circuit board, any bending and expanding force against them shall be kept minimum to prevent them from being damaged or cracked.

Following precautions and recommendation shall be observed carefully in the process:

- (1) Maximum stroke of the vacuum nozzle shall be adjusted so that the pushing force to the printed circuit board shall be limited to a static of 1 to 3 N (100 to 300 gf) (See Fig.4).
- (2) Maximum stroke of the nozzle shall be adjusted so that the maximum bending of printed circuit board dose not exceeded 0.5mm (See Fig.4)



(3) The printed circuit board shall be supported by means of adequate supporting pins as shown in Fig.5-(b)



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3.3 Soldering Flux and Solder

- (1) Solder Flux:
 - a. The content of halogen in the soldering shall be 0.2 wt% or less.
 - b. Rosin-based and non-activated soldering flux is recommended.
- (2) Water soluble type Soldering Flux:

In case of water soluble type soldering flux being applied, the flux residue on the surface of PC boards may have influences on the reliability of the components and cause deterioration and failures of them.

(3) Solder:

An eutectic solder (Sn63: Pb37) is recommended.

3.4 Soldering

Since a multilayer ceramic chip capacitor comes into direct contact with melted solder during soldering. It is exposed to potentially damaging mechanical stress caused by the sudden temperature change. The capacitor may also be subject to silver migration, and to contamination by the flux. Because of these factors, soldering technique is critical. Adhere to the following guidelines.

3.4.1 Hand soldering:

In hand soldering of the Capacitors, large temperature gradient between preheated the capacitors and the tip of soldering iron may cause electrical failures and mechanical damages such as cracking of breaking of the devices. The soldering shall be carefully controlled and carried out so that the temperature gradient is kept minimum with following recommended conditions for hand soldering.

Recommended Soldering Conditions:

- (1) Solder:
 - φ 1mm Thread eutectic solder (Sn63:Pb37) with soldering flux *in the core.
 - *Rosin-based, and mom-activated flux is recommended.
- (2) Preheating:

The capacitors shall be preheated so that "Temperature Gradient" between the devices and the tip of soldering iron is 150°C or below.

(3) Soldering iron:

Rated Power of 20W Max with 3mm soldering tip in diameter.

Temperature of soldering iron tip: 300°C max.

(The required amount of solder shall be melted in advance on the soldering tip.)

(4) Cooling:

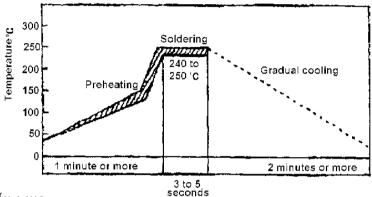
After soldering, the Capacitors shall cooled gradually at room ambient temperature.

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3.4.2.Flow Soldering

In flow soldering process, abnormal and thermal and mechanical stresses, caused by "Temperature Gradient" between the mounted Capacitors, resulting in failures and damages of the capacitors. So it is essential that the soldering process shall controlled to the following recommended conditions and precautions. (See Fig. 6)

Fig.6. Recommended Soldering Temperature Time Profile (Flow soldering)



(1) Application 6. 1 1ux.

The soldering flux(3.3) shall applied to the mounted Capacitors thinly and uniformly by forming method.

(2) Preheating:

The mounted Capacitors / Components shall be preheated sufficiently so that the "Temperature Gradient" between the Capacitors / Components and the melted solder shall be 150°C or below.

(3) Immersion to Soldering Bath:

The Capacitors shall be immersed into a soldering bath of 240 to 250°C for 3 to 5 seconds.

(4) Cooling:

The Capacitors shall be cooled gradually to room ambient temperature with the cooling temperature rates of 8° C/s max. from 250°C to 170°C and 4° C/s max. from 170°C to 130°C.

(5) Flux Cleaning:

When the Capacitors are immersed into cleaning solvent, it shall be confirmed that the surface temperature of devices do not exceed 100° C (See 3.5).

3.4.3 Reflow soldering.

In reflow soldering process, the mounted Capacitors / Components are generally heated and Soldering by a thermal conduction system such as an 'Infrared radiation and hot blast soldering system' or a "Vapor Phase Soldering System(VPS)", Large temperature gradients such as a rapid heating and cooling in the process may cause electrical and mechanical damages if the device. It is essential that the soldering process shall be controlled by following recommended conditions and precaution. (See Fig.7)

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3.4.3.1 For Tin-Lead (Sn/Pb) Termination component:

(1) Preheating 1.

The mounted Capacitors / Components shall be preheated sufficiently, for 60 to 90 seconds so that the surface temperature of them to be 140 to 150° C.

(2) Preheating 2.

After "Preheating 1", the mounted Capacitors / Components shall be the elevated temperature of 150 to 200°C for 2 to 6 Seconds.

(3) Soldering:

The mounted Capacitors / Components shall be heated under the specified heating conditions (200 to 240 to 200°C for total 20 to 40 seconds, See Fig.7) and shall be soldered at the maximum temperature of 240°C for 10 seconds of less.

(4) Cooling:

After the soldering, the mounted Capacitors / Components shall be gradually cooled to room ambient temperature for preventing mechanical damages such as cracking of the devices.

(5) Flux Cleaning:

When the mounted Capacitors / Components are immersed into cleaning solvent, it shall be confirmed the surfaces temperatures of them do not exceeding 100° C.

Note: If the mounted Capacitors / Components are partially heated in the soldering process, the devices may be separated form the printed circuit board by the surface tension of partially melted solder, and stand up like a "Tomb Stone".

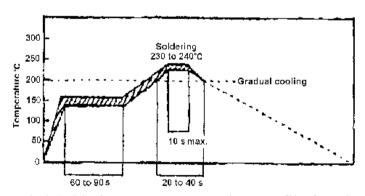


Fig. 7. Recommended Soldering Temperature Time Profile for Tin-Lead component (Reflow Soldering)

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3.4.3.2 For Lead-free (Pure Tin plating termination) Termination component:

Essentially, the soldering temperature for Lead-free component is a little higher than that for Tin-Lead component, but need to take consideration of the thermal effect for all other components mounting on board at the same time. The below picture is a recommended soldering profile for Lead-free component:

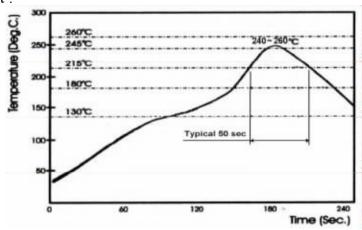


Fig.8 Recommended Soldering Temperature Time Profile for Lead-free component (Reflow Soldering)

3.5 Post soldering Cleaning

- (1) Residues of corrosive soldering fluxes on the PC board after cleaning may greatly have influences on the electrical characteristics and the reliability, (such as humidity resistance) of the Capacitors, which have been mounted on the board. It shall be confirmed that the characteristic and reliability at the devices are no effected by applied cleaning conditions.
- (2) Solubility of alternative cleaning solvent such as alcohol etc., is inferior to that of Freon cleaning solvent in the flux cleaning.
- So in case of alternative cleaning solvents, fresh cleaning solvent shall be used, and sufficient rinsing and drying shall carried out.
- (3) When an ultrasonic cleaning is applied to the mounted Capacitors on PC board, following conditions energy and the recommended for preventing failures or damages of the devices due to the large vibration energy and the resonant caused by the ultrasonic waves.

Frequency :29KHz max.

Radiated Power: 20 W/liter max.

Period :5 minutes max.

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3.6 Process Inspection

When the mounted printed circuit are inspected with measuring terminal pins, abnormal and excess mechanical stresses shall not be applied to the PC board mounted components, to prevent failure or damages of the devices.

- (1) The mounted PC board shall be supported a same adequate supporting pins prevent their banding.
- (2) It shall be confirmed that the measuring pin have the right tip in shape, equal in height and are set in the tight positions.
- (3) The amount of adhesive shall be such that the adhesive dose flow off or be out of alignment.

3.7 Protective Coating

When the surface of a printed board on which the Capacitors has been mounted is coated with Resin to protect against moisture and dust, it shall be confirmed that the protective coat dose not have influences on reliability of the capacitors in the actual equipment.

- (1) Coating materials, such as being corrosive and chemically active, shall not be applied to the capacitors and other components.
- (2) Coating materials with a large expansively shall not be applied to the Capacitors for preventing failures or damages (such as cracking) of the devices in the curing process.

3.8 Dividing / Breaking of PC boards

- (1) Abnormal and excessive mechanical stresses, such as bending or expanding force on the components on the printed circuit board, shall be kept minimum in the dividing / breaking.
- (2) Dividing / Breaking of the PC board shall be done carefully at moderate speed using a Jig boards from mechanical damages.

3.9 Long Term Storage

The Capacitors shall not be stored under severe conditions of high temperatures and high humidity. Store them under 40°C max. and 75%RH max. Use them within 6 months and check the solderability before use.