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MC10951
MC10L951
MC100951

Advance Information

12 X 12 EXPANDABLE MULTIPLIERS

The MC10951, 10L951 and 100951 are high-speed 12 x 12 multipliers that multiply two 12-bit 2's complement numbers and produce a 24-bit 2's complement output.

The M10951 series multiplies two 12-bit magnitude-only numbers and produces a 24-bit magnitude-only product. They multiply a 12-bit magnitude-only number together with a 12-bit 2's complement number and produce a 24-bit 2's complement output. Two 13-bit signed magnitude numbers (12-bits magnitude, 1-bit sign) can be multiplied to produce a 25-bit signed magnitude answer.

The MC10951 can be used as a stand alone 12-bit multiplier or as a building block for larger multiplier arrays.

The part performs the function: P = (X times Y) + M + K

Where K and M are 12-bit input fields used to add partial products in an array or to add a constant to the least significant part of the array product, or to add a constant in the stand alone mode.

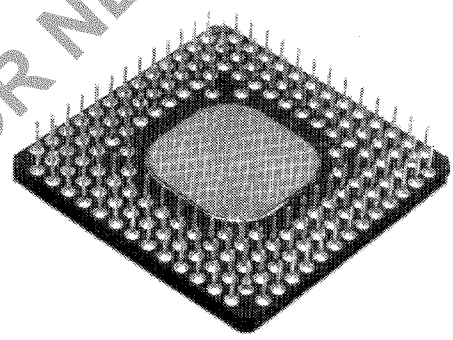
The algorithm used is an asynchronous sequential add technique. This algorithm eliminates the need for subtractions which simplifies the multiplier network.

- 12-Nanosecond Typical Multiply Time
- 12 x 12 Parallel Multiplication
- 13 x 13 Signed Magnitude Multiplication
- IEEE Format Floating Point Multiply with Shift Bit Correction
- 2's Complement, Unsigned Magnitude, Signed Magnitude or Mixed Mode Operation
- Two 12-Bit Input Expansion Ports for Summing Partial Products
- Control Inputs for Easy Expansion to Larger Multipliers
- Single-Chip Bipolar Technology
- Two 24-Bit Outputs, Latched for Product Outputs and Unlatched for Fast Partial Product Summation in Array
- Product Output Enable to Allow Wire-ORing of Outputs for Bus Operations
- Latched Inputs and Outputs with Complementary Clocks for Use In Pipelined Configurations
- Voltage Compensated, V_{EE} = −4.2 Vdc to −5.72 Vdc
- Interfaces with MECL 10K and 10KH with a 100K Version Also Available

ORDERING INFORMATION

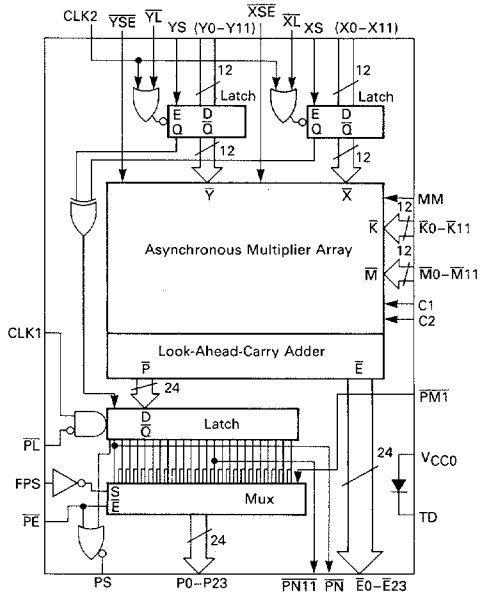
Part Number	Description
MC10951R	— 10K/10KH compatible V_{EE} = −5.2 Vdc ±5%
MC10L951R	— 10K/10KH compatible V_{EE} = −4.5 ±0.3 Vdc
MC100951R	— 100K compatible V_{EE} = −4.5 ±0.3 Vdc

MECL-LSI
12 X 12-BIT MULTIPLIERS



R SUFFIX
CASE 768-02

FIGURE 1 — LOGIC DIAGRAM



PRODUCT DESCRIPTION

The MC10951, MC10L951 and MC100951 are very high-speed multipliers which are implemented on Motorola's MCA2500ECL macrocell array. The parts are capable of multiplying two 13-bit (12-bits magnitude, 1-bit sign) signed-magnitude numbers and outputting a 25-bit signed-magnitude result. They also multiply two 12-bit 2's, complement numbers and output a 24-bit 2's complement result. The multipliers also handle mixed-mode operation. A 12-bit 2's complement number can be multiplied by a 12-bit magnitude-only number to produce a 24-bit 2's complement result.

The circuits perform IEEE standard floating-point operations on the chip. These include automatic shifting of the output for normalization, and shift-in, shift-out, for normalizing an expanded floating multiply result.

To make the chip faster for expanded multiples the chip has dual outputs, product outputs which are latched and high-speed expansion outputs which are used to output partial products in a multiplier array. It also has dual 12-bit partial product inputs to add in partial products in expanded arrays of multipliers.

The inputs and one of the 24-bit outputs are latched so the multiplier can perform in a pipeline configuration which allows a N-by-N multiply in the time needed for a single 12-by-12 multiply. This is extremely useful in high-speed digital signal processing applications.

The algorithm used is an asynchronous sequential add technique. This algorithm eliminates the need for subtractions which simplifies the multiplier network.

The circuits have a typical multiply time of 12 ns and a worst case limit of 21 ns.

The circuit is fully compatible with the other MECL logic families (10K, 10KH, MECL III, 10900, MCA2500ECL, MCA800ECL, MCA1200ECL, and MCA600ECL) and is specified around the dc specifications of the MECL 10KH family featuring a guaranteed dc noise margin of 150 mV over a ±5.0% power supply range and an ambient temperature range of 0 to 70°C. Although the array is voltage compensated over a range of V_{EE} of −4.2 to −5.72 volts, the dc parameters are specified with a V_{EE} of either −5.2 V ±5.0% (MC10951) or −4.5 volts ±0.30 volts (MC10L951) for reduced power consumption.

The multiplier is also offered with an ECL 100K option that features approximately constant output levels over temperatures. The MC100951 is specified (with standard ECL 100K specifications) with a guaranteed dc noise margin of 130 mV with ambient temperature variations of 0 to 70°C and a V_{EE} = −4.5 volts ±0.3 volts. The MC100951 is not fully compatible with the other MECL logic families over temperature due to differences in output level and input threshold (V_{BB}) temperature tracking.

DESCRIPTION OF SIGNALS

Signals	Symbol	Description
Clocks	CLK1 and CLK2	Separate master clocks for the input operands and the product allow either synchronous or asynchronous data flow through the multiplier. The X and Y operand latches are transparent when CLK2 is at a Logic "L." The product latch is transparent when CLK1 is at a Logic "H." For synchronous mode of operation (i.e., pipelined architectures), the two clocks are driven by the same source.
Control	C1 and C2	These two inputs determine the arithmetic format of the X and Y operands. When C1 is at a Logic "H" the Y operand is assumed to be a signed 2's complement 12-bit number, while a Logic "L" on C1 indicates the Y inputs are in unsigned-magnitude notation. The C2 and X inputs function similarly. The function of these two inputs also indicate to each multiplier chip its relative position in an array.
Sign Enables	XSE and YSE (Active Low)	Due to the nature of the multiplication algorithm, correction terms need to be added to obtain the correct 2's complement signed product. The sign bits of the X and Y 12-bit operands (i.e., X11 and Y11) are added if XSE and YSE are at a Logic "L."
Input Latch Enables	XL and YL (Active Low)	Data is passed through the latch when the respective latch enable and CLK2 is at a Logic "L." Data is latched when the respective latch enable or CLK2 is at a Logic "H."
Sign-Magnitude Bits	XS and YS	Multiplication of 13-bit signed-magnitude operands is accommodated by the inclusion of the XS and YS inputs. The result is a 25-bit product where the sign is the exclusive-OR of the two operand sign bits.
Input Buses	X0–X11 and Y0–Y11	Multiplicand and multiplier data enter the multiplier chip as 12-bit values. The inputs are designated with bit 11 as the most significant bit (MSB), and bit 0 as the least significant bit (LSB).
Expansion Input Buses	K0–K11 and M0–M11 (Active Low)	The expansion inputs are used to add the partial products generated in an array of multipliers. These 12-bit active low inputs connect directly into the internal asynchronous multiplier logic for fast partial product summation.

Signals	Symbol	Description
Partial Product Bit	PM1 (Active Low)	The partial product bit is used to input the most significant bit from the previous multiplier in a floating point multiplier array. Then a single bit normalization of the final product is necessary. The PM1 bit makes the upshift continuous across the multiplier array.
Floating Point Shift	FPS	A Logic "H" on this input will shift the final product towards the MSB by one bit (i.e. normalize). A Logic "L" cause the product output to be unaffected.
Product Latch Enable	PL (Active Low)	Data is passed through the latch when the latch enable is at a Logic "L" and CLK1 is at a Logic "H." The data is latched when the latch enable is at a Logic "H" or CLK1 is at a Logic "L." The product latch enable operates with the same polarity as the XL and YL controls, but the clocks, CLK1 and CLK2, are phased opposite. This simplifies synchronous operation and reduces sensitivity to timing skew and jitter.
Product Output Enable	PE (Active Low)	The product is disabled (i.e. forced to a Logic "L" on all bits) when the PE input is a a Logic "H." The product is present at the output when the PE input is at a Logic "L." This feature permits the use of wired-ORing and bus operation.
Product Output Bit (N)	PN (Active Low)	The PN bit is the inverted value of the most significant product bit as presented to the normalization logic. When connected to the FPS input in a floating point multiplier configuration, a single bit upshift occurs when the PN bit is at a Logic "H" (i.e., the most significant unnormalized product bit is at a Logic "L"). If the PN bit is at a Logic "L," the product is fully normalized already and no upshift is required.
Product Output Bit (11)	PN11 (Active Low)	The PN11 bit is the inverted value of the unnormalized product bit 11. In a floating point multiplier array, this bit is connected to the PM1 input.
Product Sign	PS	The product sign bit is the exclusive-OR of the XS and YS inputs, and is used for signed-magnitude multiplier operation. It is also latched and enabled by the PL and PE respectively.
Product Bus	P0–P23	The 24-bit product from the multiplication of the X and Y operands is output on the product bus.
Expansion Bus	E0–E23 (Active Low)	The expansion bus outputs the active low 24-bit partial product directly from the internal asynchronous multiplier logic. This approach provides fast partial product summation when used with the K and M input buses.
Mixed Mode Input	MM	Due to the nature of the algorithm, this bit must be set high when multiplying a 2's complement number by a magnitude-only number. This corrects the sign bit which would otherwise be incorrect when multiplying by a negative 2's complement number.
Temperature Measurement Diode	TMD	A test diode is connected to this pin for use in measuring the junction temperature of the multiplier IC. The cathode of the diode is connected to this pin and the anode is connected to V_{CC0} (K13, J13). By connecting the anode to a constant current source (i.e. 100K ohms to V_{EE}). The resulting pin voltage varies linearly with junction temperature.

DEVICE OPERATION

The multiplication matrix for the M10951 series is shown in Table 1. This matrix shows how the circuit calculates the product. The product is the binary sum of all the terms in the matrix.

The operation and expansion of the device is controlled by the C1, C2 and the MM pins. When C2 is at a logic low, the X input is in a magnitude form, when C2 is at a Logic "H" the X input is in a 2's complement form. The same is true for C1 and Y.

When multiplying a 2's complement number by a magnitude-only number, the MM or mixed mode pin must be set in a high state, otherwise it should remain in a low state.

For setting control pins for different modes, refer to Table 1.

TABLE 1 — MULTIPLICATION MATRIX

								$(C1 \oplus X4) \cdot Y11$
							$(C1 \oplus X5) \cdot Y11$	$X5 \cdot Y10$
						$(C1 \oplus X6) \cdot Y11$	$X6 \cdot Y10$	$X6 \cdot Y9$
	$C1 \cdot C2 \cdot \overline{Y11}$				$(C1 \oplus X7) \cdot Y11$	$X7 \cdot Y10$	$X7 \cdot Y9$	$X7 \cdot Y8$
	$\overline{X11} \cdot C1 \cdot C2$			$(C1 \oplus X8) \cdot Y11$	$X8 \cdot Y10$	$X8 \cdot Y9$	$X8 \cdot Y8$	$X8 \cdot Y7$
	$\overline{X11} \cdot C1 \cdot \overline{C2} \cdot Y11$		$(C1 \oplus X9) \cdot Y11$	$X9 \cdot Y10$	$X9 \cdot Y9$	$X9 \cdot Y8$	$X9 \cdot Y7$	$X9 \cdot Y6$
$+MM \cdot (C2 \cdot X11 + C1 \cdot Y11)$	$X11 \cdot \overline{C1} \cdot C2 \cdot \overline{Y11}$	$(C1 \oplus X10) \cdot Y11$	$X10 \cdot Y10$	$X10 \cdot Y9$	$X10 \cdot Y8$	$X10 \cdot Y7$	$X10 \cdot Y6$	$X10 \cdot Y5$
$C1 \cdot C2$	$X11 \cdot (C1 \overline{\oplus} C2) \cdot Y11$	$X11 \cdot (C2 \oplus Y10)$	$X11 \cdot (C2 \oplus Y9)$	$X11 \cdot (C2 \oplus Y8)$	$X11 \cdot (C2 \oplus Y7)$	$X11 \cdot (C2 \oplus Y6)$	$X11 \cdot (C2 \oplus Y5)$	$X11 \cdot (C2 \oplus Y4)$
P23	P22	P21	P20	P19	P18	P17	P16	P15

			XSE·X11											
			YSE·Y11											
			K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1	K0
			M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
			$(C1 \oplus X0) \cdot Y11$	X0·Y10	X0·Y9	X0·Y8	X0·Y7	X0·Y6	X0·Y5	X0·Y4	X0·Y3	X0·Y2	X0·Y1	X0·Y0
		$(C1 \oplus X1) \cdot Y11$	X1·Y10	X1·Y9	X1·Y8	X1·Y7	X1·Y6	X1·Y5	X1·Y4	X1·Y3	X1·Y2	X1·Y1	X1·Y0	
	$(C1 \oplus X2) \cdot Y11$	X2·Y10	X2·Y9	X2·Y8	X2·Y7	X2·Y6	X2·Y5	X2·Y4	X2·Y3	X2·Y2	X2·Y1	X2·Y0		
$(C1 \oplus X3) \cdot Y11$	X3·Y10	X3·Y9	X3·Y8	X3·Y7	X3·Y6	X3·Y5	X3·Y4	X3·Y3	X3·Y2	X3·Y1	X3·Y0			
X4·Y10	X4·Y9	X4·Y8	X4·Y7	X4·Y6	X4·Y5	X4·Y4	X4·Y3	X4·Y2	X4·Y1	X4·Y0				
X5·Y9	X5·Y8	X5·Y7	X5·Y6	X5·Y5	X5·Y4	X5·Y3	X5·Y2	X5·Y1	X5·Y0					
X6·Y8	X6·Y7	X6·Y6	X6·Y5	X6·Y4	X6·Y3	X6·Y2	X6·Y1	X6·Y0						
X7·Y7	X7·Y6	X7·Y5	X7·Y4	X7·Y3	X7·Y2	X7·Y1	X7·Y0							
X8·Y6	X8·Y5	X8·Y4	X8·Y3	X8·Y2	X8·Y1	X8·Y0								
X9·Y5	X9·Y4	X9·Y3	X9·Y2	X9·Y1	X9·Y0									
X10·Y4	X10·Y3	X10·Y2	X10·Y1	X10·Y0										
$X11 \cdot (C2 \oplus Y3)$	$X11 \cdot (C2 \oplus Y2)$	$X11 \cdot (C2 \oplus Y1)$	$X11 \cdot (C2 \oplus Y0)$											
P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

EXPANSION RULES

The M10951 series can be used in arrays to perform larger multiplications. An example of a 24-by-24 bit 2's complement multiplication which produces a 48-bit 2's complement result is shown in Figure 6. Any number of bits can be multiplied using multiple parts in an array. This is true for magnitude- and floating-point multiplication also.

For an M-bit by N-bit multiplier a M + N bit product is formed. The number of MC10951 needed can be calculated by the equation (M x N) / 144. For an example, a 24-by-24 bit multiply would need (24 x 24) / 144 = 4 pkgs.

The normal parallelogram structure consists of several stages, each multiplying 12-bits of multiplier times 12-bits of multiplicand, and adding the partial products.

The sign bits of the multiplicand and multiplier must be added to the product. As an example, a 12-by-24 bit multiplier would require the sign bit of the 12-bit word to be added to the least significant 12th bit of the product. Likewise, the sign bit of thhe 24-bit word is to be added to the least significant 24th bit of the product.

The X-sign bit and Y-sign bit must be added to the product with a binary weight (power of 2) equivalent to their respective binary weights. The control inputs C1, C2 and MM must be programmed correctly depending on the multiplier type and on the position of the MC10951 within the array.

1) For magnitude-arrays all control inputs are programmed low.
2) For 2's complement arrays the programming of the control inputs is dependant on the position of the multiplier within the array, and the terms required by the algorithm.

TABLE 2 — CONTROL INPUTS FOR DIFFERENT MODES OF MULTIPLICATION

X Input	Y Input	C1	C2	$\overline{XSE}$	$\overline{YSE}$	MM
12-Bit Magnitude	12-Bit Magnitude	L	L	H	H	L
12-Bit Magnitude	12-Bit 2's Comp #	H	L	H	L	H
12-Bit 2's Comp #	12-Bit Magnitude	L	H	L	H	H
12-Bit 2's Comp #	12-Bit 2's Comp #	H	H	H	H	L
13-Bit Sign-Magnitude	13-Bit Sign-Magnitude	L	L	H	H	L
13-Bit Floating Point	13-Bit Floating Point	L	L	H	H	L

TABLE 3 — CONTROL INPUTS FOR 2'S COMPLEMENT EXPANSION

X and Y Input to Multiplier	C1	C2	$\overline{XSE}$	$\overline{YSE}$	MM
No Sign Bits	0	0	1	1	0
X Sign Bit Only	0	1	0	1	0
Y Sign Bit Only	1	0	1	0	0
Both Sign Bits	1	1	1	1	0

TABLE 4 — PRODUCT LATCH CONTROL TABLE

$\overline{PL}$	CLK1	Latch Operation
Ø	L	Latched
L	H	Transparent
H	Ø	Latched

Ø = Don't Care

TABLE 5 — FLOATING POINT SHIFT AND OUTPUT ENABLE OPERATION

FPS	$\overline{PE}$	Product Output Mode	Product Outputs
L	L	Standard Output	P23 . . . . P1, P0
H	L	Floating Point Shift Output*	P22 . . . . P0, $\overline{PM1}$
X	H	Disabled	All Low

*By connecting $\overline{PN}$ to FPS automatic normalization of product output occurs.

FIGURE 2 — 25-BIT X 25-BIT SIGNED-MAGNITUDE FLOATING POINT MULTIPLY W/ 49-BIT NORMALIZED SIGNED-MAGNITUDE RESULT

Note: $\overline{PN}$ output is connected to FPS inputs for automatic normalization of floating point product.

For all parts in the array:
C1 = Low
C2 = Low
$\overline{XSE}$ = High
$\overline{YSE}$ = High
MM = Low

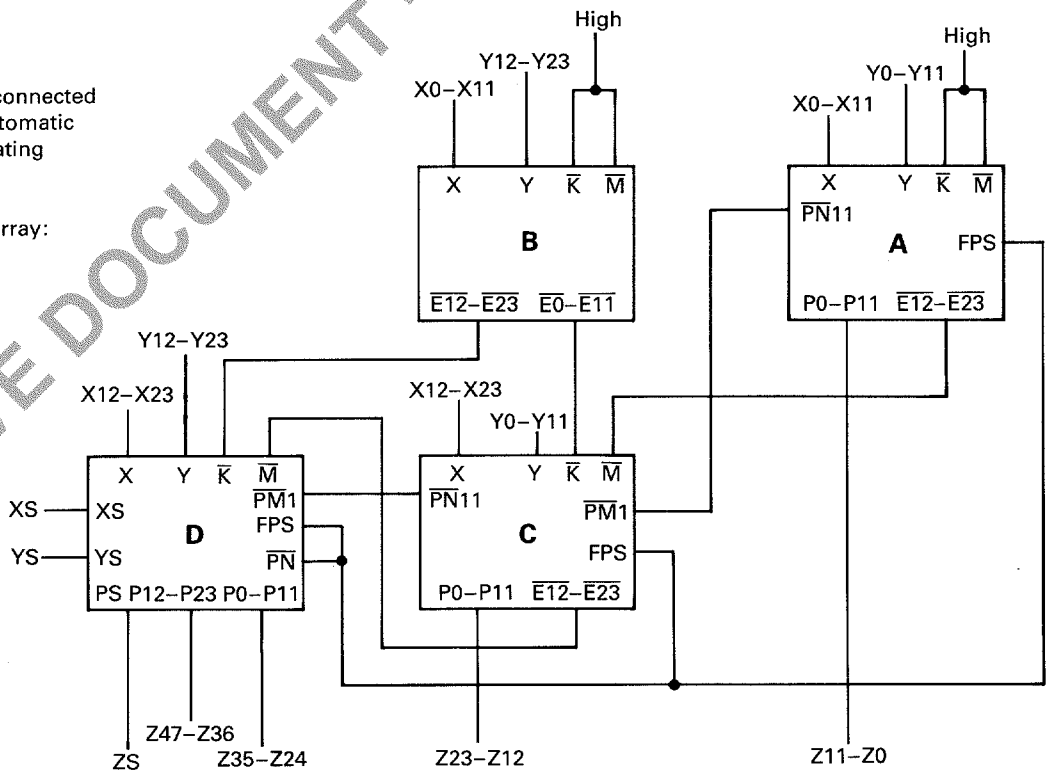


FIGURE 3 — 25-BIT X 25-BIT SIGNED-MAGNITUDE FLOATING POINT MULTIPLY W/ 25-BIT NORMALIZED SIGNED-MAGNITUDE RESULT 1/2 BIT (LSB) ERROR MAX

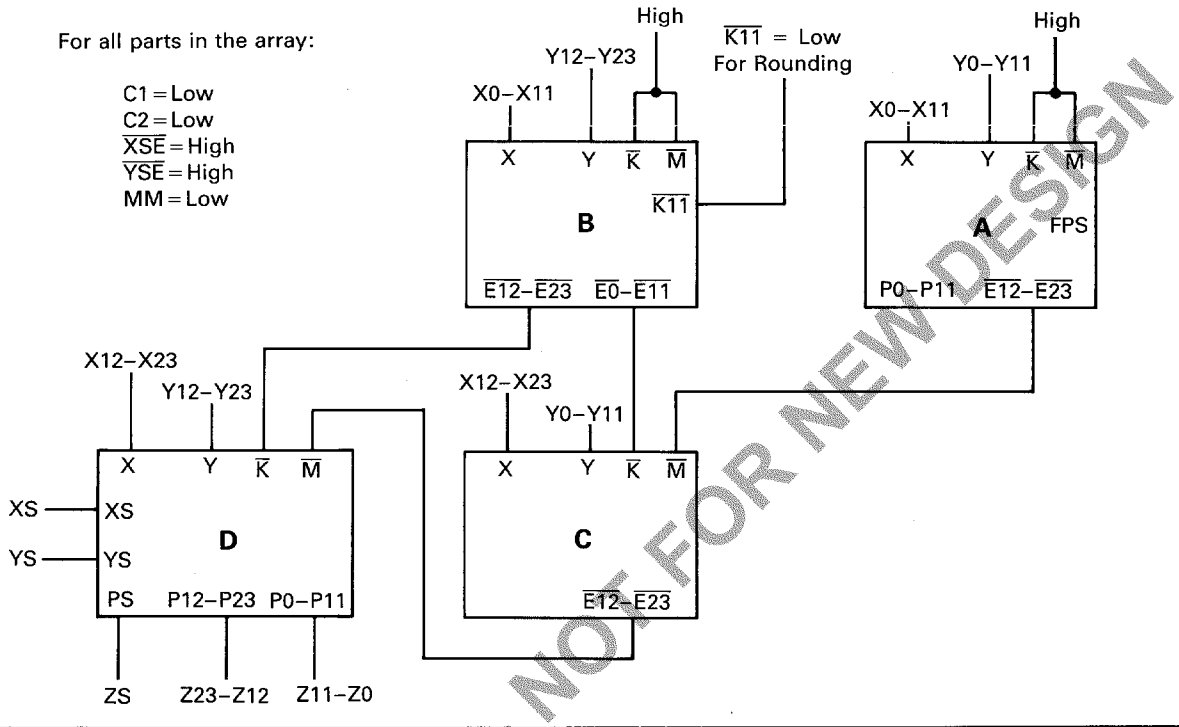


FIGURE 4 — 25-BIT X 25-BIT SIGNED-MAGNITUDE FLOATING POINT MULTIPLY W/ 25-BIT SIGNED-MAGNITUDE NORMALIZED FLOATING POINT RESULT 1-BIT (LSB) ERROR MAX

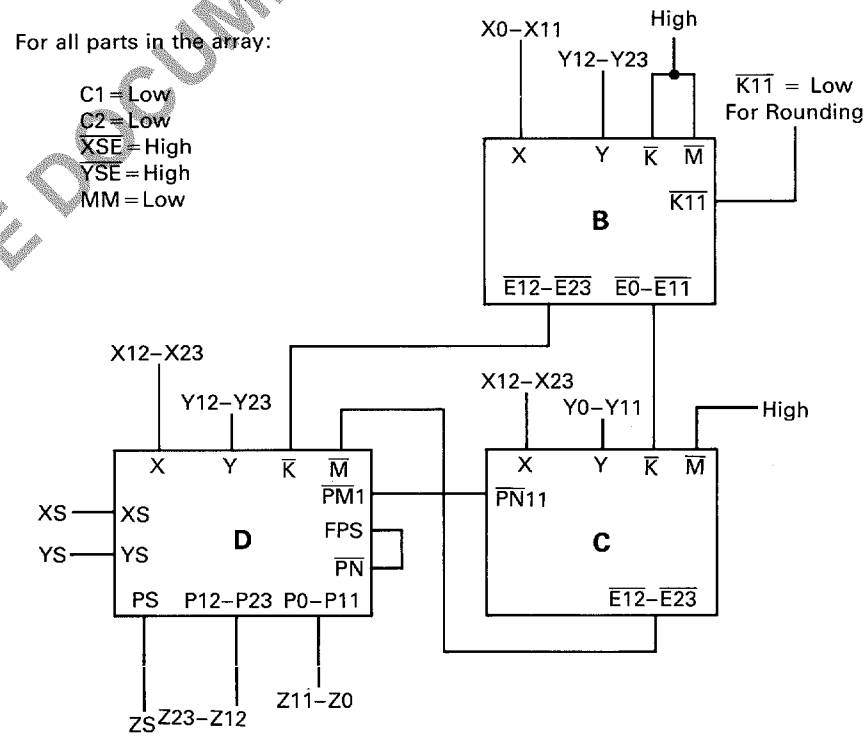


FIGURE 5 — 25-BIT X 25-BIT SIGNED MAGNITUDE MULTIPLY W/ 49-BIT SIGNED-MAGNITUDE RESULT

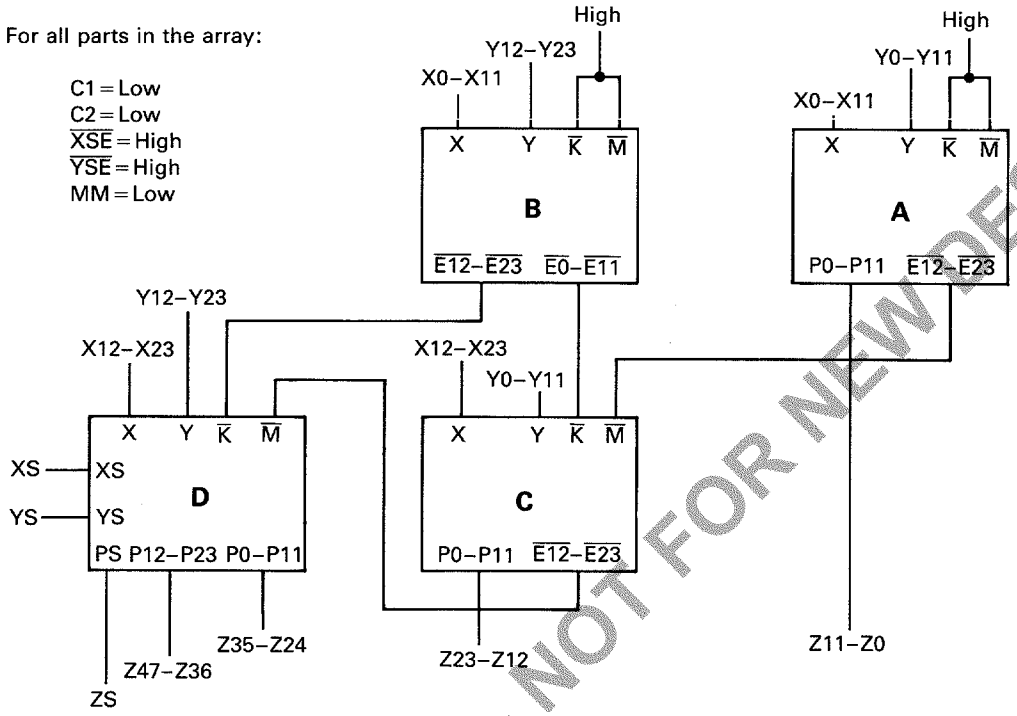


FIGURE 6 — 24-BIT X 24-BIT 2'S COMPLEMENT MULTIPLY W/ 48-BIT 2'S COMPLEMENT RESULT

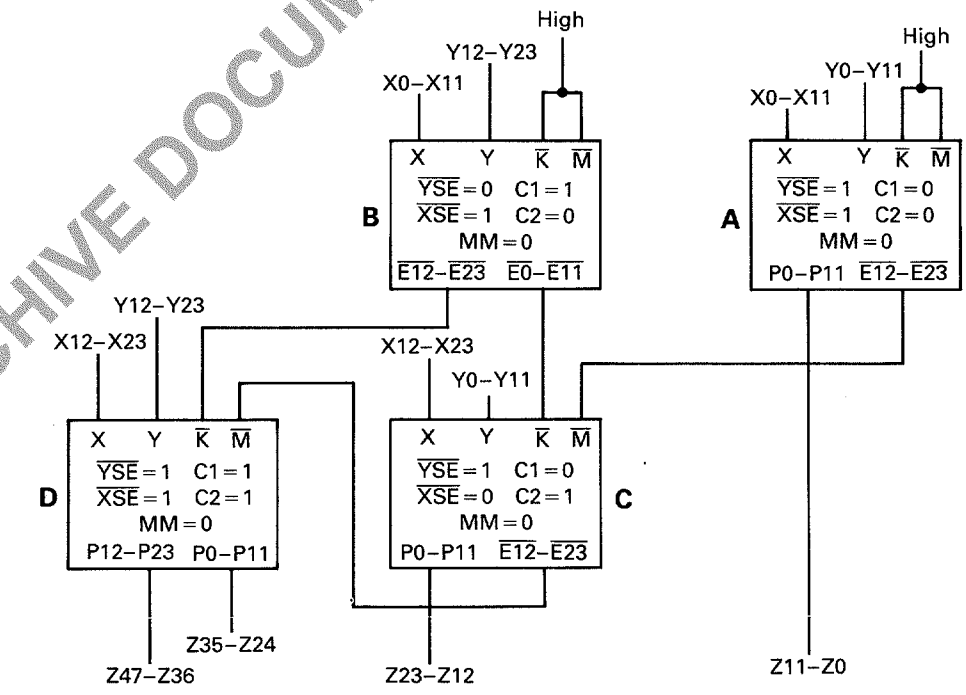


FIGURE 7 — 24-BIT X 24-BIT MIXED MODE MULTIPLICATION 24-BIT 2'S COMPLEMENT (Y), TIMES 24-BIT MAGNITUDE (X) W/ 48-BIT 2'S COMPLEMENT RESULT

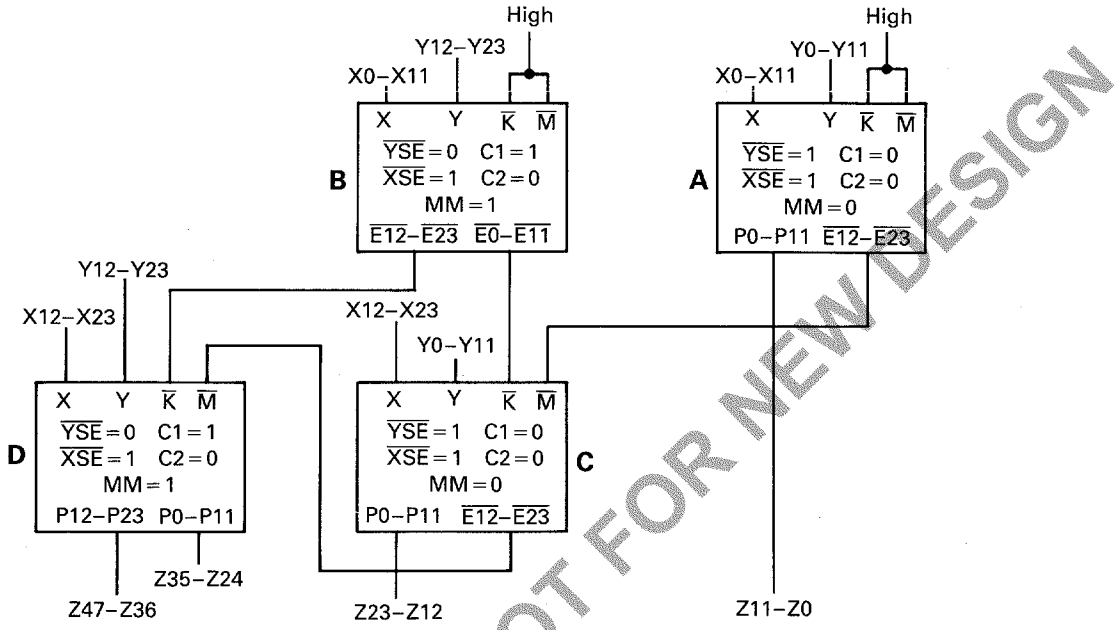


FIGURE 8 — 24-BIT X 24-BIT MULTIPLY PIPELINE ALLOWS CONTINUOUS MULTIPLYING FOR HIGH SPEED SIGNAL PROCESSING

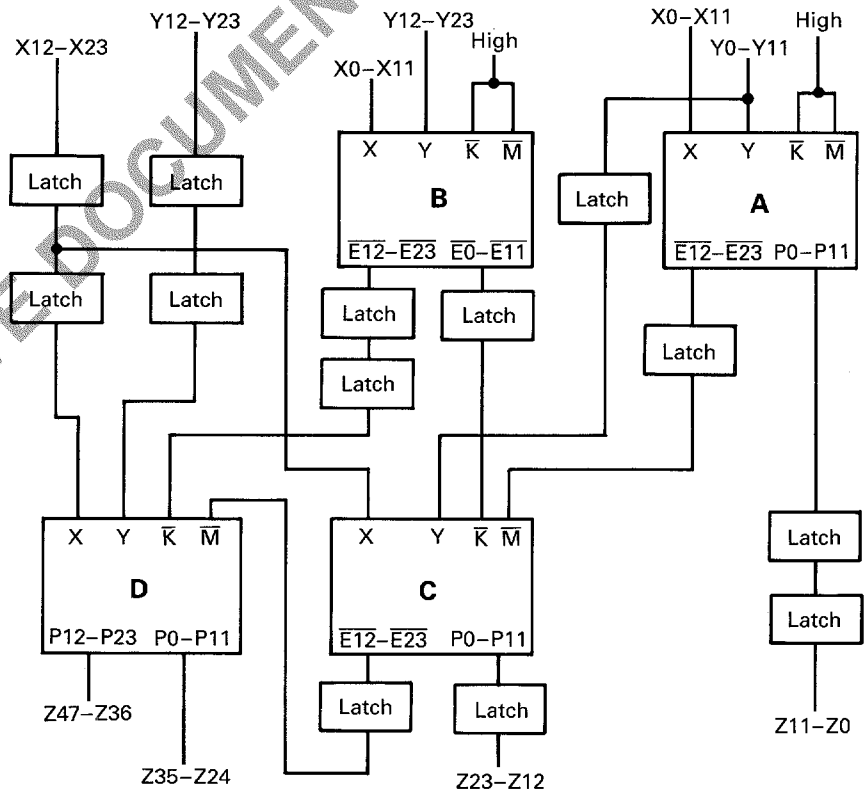


FIGURE 9 — 48-BIT X 48-BIT 2'S COMPLEMENT MULTIPLY W/ 96-BIT OUTPUT USING 16 MC10951 12 X 12 MULTIPLIERS

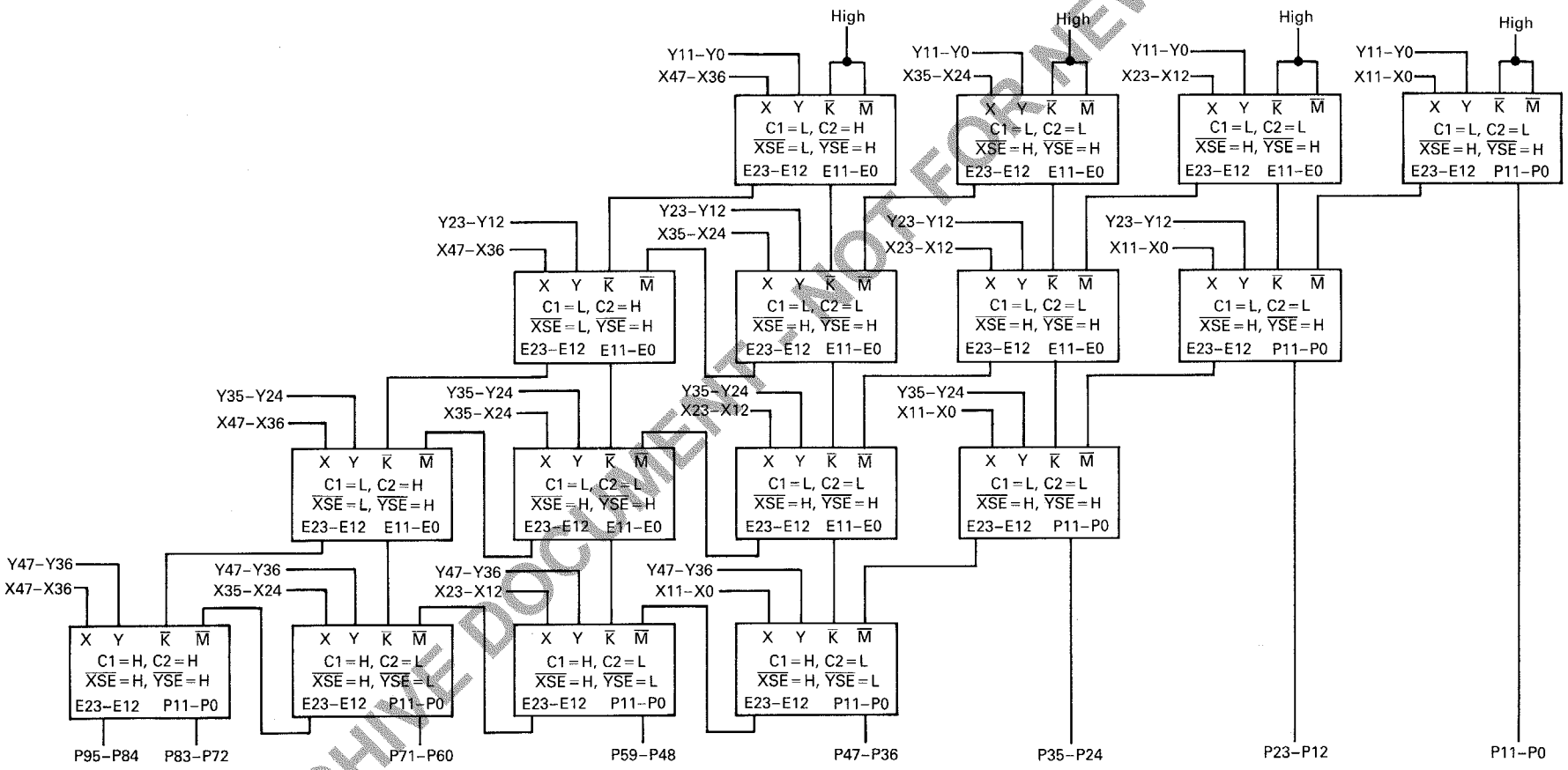


TABLE 6 — TYPICAL AND MAXIMUM TIMES FOR EXPANDED MULTIPLES

Size of Operands	Number of Parts	Multiply Time	
		Typ	Max
12 x 12	1	12	21.4
24 x 24	4	22.4	38.8
48 x 48	16	42	73.6

PIPELINE CONFIGURATION

Using a pipeline configuration a N x N multiply can be output each clock cycle. This is accomplished using complemented clocks CLK1 and CLK2. The input and output are latched on opposite edges, allowing the multiplier to begin a new multiply while still outputting the results of the previous multiply, also to change the inputs to the MC10951 after a multiply has begun without affecting the result of the multiply in progress. An example of a 24 x 24 pipeline multiply is shown in Figure 8. The latches are needed to store the partial operands and partial products so they reach the outputs during the same clock cycle. In this way a new 24 x 24 bit multiply begins each clock cycle. This pipeline would require 4 clocks to set up and then would output one 48-bit result after each subsequent clock. The time interval for one clock is the time it takes for one 12 x 12 multiply, or approximately 12 ns. This would enable roughly 84 million multiply per second.

ELECTRICAL CHARACTERISTICS

Consistent with industry LSI design requirements, the multiplier is voltage-compensated and available in either MECL 10K/10KH temperature tracking or ECL 100K temperature compensation. The circuit is voltage compensated over a range of V_{EE} values from −4.2 Vdc to −5.72 Vdc. Three options are available:

10K/10KH compatible at V_{EE} = −5.2 Vdc ± 5% — MC10951R

10K/10KH compatible at V_{EE} = −4.5 ± 0.3 Vdc — MC10L951R

100K compatible at V_{EE} = −4.5 ± 0.3 Vdc — MC100951R

LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

Characteristic	Symbol	Unit	Value
Supply Voltage (V_{CC} = 0)	V_{EE}	Vdc	−7.0 to 0
Input Voltage (V_{CC} = 0)	V_{in}	Vdc	0 to V_{EE}
Input Voltage Bus (V_{CC} = 0)	V_{in}	Vdc	0 to −2.0[1]
Output Source Current Continuous (50 Ω drive)	I_{out}	mAdc	30
Output Source Current Surge (50 Ω drive)[3]	I_{out}	mAdc	100
Output Source Current Continuous (25 Ω drive)	I_{out}	mAdc	60
Output Source Current Surge (25 Ω drive)[3]	I_{out}	mAdc	200
Storage Temperature	T_{stg}	°C	−55 to +150
Junction Temperature[2]	T_J	°C	165

1. Input voltage limit is V_{CC} to −2.0 volts when bus is used as an input and the output drivers are disabled.
2. Maximum T_J may be exceeded (≤ 250°C) for short periods of time (≤ 240 hours) without significant reduction in device life.
3. The surge current is defined as an output current between 30 mA and 100 mA for 50 Ω drive and between 60 mA and 200 mA for 25 Ω drive lasting for ≤ 10 μs and having a duty cycle of not more than 1%.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Unit	Value
Supply Voltage (V_{CC} = 0) For 4.5 V option	V_{EE}	Vdc	−4.5 ± 0.3
Supply Voltage (V_{CC} = 0) For 5.2 V 10KH/10K option	V_{EE}	Vdc	−5.2 ± 5%
Operating Temperature With Heat Sink and 750 lfm (ac and dc Specifications)	T_A	°C	0 to +70
Maximum Junction Temperature (Functional)	T_J	°C	130
Maximum Junction Temperature (For ac and dc Specifications)	T_J	°C	115
Maximum Clock Input Rise and Fall Times (20 to 80%)	t_r, t_f	ns	10

DC ELECTRICAL CHARACTERISTICS

Input Forcing Voltages	Parameter	MECL 10K/10KH Compatible Spec Limits(1) Ambient Temperature 0°C	25°C	70°C	ECL 100K Compatible Spec Limits(1) Ambient Temperature 0 to 70°C	Unit
V_{IH} Max and V_{IL} Min	V_{OH} Max	−0.840	−0.810	−0.740	−0.880[4]	Vdc
	V_{OH} Min	−1.000	−0.960	−0.900	−1.025	Vdc
	V_{OL} Max	−1.650	−1.650	−1.620	−1.620	Vdc
	V_{OL} Max[2]	−1.950	−1.950	−1.950	−1.950	
	V_{OL} Min	−1.950	−1.950	−1.950	−1.810	Vdc
	V_{OL} Min[2]	−2.020	−2.020	−2.020	−2.020	
V_{IHA} Min and V_{ILA} Max	V_{OHA} Min	−1.020	−0.980	−0.920	−1.035	Vdc
	V_{OLA} Max	−1.630	−1.630	−1.600	−1.610	Vdc
	V_{OLA} Max[2]	−1.950	−1.950	−1.950	−1.950	Vdc
V_{IH} Max	I_{INH} Max[3]	25	25	25	25	μA
	I_{INH} Max[5]	150	150	150	150	
V_{IL} Min	I_{INL} Min[6]	0.5	0.5	0.5	0.5	μA
Input Voltage Values	V_{IH} Max	−0.840	−0.810	−0.730	−0.880	Vdc
	V_{IL} Min	−1.950	−1.950	−1.950	−1.810	Vdc
	V_{IHA} Min	−1.170	−1.130	−1.070	−1.165	Vdc
	V_{ILA} Max	−1.480	−1.480	−1.450	−1.475	Vdc
Power Supply Drain Current	I_{EE} Max	1907	1987	1987	1987	mAdc

NOTES:
1. DC test limits are specified after thermal equilibrium has been established with the MCA device having an attached heat sink and a transverse air flow of 750 lfpm. V_{EE} = −4.5 V ± 0.3 V. V_{EE} = −5.2 V ± 5% for the 10KH/10K 5.2 V option. All outputs are loaded with 50 Ω to −2.0 V except the 25 Ω drivers which are loaded with 25 Ω to −2.0 V.
2. These voltage limits are for the driver output of macros with V_{OL} in the cutoff mode.
3. Per input fan-in.
4. For outputs connected to Output macro X261, 25 ohm driver, V_{OH} Max = −0.740 Vdc.
5. For input pulldown (≈ 50 kΩ).
6. Measured because input pulldown is always used.

ELECTRICAL CHARACTERISTICS

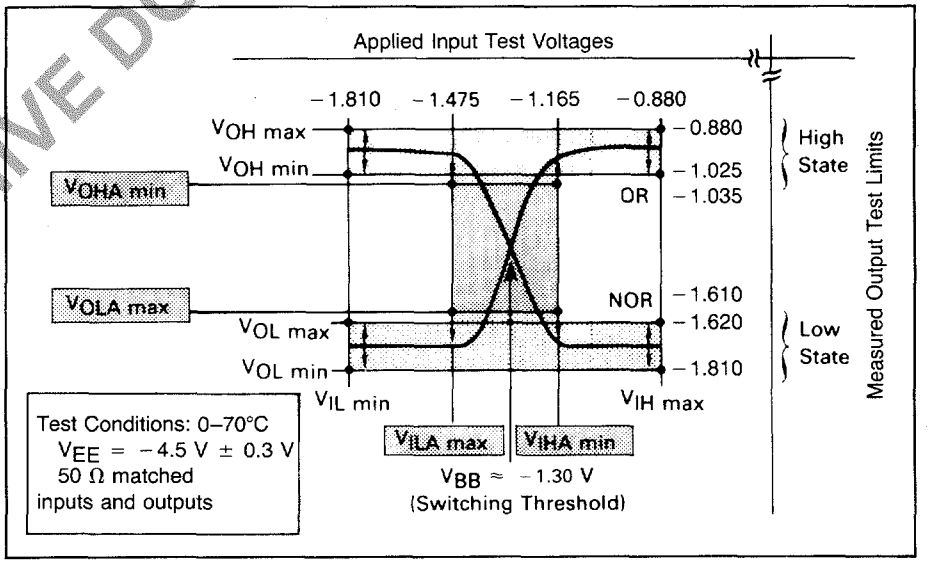


FIGURE 10 — MECL TRANSFER CURVES (ECL 100K OPTION) AND SPECIFICATION TEST POINTS

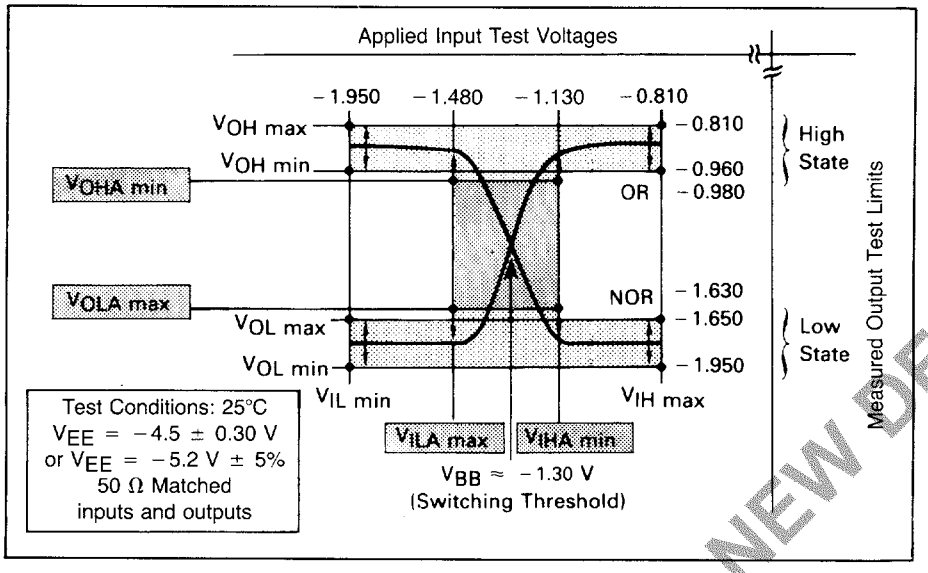


FIGURE 11 — MECL TRANSFER CURVES (MECL 10K/10KH OPTION) AND SPECIFICATION TEST POINTS

It is not necessary to measure all points on the transfer curves. To guarantee correct operation it is sufficient to measure two sets of min/max logic level parameters.

The first set is obtained by applying test voltages, $V_{IL\ min}$ and $V_{IH\ max}$ (sequentially) to the gate inputs, and measuring the output level to make sure they are between $V_{OL\ max}$ and $V_{OL\ min}$, and $V_{OH\ max}$ and $V_{OH\ min}$ specifications.

The second set of logic level parameters relates to the switching thresholds. This set of data is distinguished by an "A" in symbol subscripts. A test voltage, $V_{ILA\ max}$, is applied to the inputs and the outputs are measured to see that they are above the $V_{OHA\ min}$ and below the $V_{OLA\ max}$ levels, respectively. Similar checks are made using the test input voltage $V_{IHA\ min}$.

The result of these specifications insure that:

a) The switching threshold ($\approx V_{BB}$) falls within the darkest rectangle; i.e., switching does not begin outside this rectangle;

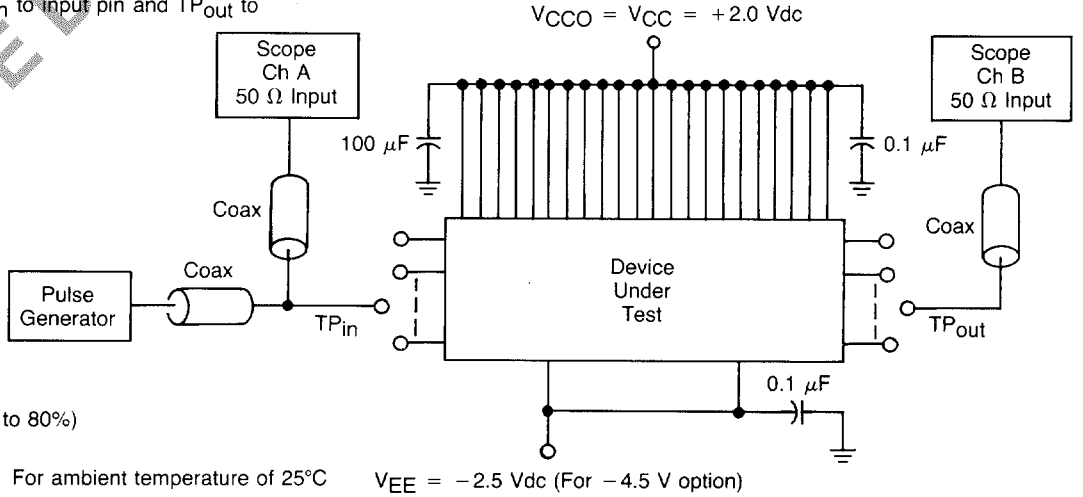
b) Quiescent logic levels fall in the lightest shaded ranges;

c) Noise immunity guideline is met.

SWITCHING CHARACTERISTICS OVER OPERATING VOLTAGE AND TEMPERATURE RANGE

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1 4 inch from TP_{in} to input pin and TP_{out} to output pin.



INPUT PULSE

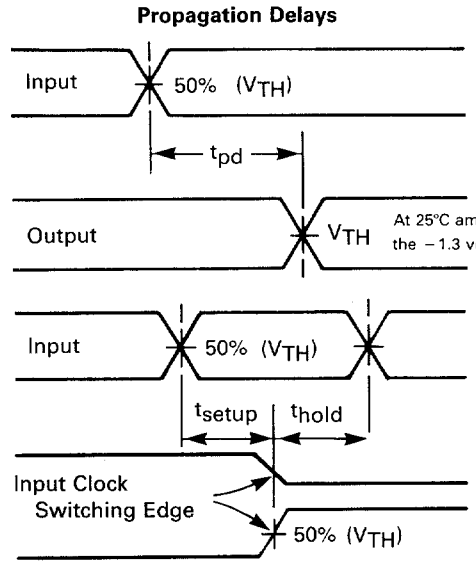
$t_r = t_f = 1.0$ ns (20 to 80%)

$V_{OH} = +1.10$ V

$V_{OL} = +0.30$ V

For ambient temperature of 25°C

FIGURE 12 — SWITCHING TEST CIRCUIT



Propagation delays are measured from the 50% point of the input rising or falling edge to the V_{TH} point of the output rising or falling edge. V_{TH} is the V_{BB} threshold voltage.

TEST PROCEDURE:
a) Establish setup time with long t_{hold}.
b) Keeping the leading edge of the input constant (t_{setup}) vary the trailing edge of the input to determine t_{hold}.

FIGURE 13 — SWITCHING WAVEFORMS

Table 7 defines the timing characteristics of the MC10951 over operating voltage and temperature ranges. Worst-Case Setup and Hold and Propagation Delays are guaranteed for V_{EE} = −5.2 Volts ± 5% and a T_{Jmax} = 115°C. The maximum recommended operating junction temperature is +130°C.

AC limits are based on several performance factors as described in Motorola's Preliminary Design Manual for the MCA2500ECL Macrocell Array. Factors include worst-case delays due to Macro selections, Fan-Out, Metal Lengths, Wire-OR, and Input Follower options. AC measurements are performed on each device to assure process integrity.

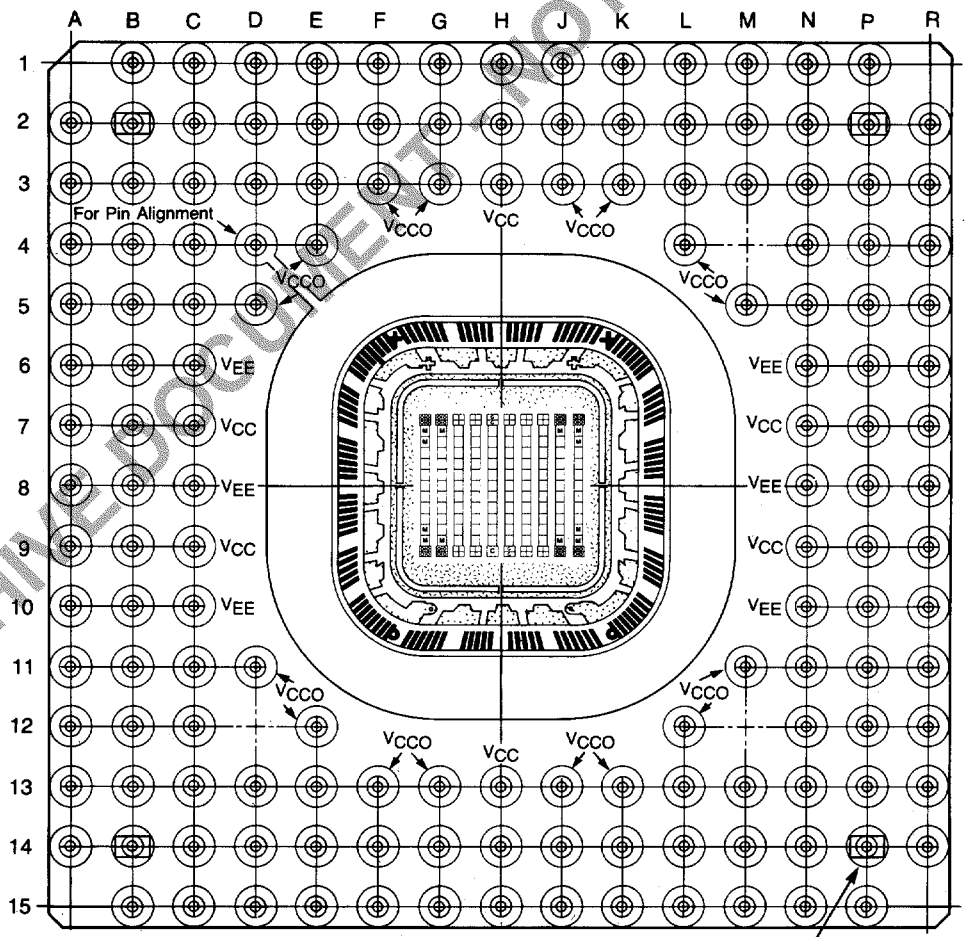
TABLE 7 — M10951 SERIES AC SPECIFICATIONS

Input	Output	Prop Delay Typ (ns)	Prop Delay Max (ns)	Setup and Hold Times (ns)		
X and Y Transparent Mode	P0–P11	—	13.8	For Input Latches (CLK2)		
	P12–P23	—	19.1		Setup	Hold
	E0–E11	—	12.3	X, Y	0.450	0.400
	E12–E23	—	16	X5, Y5	0.450	0.400
	PN11	—	14			
	PN	—	17.3			
	P5	—	4.0			
CLK2	P0–P11	10.1	16.2	For Product Latch (CLK1)		
	P12–P23	12	21.4		Setup	Hold
	E0–E11	9.1	14.6	X & Y Transparent Mode	16.75	−0.7
	E12–E23	11.8	18.9			
	PN11	9.7	15.5			
	PN	11.6	18.6			
	P5	3.3	5.3			
CLK1	P0–P23	2.8	4.5	X5 & Y5 Transparent Mode	4.52	−0.67
	PN11	2.5	4.0			
	PN	2.55	4.1			
	P5	2.5	4.0			
K	P0–P11	7.6	12.2	X & Y From CLK2	18.10	−1.05
	P12–P23	10.1	16.2			
	E0–E11	6.4	10.3			
	E12–E23	8.5	13.7			
M	P0–P11	5.8	9.3	X5 & Y5 From CLK2	5.77	−0.98
	P12–P23	7.0	11.2			
	E0–E11	4.7	7.5			
	E12–E23	5.4	8.7			
FPS	P0–P23	2.35	3.8	K	14.05	−0.50
PM1	P0	0.9	1.4			
PE	P0–P23	2.19	3.5	M	9.05	−0.35

TABLE 8 — INPUT/OUTPUT PIN REFERENCE

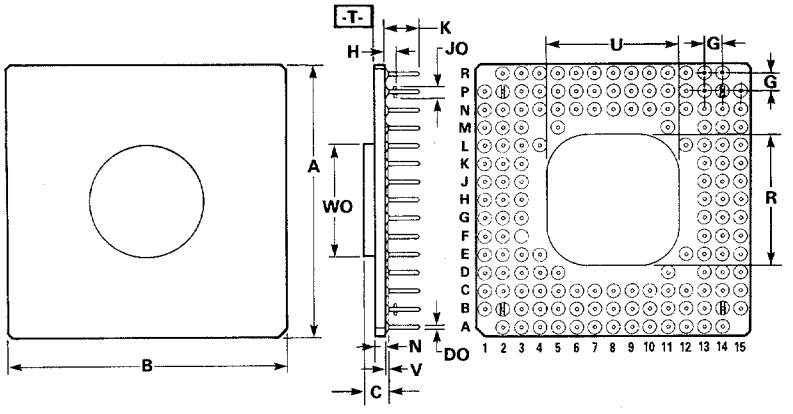
Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
P0	M13	P23	D1	$\overline{E7}$	P2	Y6	A13	$\overline{M2}$	R13
P1	L13	X0	G15	$\overline{E8}$	P1	Y7	B12	$\overline{M3}$	R10
P2	M15	X1	H15	$\overline{E9}$	M3	Y8	P8	$\overline{M4}$	R9
P3	K14	X2	A6	$\overline{E10}$	L3	Y9	A8	$\overline{M5}$	R7
P4	K15	X3	B8	$\overline{E11}$	L1	Y10	C12	$\overline{M6}$	P5
P5	N15	X4	B7	$\overline{E12}$	M2	Y11	C14	$\overline{M7}$	P3
P6	L15	X5	A7	$\overline{E13}$	N2	YS	E14	$\overline{M8}$	P4
P7	J15	X6	B14	$\overline{E14}$	K1	$\overline{YSE}$	B11	$\overline{M9}$	R2
P8	J14	X7	A14	$\overline{E15}$	F2	$\overline{YL}$	A11	$\overline{M10}$	R3
P9	N14	X8	F14	$\overline{E16}$	G1	$\overline{K0}$	R12	$\overline{M11}$	R4
P10	L2	X9	D15	$\overline{E17}$	N1	$\overline{K1}$	P12	CLK1	A4
P11	M1	X10	A12	$\overline{E18}$	D2	$\overline{K2}$	N11	CLK2	A3
P12	H1	X11	C11	$\overline{E19}$	D3	$\overline{K3}$	R11	C1	B15
P13	H2	XS	C15	$\overline{E20}$	F1	$\overline{K4}$	P9	C2	C13
P14	J1	$\overline{XSE}$	A9	$\overline{E21}$	C3	$\overline{K5}$	R8	$\overline{PM1}$	M14
P15	G2	$\overline{XL}$	B13	$\overline{E22}$	A2	$\overline{K6}$	P6	$\overline{PN11}$	K2
P16	E3	$\overline{E0}$	P14	$\overline{E23}$	D14	$\overline{K7}$	P7	$\overline{PN}$	E15
P17	C1	$\overline{E1}$	P15	Y0	F15	$\overline{K8}$	N5	$\overline{PE}$	R6
P18	B2	$\overline{E2}$	N13	Y1	G14	$\overline{K9}$	B3	FPS	P11
P19	C2	$\overline{E3}$	L14	Y2	A10	$\overline{K10}$	B6	$\overline{PL}$	A5
P20	B1	$\overline{E4}$	R14	Y3	B10	$\overline{K11}$	P10	PS	J2
P21	E1	$\overline{E5}$	N4	Y4	D13	$\overline{M0}$	N12	MM	B9
P22	E2	$\overline{E6}$	N3	Y5	E13	$\overline{M1}$	P13	TMD	H14

FIGURE 14 — PIN LOCATION FOR 149 PIN GRID ARRAY PACKAGE



NOTES: V_{CC} pins — H3, H13, C7, N7, C9, N9
V_{EE} pins — C8, N8, C6, N6, C10, N10
V_{CCO} pins — F3, G3, J3, K3, E4, L4, D5, M5, D11, M11, E12, L12, F13, G13, J13, K13
Pin D4 is connected to the seal ring, but isolated electrically.

FIGURE 15 — PACKAGE DIMENSIONS



NOTES:
1. A AND B ARE DATUMS AND -T- IS A DATUM PLANE.
2. POSITIONAL TOLERANCE FOR LEADS: ⌖ | ϕ 0.13 (0.005) Ⓜ | T | A Ⓢ | B Ⓢ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	37.85	38.60	1.490	1.520
B	37.85	38.60	1.490	1.520
C	2.64	3.55	0.104	0.140
D	0.43	0.48	0.017	0.019
G	2.54 BSC		0.100 BSC	
H	1.14	1.39	0.045	0.055
J	1.14	1.39	0.045	0.055
K	4.19	4.69	0.165	0.185
N	1.37	1.67	0.054	0.066
R	17.65	17.90	0.695	0.705
U	17.65	17.90	0.695	0.705
V	0.277	0.340	0.0109	0.0134
W	15.62	16.12	0.615	0.635

CASE 768-03

FIGURE 16 — THERMAL CHARACTERISTICS (TYPICAL)
(with prototype heat sink or equivalent)

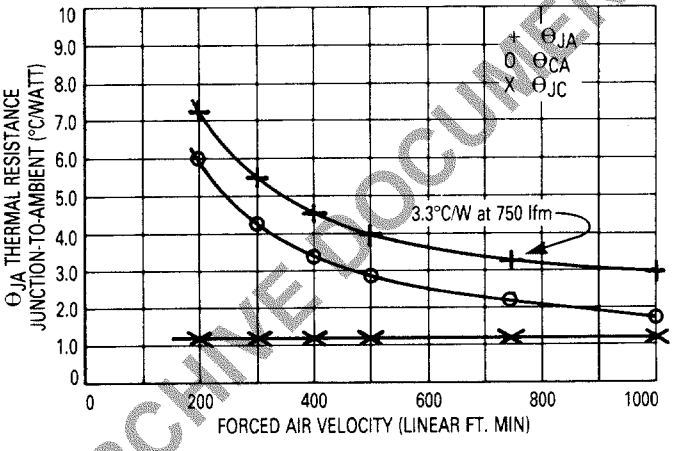


FIGURE 17 — CONSTRUCTION PROFILE

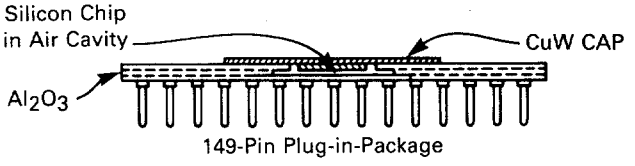
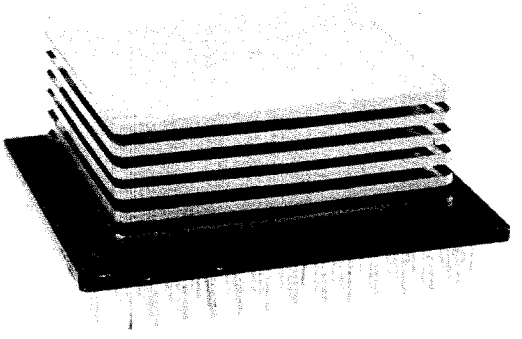


FIGURE 18 — PROTOTYPE HEAT SINK



Prototype Heat Sink — 6 plates 1.25 X 1.25 X 0.04 inches spaced 0.0625 inch apart, mounted on 0.5 inch diameter spindle — omnidirectional.
Equivalent Heat Sink — Thermalloy #16506. Horizontal fins. 7 round plates 1.25 inch in diameter by 0.7 inch high.

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