

T6A41

COLUMN DRIVER LSI FOR A DOT MATRIX LCD

The T6A41 is a column driver with 64-output channels for a dot matrix LCD.

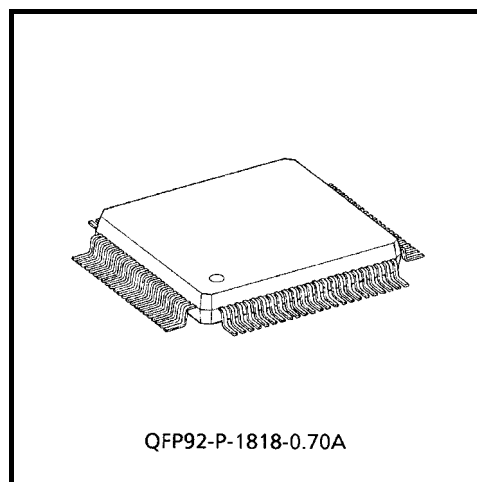
The T6A41 realizes low power LCD systems using the CMOS Si-Gate process.

The T6A41 has two bi-directional data Input / Output pins and three types of data flow (pin program):

(1) $O_1 \rightarrow O_{64}$, (2) $O_{64} \rightarrow O_1$, (3) $O_1 \rightarrow O_{32}$, $O_{64} \rightarrow O_{33}$.

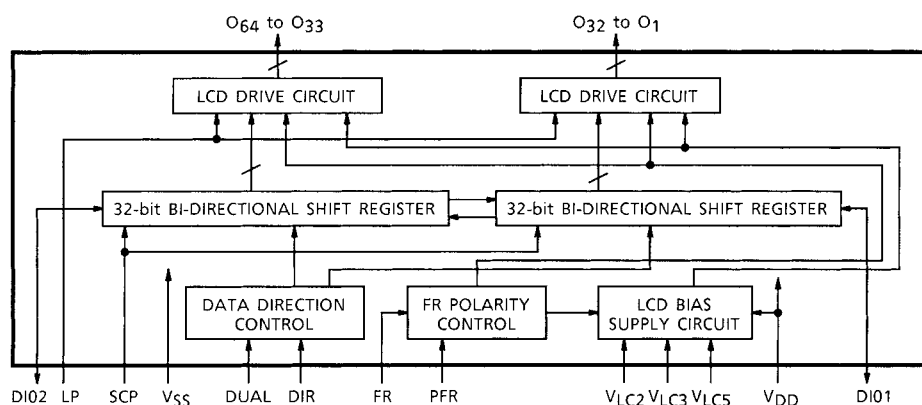
Features

- 64-output column driver
- Three types of data flow:
 - (1) $O_1 \rightarrow O_{64}$
 - (2) $O_{64} \rightarrow O_1$
 - (3) $O_1 \rightarrow O_{32}$, $O_{64} \rightarrow O_{33}$
- High speed operation
- Low power consumption
- Power supply: $5\text{ V} \pm 10\%$
- 92-pin plastic flat package

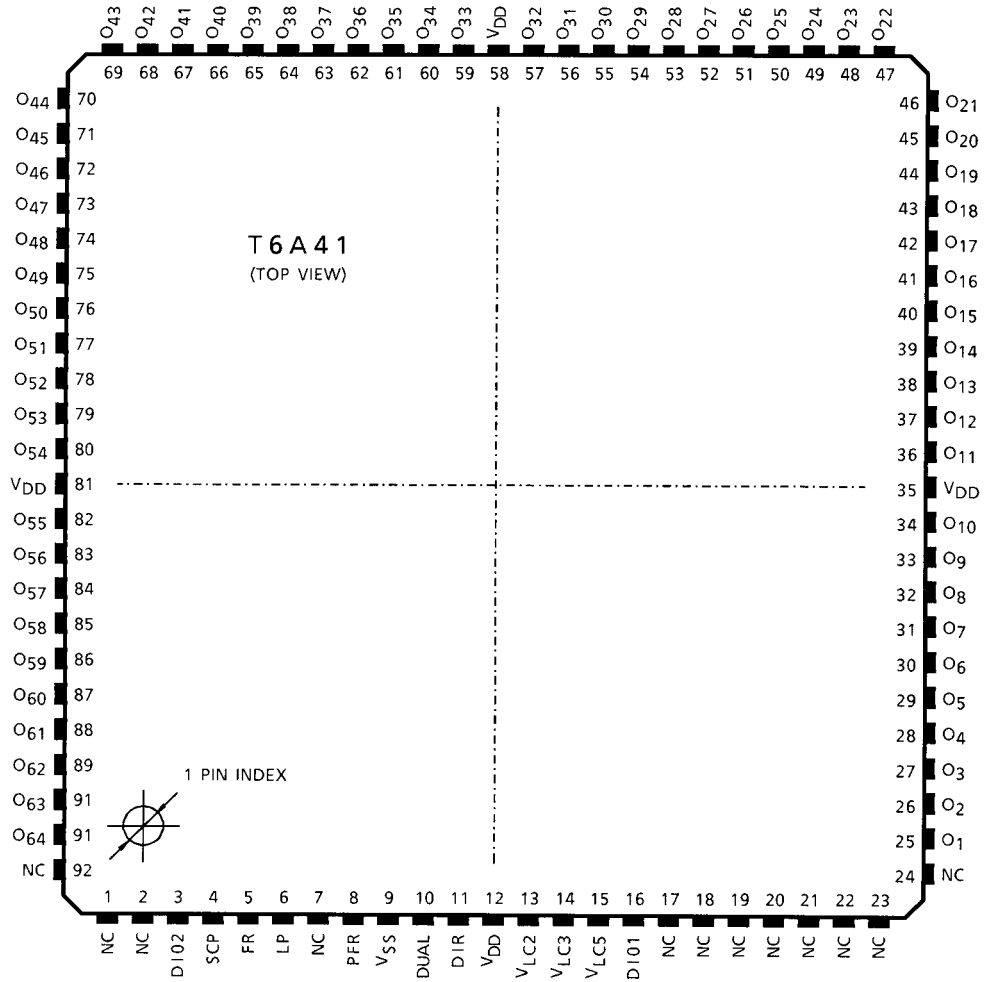


Weight: 1.4 g (typ.)

Block Diagram



Pin Assignment

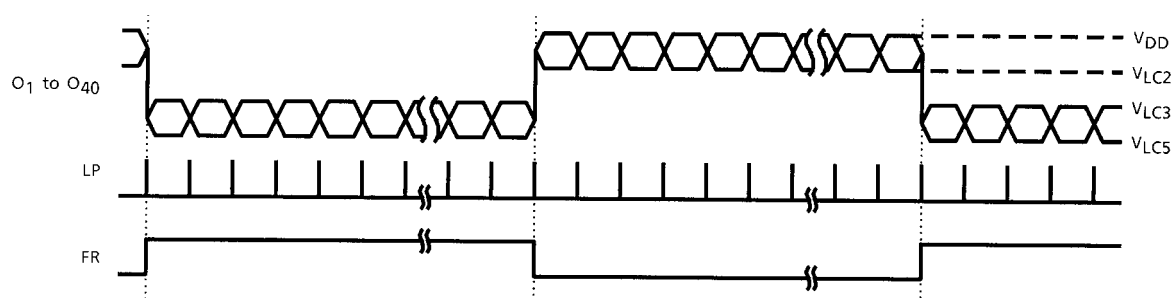


Pin Functions

Pin Name	I / O	Functions	Level
O ₁ to O ₆₄	Output	LCD drive signal output	V _{DD} to V _{LC5}
DIO1 , DIO2	I / O	Bi-directional data input and output	V _{DD} to V _{SS}
SCP	Input	(Shift Clock Pulse) Shift clock pulse input	
FR	Input	(Frame) Frame signal input	
LP	Input	(Latch Pulse) Latch pulse signal input	
DUAL	Input	(Dual Mode) Selects dual mode or single mode data flow.	
DIR	Input	(Direction) Selects input data flow direction.	
PFR	Input	(Polarity of Frame) Usually connected to V _{SS}	
V _{LC2}	—	Power supply for LCD drive	—
V _{LC3}	—	Power supply for LCD drive	
V _{LC5}	—	Power supply for LCD drive	
V _{DD}	—	Power supply (5 V)	
V _{SS}	—	Power supply (0 V)	

DUAL	DIR	DIO1	DIO21	Data Direction
L	L	OUT	IN	O ₆₄ → O ₁
L	H	IN	OUT	O ₁ → O ₆₄
H	L	—	—	Do not use
H	H	IN	IN	O ₁ → O ₃₂ , O ₆₄ → O ₃₃

Timing Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage (1)	V _{DD} (Note 1)	-0.3 to 7.0	V
Supply Voltage (2)	V _{LC2} , V _{LC3} , V _{LC5} (Note1, 2)	-0.3 to 7.0	V
Input Voltage	V _{IN} (Note 1)	-0.3 to V _{DD} + 0.3	V
Operating Temperature	T _{opr}	-20 to 75	°C
Storage Temperature	T _{stg}	-55 to 125	°C

Note 1: Referenced to V_{SS} = 0 V

Note 2: Ensure that the following condition is always maintained.

$$V_{DD} \geq V_{LC2} \geq V_{LC3} \geq V_{LC5}$$

Electrical Characteristics

DC Characteristics

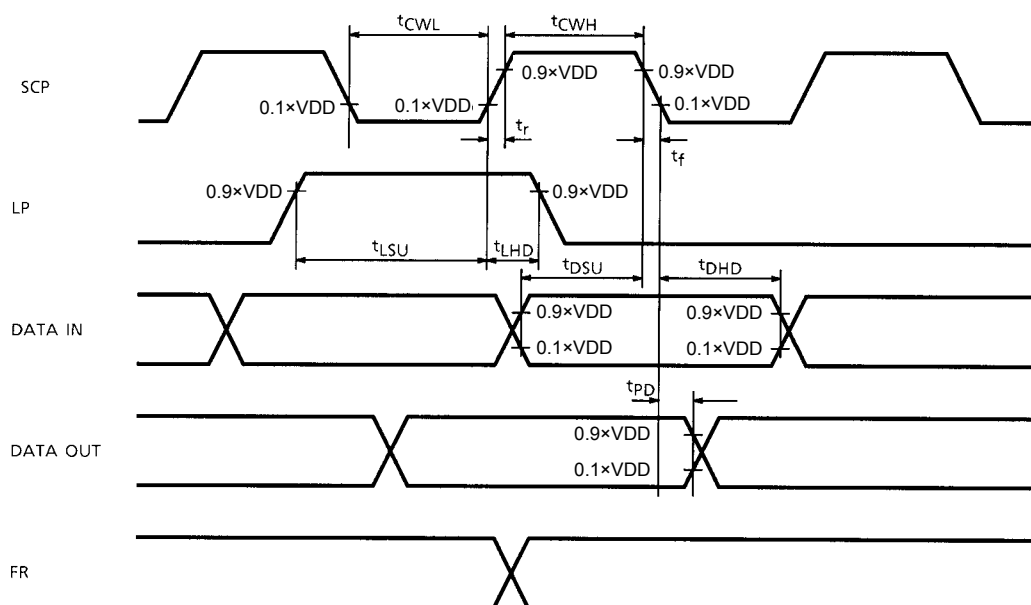
Test Conditions

(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%,
V_{LC5} = 0 V, Ta = -20 to 75°C)

Item		Symbol	Test Circuit	Test Conditions	Min	Typ.	Max	Unit	Pin Name	
Operating Voltage (1)		V _{DD}	—	—	4.5	5.0	5.5	V	V _{DD}	
Operating Voltage (2)		V _{LC5}	—	—	0	—	V _{DD} -3.0	V	V _{LC5}	
Input Voltage	H Level	V _{IH}	—	—	V _{DD} -1.0	—	V _{DD}	V	(*)	
	L Level	V _{IL}	—	—	0	—	1.0	V	(*)	
Output Voltage	H Level	V _{OH}	—	I _{OH} = -0.4 mA	V _{DD} -0.4	—	V _{DD}	V	DIO1, DIO2	
	L Level	V _{OL}	—	I _{Oh} = 0.4 mA	0	—	0.4	V	DIO1, DIO2	
Output Resistance		R _{COL}	—	I _d = ±50 μA	—	—	30	kΩ	O ₁ to O ₆₄	
Operating Frequency		f _{scp}	—	T _a = -20 to 75°C	—	—	400	kHz	SCP	
Current Consumption		I _{SS}	—	V _{DD} = 5.0 V V _{LC2} = 3.0 V V _{LC3} = 2.0 V V _{LC5} = 0.0 V f _{FR} = 39 Hz f _{SCP} = 250 kHz O ₁ to O ₈₀ : No Load	Binary Data Input	—	—	1.0	mA	V _{SS}
				Input Data : LOW Constant	—	—	0.4	mA		

*: DIO1, DIO2, SCP, FR, LP, PFR, DUAL, DIR

AC Characteristics



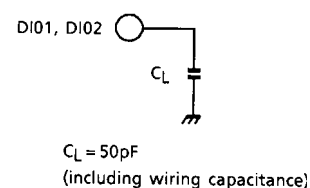
Test Conditions

(Unless Otherwise Noted, $V_{SS} = 0\text{ V}$, $V_{DD} = 5\text{ V} \pm 10\%$, $V_{LC5} = 0\text{ V}$, $T_a = -20\text{ to }75^\circ\text{C}$)

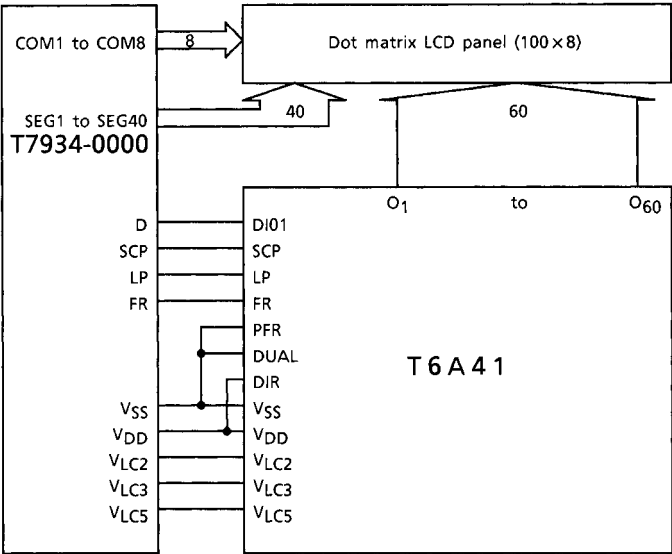
Item	Symbol	Min	Max	Unit
Operating Frequency	f_{SCP}	—	400	kHz
SCP Pulse Width	t_{CWL} , t_{CWH}	800	—	ns
SCP Rise / Fall Time	t_r , t_f	—	200	ns
LP Set-up Time	t_{LSU}	500	—	ns
LP Hold Time	t_{LHD}	—	10	ns
Data Set-up Time	t_{DSU}	300	—	ns
Data Hold Time	t_{DHD}	300	—	ns
Output Data Delay Time	t_{PD} (Note)	—	500	ns

Note: With load circuit connected

Load Circuit

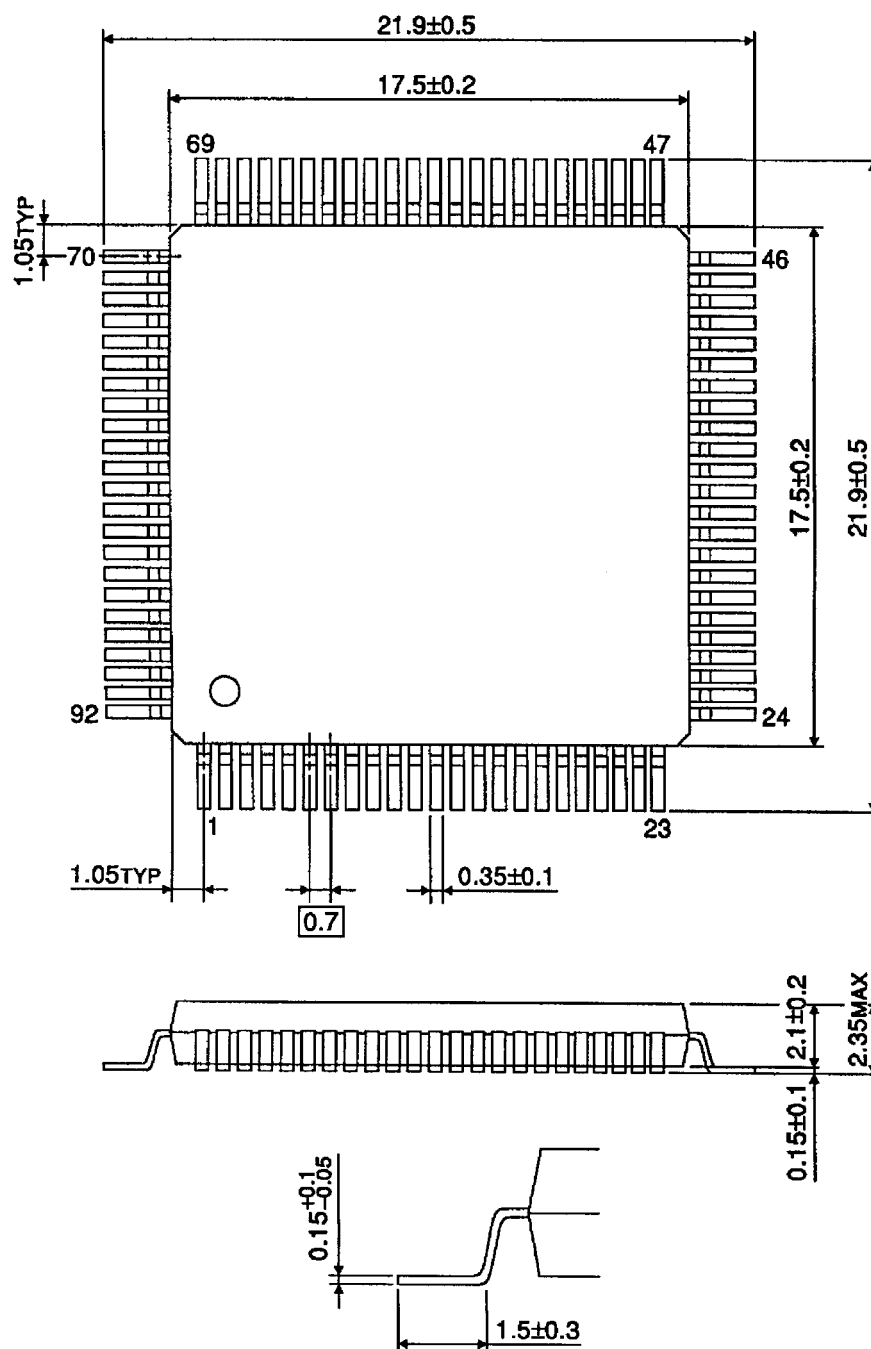


Application Circuit



QFP92-P-1818-0.70A

Unit : mm



Weight : 1.4g (Typ.)

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