

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# T6A41

## COLUMN DRIVER LSI FOR A DOT MATRIX LCD

The T6A41 is a column driver with 64-output channels for a dot matrix LCD.

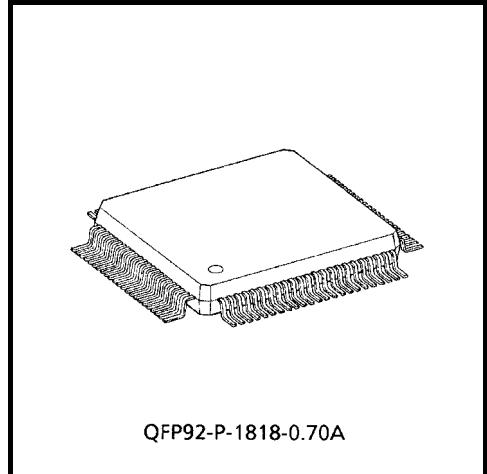
The T6A41 realizes low power LCD systems using the CMOS Si-Gate process.

The T6A41 has two bi-directional data Input / Output pins and three types of data flow (pin program):

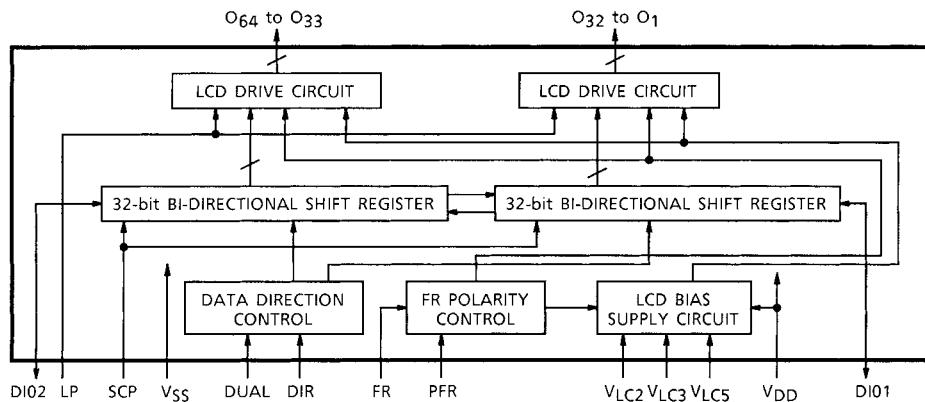
(1) O<sub>1</sub> → O<sub>64</sub>, (2) O<sub>64</sub> → O<sub>1</sub>, (3) O<sub>1</sub> → O<sub>32</sub>, O<sub>64</sub> → O<sub>33</sub>.

### Features

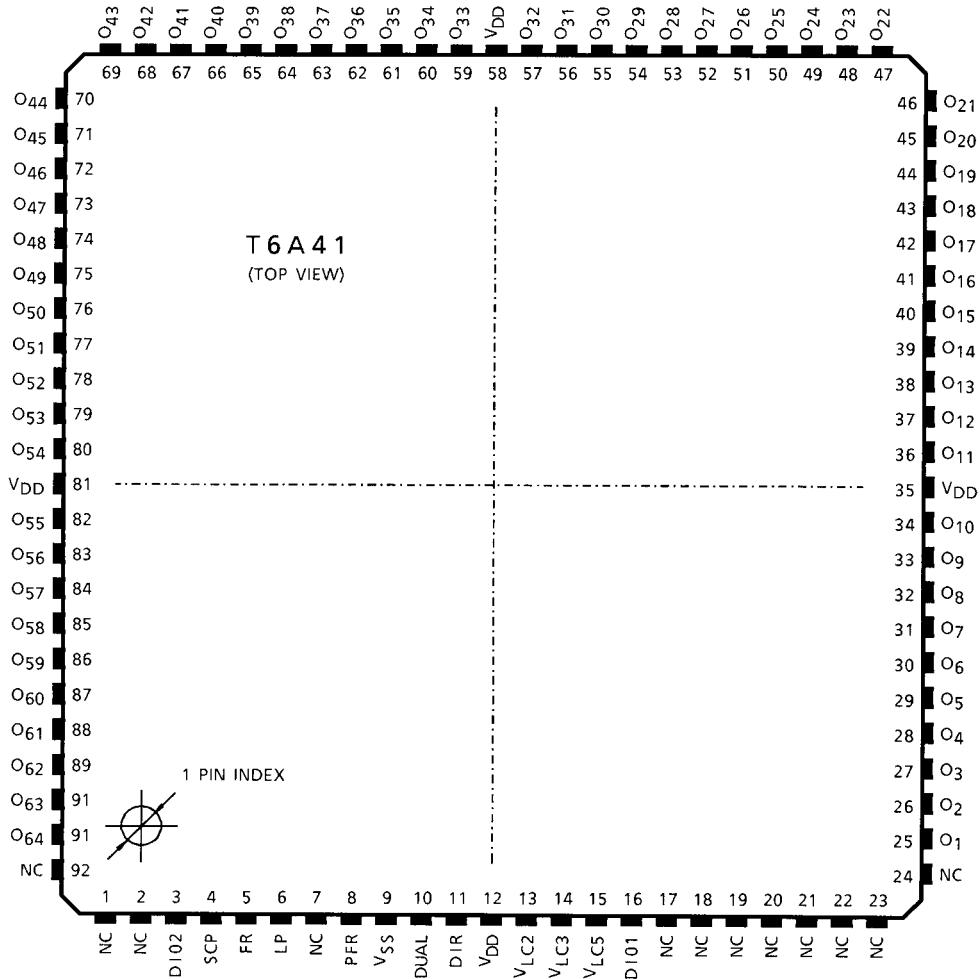
- 64-output column driver
- Three types of data flow:
  - (1) O<sub>1</sub> → O<sub>64</sub>
  - (2) O<sub>64</sub> → O<sub>1</sub>
  - (3) O<sub>1</sub> → O<sub>32</sub>, O<sub>64</sub> → O<sub>33</sub>
- High speed operation
- Low power consumption
- Power supply: 5 V ± 10%
- 92-pin plastic flat package



### Block Diagram



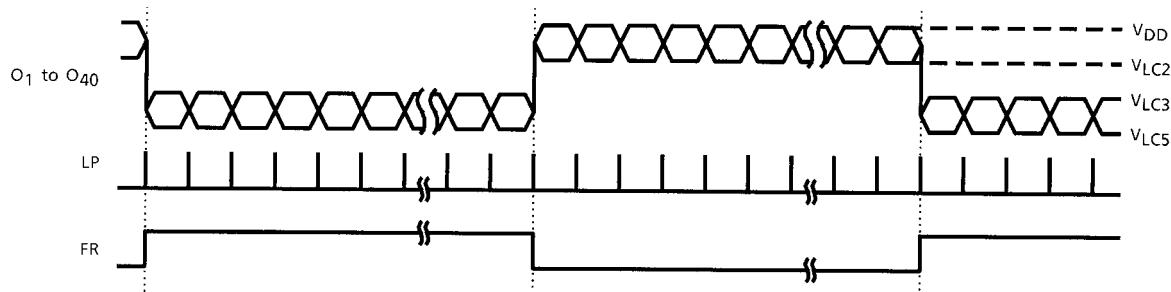
## Pin Assignment



## Pin Functions

Pin Name	I / O	Functions	Level	
O <sub>1</sub> to O <sub>64</sub>	Output	LCD drive signal output	V <sub>DD</sub> to V <sub>LC5</sub>	
DIO1 , DIO2	I / O	Bi-directional data input and output		
SCP	Input	(Shift Clock Pulse) Shift clock pulse input		
FR	Input	(Frame) Frame signal input		
LP	Input	(Latch Pulse) Latch pulse signal input		
DUAL	Input	(Dual Mode) Selects dual mode or single mode data flow.	DUAL	DIR
			L	L
			L	H
			H	L
			H	H
			OUT	IN
			IN	OUT
			—	—
			IN	IN
			O <sub>64</sub> → O <sub>1</sub>	O <sub>1</sub> → O <sub>64</sub>
			O <sub>64</sub> → O <sub>1</sub>	O <sub>1</sub> → O <sub>32</sub> , O <sub>64</sub> → O <sub>33</sub>
DIR	Input	(Direction) Selects input data flow direction.		
PFR	Input	(Polarity of Flame) Usually connected to V <sub>SS</sub>		
V <sub>LC2</sub>	—	Power supply for LCD drive		
V <sub>LC3</sub>	—	Power supply for LCD drive		
V <sub>LC5</sub>	—	Power supply for LCD drive		
V <sub>DD</sub>	—	Power supply (5 V)		
V <sub>SS</sub>	—	Power supply (0 V)		

## Timing Diagram



**Absolute Maximum Ratings (Ta = 25°C)**

Item	Symbol	Rating	Unit
Supply Voltage (1)	V <sub>DD</sub> (Note 1)	-0.3 to 7.0	V
Supply Voltage (2)	V <sub>LC2</sub> , V <sub>LC3</sub> , V <sub>LC5</sub> (Note 1, 2)	-0.3 to 7.0	V
Input Voltage	V <sub>IN</sub> (Note 1)	-0.3 to V <sub>DD</sub> + 0.3	V
Operating Temperature	T <sub>opr</sub>	-20 to 75	°C
Storage Temperature	T <sub>stg</sub>	-55 to 125	°C

Note 1: Referenced to V<sub>SS</sub> = 0 V

Note 2: Ensure that the following condition is always maintained.

$$V_{DD} \geq V_{LC2} \geq V_{LC3} \geq V_{LC5}$$

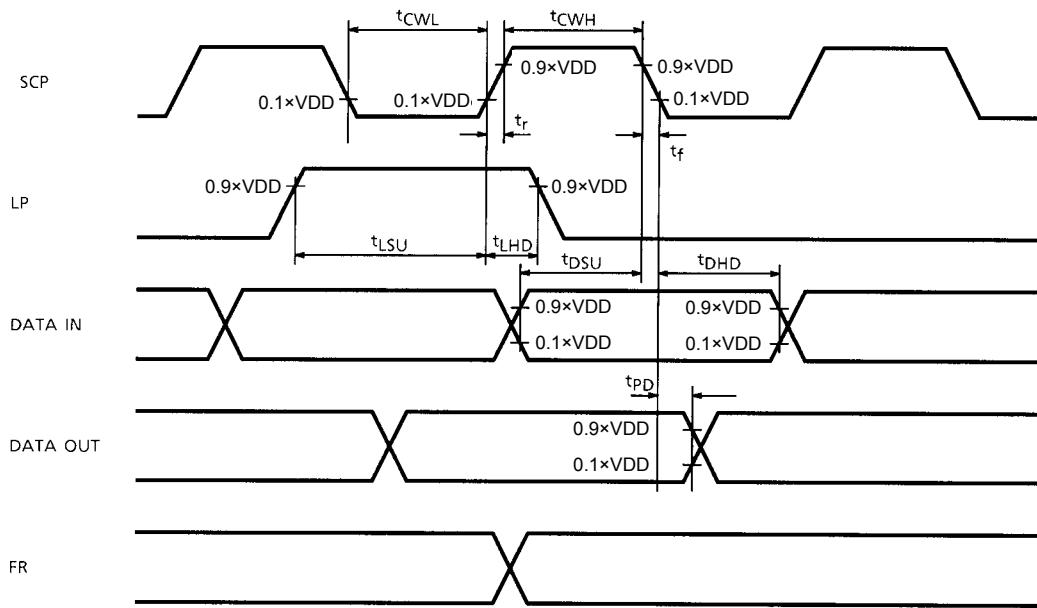
**Electrical Characteristics****DC Characteristics**

**Test Conditions** (Unless Otherwise Noted, V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 5.0 V ± 10%,  
V<sub>LC5</sub> = 0 V, Ta = -20 to 75°C)

Item	Symbol	Test Circuit	Test Conditions	Min	Typ.	Max	Unit	Pin Name
Operating Voltage (1)	V <sub>DD</sub>	—	—	4.5	5.0	5.5	V	V <sub>DD</sub>
Operating Voltage (2)	V <sub>LC5</sub>	—	—	0	—	V <sub>DD</sub> -3.0	V	V <sub>LC5</sub>
Input Voltage	H Level	V <sub>IH</sub>	—	V <sub>DD</sub> -1.0	—	V <sub>DD</sub>	V	(*)
	L Level	V <sub>IL</sub>	—	0	—	1.0	V	(*)
Output Voltage	H Level	V <sub>OH</sub>	I <sub>OH</sub> = -0.4 mA	V <sub>DD</sub> -0.4	—	V <sub>DD</sub>	V	DIO1, DIO2
	L Level	V <sub>OL</sub>	I <sub>Oh</sub> = 0.4 mA	0	—	0.4	V	DIO1, DIO2
Output Resistance	R <sub>COL</sub>	—	I <sub>d</sub> = ±50 µA	—	—	30	kΩ	O <sub>1</sub> to O <sub>64</sub>
Operating Frequency	f <sub>scp</sub>	—	T <sub>a</sub> = -20 to 75°C	—	—	400	kHz	SCP
Current Consumption	I <sub>SS</sub>	—	V <sub>DD</sub> = 5.0 V V <sub>LC2</sub> = 3.0 V V <sub>LC3</sub> = 2.0 V V <sub>LC5</sub> = 0.0 V f <sub>FR</sub> = 39 Hz f <sub>SCP</sub> = 250 kHz O <sub>1</sub> to O <sub>80</sub> : No Load	Binary Data Input	—	—	1.0	mA
				Input Data : LOW Constant	—	—	0.4	mA

\*: DIO1, DIO2, SCP, FR, LP, PFR, DUAL, DIR

## AC Characteristics



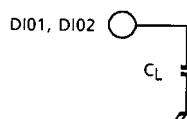
## Test Conditions

(Unless Otherwise Noted,  $V_{SS} = 0$  V,  $V_{DD} = 5$  V  $\pm 10\%$ ,  
 $V_{LC5} = 0$  V,  $T_a = -20$  to  $75^\circ\text{C}$ )

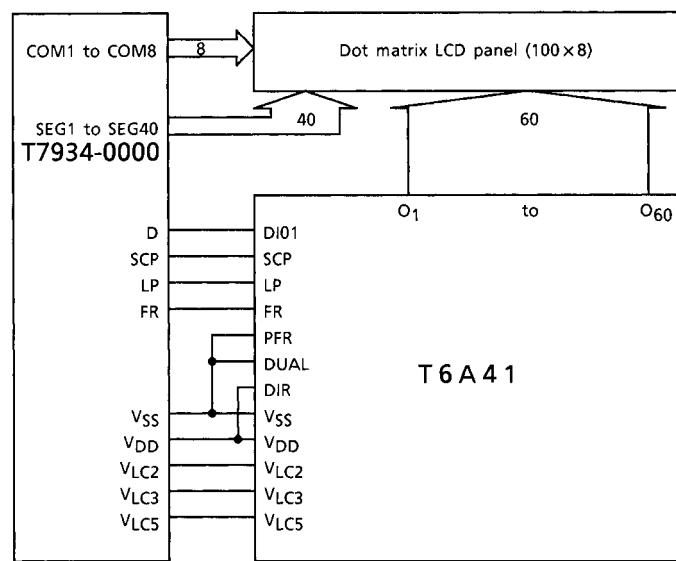
Item	Symbol	Min	Max	Unit
Operating Frequency	$f_{SCP}$	—	400	kHz
SCP Pulse Width	$t_{CWL}, t_{CWH}$	800	—	ns
SCP Rise / Fall Time	$t_r, t_f$	—	200	ns
LP Set-up Time	$t_{LSU}$	500	—	ns
LP Hold Time	$t_{LHD}$	—	10	ns
Data Set-up Time	$t_{DSU}$	300	—	ns
Data Hold Time	$t_{DHD}$	300	—	ns
Output Data Delay Time	$t_{PD}$ (Note)	—	500	ns

Note: With load circuit connected

## Load Circuit



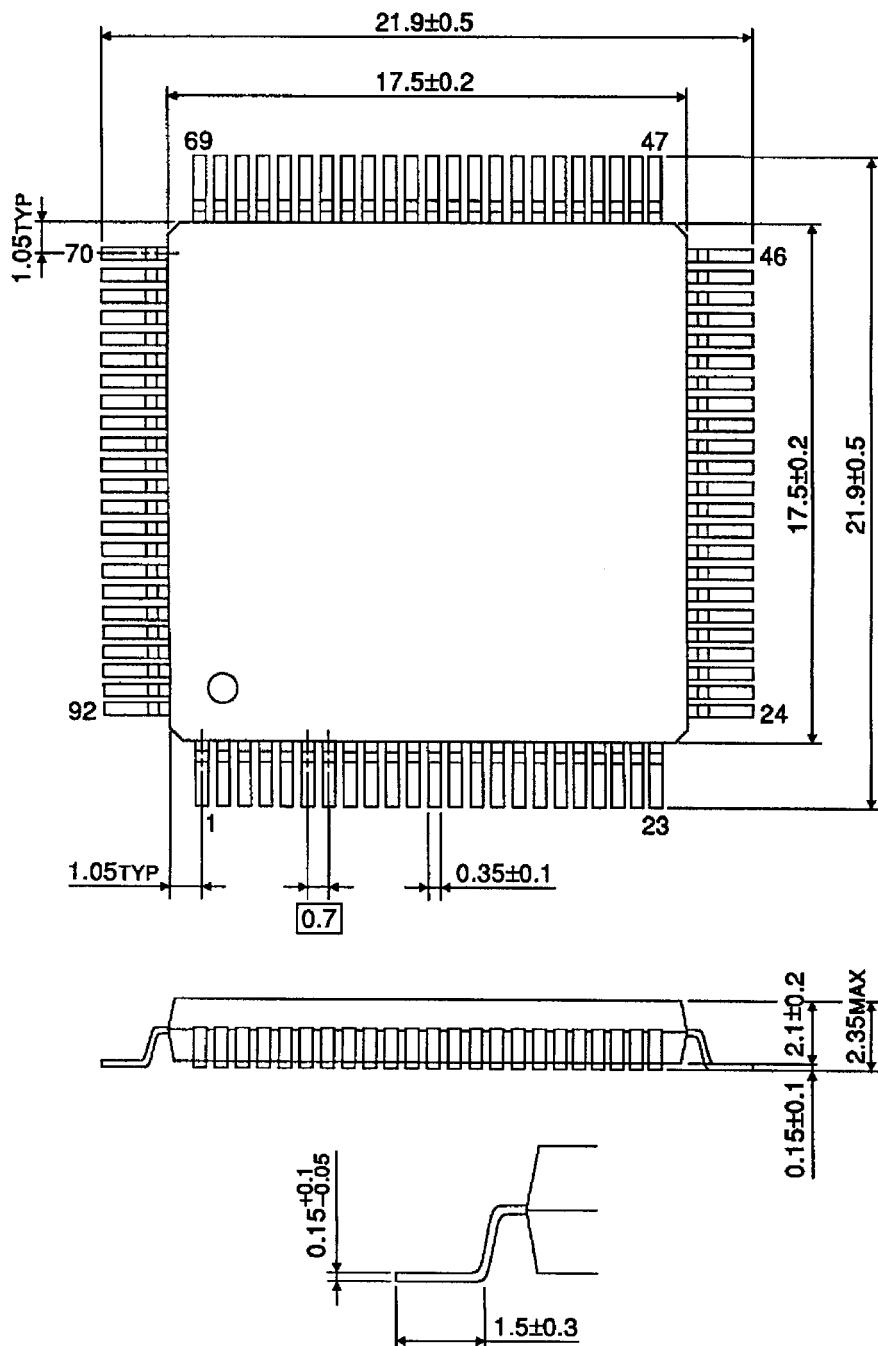
$C_L = 50\text{pF}$   
 (including wiring capacitance)

**Application Circuit**

**Package Dimensions**

QFP92-P-1818-0.70A

Unit : mm



Weight : 1.4g (Typ.)

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000707EBA

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