



# Precision Analog Microcontroller, 14-Bit Analog Input/Output with MDIO Interface, ARM Cortex-M3

Data Sheet

**ADuCM320**

## FEATURES

### Analog input/output

- Multichannel, 14-bit, 1 MSPS analog-to-digital converter (ADC)
  - Up to 16 ADC input channels
  - 0 V to VREF analog input range
  - Fully differential and single-ended modes
  - AV<sub>DD</sub> and IOV<sub>DD</sub> monitors
- 12-bit voltage output digital-to-analog converters (VDACs)
  - 8 VDACs with a range of 0 V to 2.5 V or AV<sub>DD</sub> outputs
- 12-bit current output DACs (IDACs)
  - 4 IDACs with a range of 0 mA to 150 mA outputs

### Voltage comparator

### Microcontroller

- ARM® Cortex®-M3 processor, 32-bit RISC architecture
- Serial wire port supports code download and debug

### Clocking options

- 80 MHz phase-locked loop (PLL) with programmable divider
- Trimmed on-chip oscillator ( $\pm 3\%$ )
- External 16 MHz crystal option
- External clock source up to 80 MHz

### Memory

- 2 × 128 kB independent Flash/EE memories
- 10,000 cycle Flash/EE endurance
- 20-year Flash/EE retention
- 32 kB SRAM

### Software triggered in-circuit reprogrammability via management data input/output (MDIO)

### On-chip peripherals

- MDIO slave up to 4 MHz
- 2 × I<sup>2</sup>C, 2 × SPI, UART
- Multiple general-purpose input/output (GPIO) pins: 3.6 V compliant
- 7 × 1.2 V compatible when used for MDIO
- 32-element programmable logic array (PLA)
- 3 general-purpose timers
- Wake-up timer
- Watchdog timer
- 16-bit pulse width modulator (PWM)

### Power

- Supply range: 2.9 V to 3.6 V, and 1.8 V to 2.5 V for IDACs
- Flexible operating modes for low power applications

### Packages and temperature range

- 6 mm × 6mm, 96-ball CSP\_BGA package
- Fully specified for -40°C to +105°C ambient operation

### Tools

- Low cost QuickStart™ development system
- Full third party support

## APPLICATIONS

### Optical networking

Rev. C

[Document Feedback](#)

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- ADuCM320 Evaluation Board

## DOCUMENTATION

### Application Notes

- AN-1310: Flash Programming via MDIO—Protocol Type 8
- AN-1322: ADuCM320 Code Execution Speed

### Data Sheet

- ADuCM320: Precision Analog Microcontroller, 14-Bit Analog I/O with MDIO Interface, ARM Cortex-M3 Data Sheet

### User Guides

- UG-498: ADuCM320 Hardware Reference Manual
- UG-692: ADuCM320 Development Systems Getting Started Tutorial

## DESIGN RESOURCES

- ADuCM320 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all ADuCM320 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

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Submit a technical question or find your regional support number.

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## REVISION HISTORY

### 10/15—Rev. B to Rev. C

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| Changes to Table 7 and Figure 5.....         | 18 |
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### 11/14—Rev. 0 to Rev. A

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### 6/14—Revision 0: Initial Version

## FUNCTIONAL BLOCK DIAGRAM

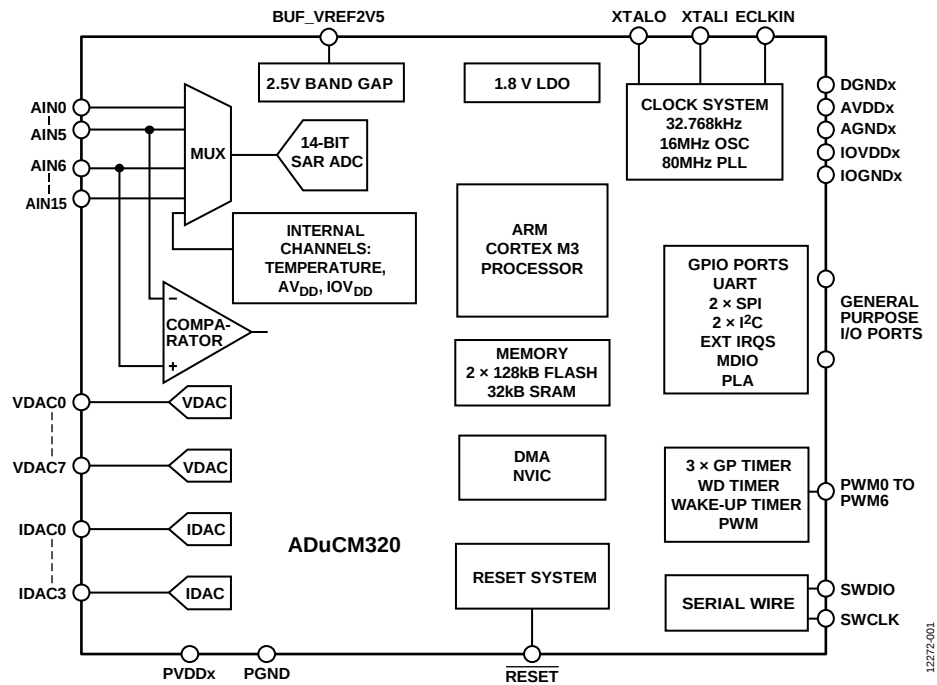


Figure 1.

## GENERAL DESCRIPTION

The [ADuCM320](#) is a fully integrated single package device that incorporates high performance analog peripherals together with digital peripherals controlled by an 80 MHz ARM Cortex-M3 processor and integral flash for code and data.

The ADC on the [ADuCM320](#) provides 14-bit, 1 MSPS data acquisition on up to 16 input pins that can be programmed for single-ended or differential operation. The voltage at the IDAC output pins can also be measured by the ADC, which is useful for controlling the power consumption of the current DACs. Additionally, chip temperature and supply voltages can be measured.

The ADC input voltage is 0 V to VREF. A sequencer is provided, which allows a user to select a set of ADC channels to be measured in sequence without software involvement during the sequence. The sequence can optionally repeat automatically at a user selectable rate.

Up to eight VDACS are provided with output ranges that are programmable to one of two voltage ranges.

Four IDAC sources are provided. The output currents are programmable with ranges of 0 mA to 150 mA. A low drift band gap reference and voltage comparator completes the analog input peripheral set.

The [ADuCM320](#) can be configured so that the digital and analog outputs will retain their output voltages and currents through a watchdog or software reset sequence. Thus, a product can remain functional even while the [ADuCM320](#) is resetting itself.

The [ADuCM320](#) has a low power ARM Cortex-M3 processor and a 32-bit RISC machine that offers up to 100 MIPS peak performance. Also integrated on chip are 2 × 128 kB Flash/EE memory and 32 kB of SRAM. The flash comprises two separate 128 kB blocks supporting execution from one flash block and simultaneous writing/erasing of the other flash block.

The [ADuCM320](#) operates from an on-chip oscillator or a 16 MHz external crystal and a PLL at 80 MHz. This clock can

optionally be divided down to reduce current consumption. Additional low power modes can be set via software. In normal operating mode, the [ADuCM320](#) digital core consumes about 300  $\mu$ A per MHz.

The device includes an MDIO interface capable of operating at up to 4 MHz. The capability to simultaneously execute from one flash block and write/erase the other flash block makes the [ADuCM320](#) ideal for 10G, 40G, and 100G optical applications. User programming is eased by incorporating PHYADR and DEVADD hardware comparators. In addition, the nonerasable kernel code plus flags in user flash provide assistance by allowing user code to robustly switch between the two blocks of user flash code and data spaces.

The [ADuCM320](#) integrates a range of on-chip peripherals that can be configured under software control, as required in the application. These peripherals include 1 × UART, 2 × I<sup>2</sup>C, and 2 × SPI serial input/output communication controllers, GPIO, 32-element programmable logic array, 3 general-purpose timers, plus a wake-up timer and system watchdog timer. A 16-bit PWM with seven output channels is also provided.

GPIO pins on the device power up in high impedance input mode. In output mode, the software chooses between open-drain mode and push-pull mode. The pull-up resistors can be disabled and enabled in software. In GPIO output mode, the inputs can remain enabled to monitor the pins. The GPIO pins can also be programmed to handle digital or analog peripheral signals, in which case the pin characteristics are matched to the specific requirement.

A large support ecosystem is available for the ARM Cortex-M3 processor to ease product development of the [ADuCM320](#). Access is via the ARM serial wire debug port (SW-DP). On-chip factory firmware supports in-circuit serial download via MDIO. These features are incorporated into a low cost QuickStart development system supporting this precision analog microcontroller family.

## SPECIFICATIONS

### MICROCONTROLLER ELECTRICAL SPECIFICATIONS

AVDD = IOVDD = VDD1 = 2.9 V to 3.6 V (see Figure 14) maximum difference between supplies = 0.3 V, VREF = 2.5 V internal reference,  $f_{\text{CORE}} = 80 \text{ MHz}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. PVDDx for IDACs = 1.8 V to 2.5 V. Power-up sequence must be VDD1, IOVDDx, AVDDx, and then PVDDx, but no delays in the sequence are required.

Table 1.

| Parameter                       | Symbol              | Min   | Typ        | Max   | Unit                         | Test Conditions/Comments                                                                                                                                                        |
|---------------------------------|---------------------|-------|------------|-------|------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADC BASIC SPECIFICATIONS        |                     |       |            |       |                              |                                                                                                                                                                                 |
| ADC Power-Up Time               |                     |       | 5          |       | $\mu\text{s}$                | Single-ended mode, unless otherwise stated                                                                                                                                      |
| Data Rate                       | $f_{\text{SAMPLE}}$ |       |            | 1     | MSPS                         |                                                                                                                                                                                 |
| DC Accuracy <sup>1</sup>        |                     | 14    |            |       | Bits                         | 1 LSB = $2.5 \text{ V}/2^{14}$                                                                                                                                                  |
| Resolution <sup>1</sup>         |                     | 16    |            |       | Bits                         | Number of data bits                                                                                                                                                             |
| Integral Nonlinearity           | INL                 |       | $\pm 1.75$ |       | LSB                          | 2.5 V internal reference; 1 LSB = $2.5 \text{ V}/2^{14}$                                                                                                                        |
|                                 |                     |       | $\pm 1.75$ |       | LSB                          | 2.5 V external reference; 1 LSB = $2.5 \text{ V}/2^{14}$                                                                                                                        |
| Differential Nonlinearity       | DNL                 | -0.99 | $\pm 0.75$ | +1    | LSB                          | 2.5 V internal reference; 1 LSB = $2.5 \text{ V}/2^{14}$                                                                                                                        |
|                                 |                     |       | $\pm 0.75$ |       | LSB                          | 2.5 V external reference; 1 LSB = $2.5 \text{ V}/2^{14}$                                                                                                                        |
| DC Code Distribution            |                     |       | $\pm 3$    |       | LSB                          | ADC input 1.25 V; 1 LSB = $2.5 \text{ V}/2^{14}$                                                                                                                                |
| ADC ENDPOINT ERRORS             |                     |       |            |       |                              |                                                                                                                                                                                 |
| Offset Error                    |                     |       | $\pm 200$  |       | $\mu\text{V}$                |                                                                                                                                                                                 |
| Input Buffer Off                |                     |       |            |       | $\mu\text{V}/^\circ\text{C}$ | Using 2.5 V external reference                                                                                                                                                  |
| Drift <sup>1</sup>              |                     | -2.25 |            | +1.2  | $\mu\text{V}/^\circ\text{C}$ |                                                                                                                                                                                 |
| Input Buffer On                 |                     |       | -250       |       | $\mu\text{V}/^\circ\text{C}$ | Using 2.5 V external reference                                                                                                                                                  |
| Drift <sup>1</sup>              |                     | -2.6  |            | +2    | $\mu\text{V}/^\circ\text{C}$ |                                                                                                                                                                                 |
| Match                           |                     |       | $\pm 1$    |       | LSB                          | Matching compared to AIN8                                                                                                                                                       |
| Full-Scale Error                |                     |       |            |       | $\mu\text{V}$                |                                                                                                                                                                                 |
| Input Buffer Off                |                     |       | $\pm 400$  |       | $\mu\text{V}/^\circ\text{C}$ | Full-scale error drift minus offset error drift                                                                                                                                 |
| Gain Drift <sup>1</sup>         |                     | -4    |            | +2    | $\mu\text{V}/^\circ\text{C}$ |                                                                                                                                                                                 |
| Input Buffer On                 |                     |       | -350       |       | $\mu\text{V}/^\circ\text{C}$ | Full-scale error drift minus offset error drift                                                                                                                                 |
| Gain Drift <sup>1</sup>         |                     | -4.5  |            | +3    | $\mu\text{V}/^\circ\text{C}$ |                                                                                                                                                                                 |
| Match                           |                     |       | $\pm 1$    |       | LSB                          |                                                                                                                                                                                 |
| ADC DYNAMIC PERFORMANCE         |                     |       |            |       |                              |                                                                                                                                                                                 |
| Signal-to-Noise Ratio           | SNR                 |       |            |       |                              | $f_{\text{IN}} = 665.25 \text{ Hz}$ sine wave, $f_{\text{SAMPLE}} = 100 \text{ kSPS}$ ; input filter = $15 \Omega$ , $2 \text{ nF}$<br>Includes distortion and noise components |
| Input Buffer                    |                     |       |            |       |                              |                                                                                                                                                                                 |
| Disabled                        |                     |       | 80         |       | dB                           |                                                                                                                                                                                 |
| Enabled                         |                     |       | 74         |       | dB                           |                                                                                                                                                                                 |
| Total Harmonic Distortion       | THD                 |       |            |       |                              |                                                                                                                                                                                 |
| Input Buffer                    |                     |       |            |       |                              |                                                                                                                                                                                 |
| Disabled                        |                     |       | -86        |       | dB                           |                                                                                                                                                                                 |
| Enabled                         |                     |       | -83        |       | dB                           |                                                                                                                                                                                 |
| Peak Harmonic or Spurious Noise |                     |       | -88        |       | dB                           |                                                                                                                                                                                 |
| Channel-to-Channel Crosstalk    |                     |       | -90        |       | dB                           | Measured on adjacent channels                                                                                                                                                   |
| ADC INPUT                       |                     |       |            |       |                              |                                                                                                                                                                                 |
| Input Voltage Ranges            |                     |       |            |       |                              | Input buffer not enabled                                                                                                                                                        |
| Single-Ended Mode <sup>1</sup>  |                     | AGND4 |            | VREF  |                              |                                                                                                                                                                                 |
| Differential Mode <sup>1</sup>  |                     | -VREF |            | +VREF | V                            | Voltage between differential pins                                                                                                                                               |
| Compliance <sup>1</sup>         |                     | AGND4 |            | AVDD4 |                              |                                                                                                                                                                                 |
| Common Mode <sup>1</sup>        |                     | 0.9   |            | 1.6   | V                            |                                                                                                                                                                                 |

| Parameter                                                                                                                                                                                                                                                                                                                                                                                         | Symbol     | Min               | Typ                                                    | Max | Unit                                                                                                                           | Test Conditions/Comments                                                                                                                                                                                                                                                                                                                                                                       |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-------------------|--------------------------------------------------------|-----|--------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Leakage Current<br>AIN0 to AIN4, AIN6 to AIN15<br>AIN5<br>Input Current                                                                                                                                                                                                                                                                                                                           |            |                   | $\pm 1.5$<br>$\pm 20$<br>$\pm 9$<br>$\pm 6$<br>$\pm 4$ |     | nA<br>nA<br>$\mu\text{A}/\text{V}$<br>$\mu\text{A}/\text{V}$<br>$\mu\text{A}/\text{V}$                                         | Pin shared with comparator<br>At 1 MSPS; buffer off<br>$\leq 800$ kSPS; buffer off<br>500 kSPS; buffer off;<br>ADCCNVC[25:16] = 0x1E<br>During ADC acquisition                                                                                                                                                                                                                                 |
| Input Capacitance                                                                                                                                                                                                                                                                                                                                                                                 |            |                   | 20                                                     |     | pF                                                                                                                             |                                                                                                                                                                                                                                                                                                                                                                                                |
| ADC INPUT BUFFER <sup>2</sup><br>Voltage Compliance <sup>1</sup><br>Input Current                                                                                                                                                                                                                                                                                                                 |            | 0.15              |                                                        | 2.5 | V<br>nA                                                                                                                        | When enabled by software<br>Reduced accuracy below 0.15 V<br>$V_{\text{IN}} = 0.15 \text{ V}$ to $2.5 \text{ V}$ , ADC converting                                                                                                                                                                                                                                                              |
| ON-CHIP VOLTAGE REFERENCE<br><br>Accuracy<br>Reference Temperature Coefficient <sup>1</sup><br>Power Supply Rejection Ratio<br>Internal $V_{\text{REF}}$ Power-On Time                                                                                                                                                                                                                            |            |                   | 2.51                                                   |     | V                                                                                                                              | 0.47 $\mu\text{F}$ from $V_{\text{REF\_1V2}}$ to AGND4;<br>reference is measured with all<br>ADCs, VDACs, and IDACs enabled<br>$T_A = 25^\circ\text{C}$                                                                                                                                                                                                                                        |
|                                                                                                                                                                                                                                                                                                                                                                                                   | PSRR       | -34               | -15                                                    | +4  | mV<br>ppm/ $^\circ\text{C}$<br>dB<br>ms                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                |
| EXTERNAL REFERENCE INPUT<br>Range <sup>1</sup><br>Input Current                                                                                                                                                                                                                                                                                                                                   |            | 1.8               |                                                        | 2.5 | V<br>$\mu\text{A}$                                                                                                             | ADC                                                                                                                                                                                                                                                                                                                                                                                            |
| BUFFERED REFERENCE OUTPUT<br>Output Voltage<br>Accuracy<br>Reference Temperature Coefficient <sup>1</sup><br><br>Output Impedance<br>Load Current <sup>1</sup>                                                                                                                                                                                                                                    |            |                   | 2.504<br>$\pm 8$<br>-55<br>-5                          | +40 | V<br>mV<br>$\mu\text{V}/^\circ\text{C}$<br>$\Omega$<br>mA                                                                      | $T_A = 25^\circ\text{C}$ , load = 1.2 mA<br>100 nF from BUF_VREF2V5 to<br>AGND4<br>$T_A = 25^\circ\text{C}$                                                                                                                                                                                                                                                                                    |
| VDAC CHANNEL SPECIFICATIONS<br>DC Accuracy <sup>1</sup><br>Resolution <sup>1</sup><br>Relative Accuracy <sup>4</sup><br>Differential Nonlinearity <sup>4</sup><br><br>Offset Error<br><br>Drift<br>Gain Error <sup>5</sup><br><br>Drift<br>Mismatch<br>Analog Outputs<br>Output Voltage Range 1 <sup>1</sup><br>Output Voltage Range 2 <sup>1</sup><br>Output Impedance<br>DAC AC Characteristics | INL<br>DNL | 12<br>12<br>-0.99 | $\pm 4$                                                | +1  | Bits<br>Bits<br>LSB<br>LSB<br>mV<br>$\mu\text{V}/^\circ\text{C}$<br>%<br>%<br>ppm/ $^\circ\text{C}$<br>%<br>V<br>V<br>$\Omega$ | $R_L = 5 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$ <sup>3</sup><br>1 LSB = $2.5 \text{ V}/2^{12}$<br>Number of data bits<br>1 LSB = $2.5 \text{ V}/2^{12}$<br>Guaranteed monotonic, 1 LSB =<br>$2.5 \text{ V}/2^{12}$<br>2.5 V internal reference, DAC<br>Output Code 0<br>0 V to internal $V_{\text{REF}}$ range<br>0 V to AVDD range<br>Excluding reference drift<br>% of full scale on DAC0 |
| Output Settling Time<br>Glitch Energy                                                                                                                                                                                                                                                                                                                                                             |            |                   | 10<br>$\pm 20$                                         |     | $\mu\text{s}$<br>nV-sec                                                                                                        | Settled to $\pm 1$ LSB<br>1 LSB change when the maximum<br>number of bits changes<br>simultaneously in the<br>DACxDAT register                                                                                                                                                                                                                                                                 |
| IDAC CHANNEL SPECIFICATIONS<br>Resolution <sup>1</sup><br><br>Full-Scale Output <sup>1</sup><br>Supply Voltage Each Channel <sup>1</sup><br><br>Output Compliance Range<br>IDAC0, IDAC1<br>IDAC2, IDAC3                                                                                                                                                                                           |            | 14<br><br>1.8     | 150                                                    | 2.5 | Bits<br>mA<br>V<br>V<br>V                                                                                                      | Combination of overlapping<br>11 bits and 5 bits<br>Separate PVDDx supply for each<br>channel<br>See Figure 11<br>See Figure 11                                                                                                                                                                                                                                                                |

| Parameter                                       | Symbol | Min    | Typ  | Max         | Unit   | Test Conditions/Comments                                                                                                                         |
|-------------------------------------------------|--------|--------|------|-------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| Full-Scale Error<br>IDAC0, IDAC1                |        |        |      | ±0.75       | %      | IDAC set to 85% of full scale<br>25°C to 105°C range                                                                                             |
|                                                 |        |        |      | ±3.5        | %      | –40°C to +105°C range                                                                                                                            |
| IDAC2, IDAC3                                    |        |        |      | ±0.75       | %      | –40°C to +105°C range                                                                                                                            |
| Full-Scale Error Drift<br>IDAC0, IDAC1          |        |        | 25   |             | µA/°C  | Internal V <sub>REF</sub>                                                                                                                        |
| –40°C to +85°C                                  |        |        | 5    |             | µA/°C  |                                                                                                                                                  |
| 25°C to 85°C                                    |        |        | 2    |             | µA/°C  | Internal V <sub>REF</sub>                                                                                                                        |
| IDAC2, IDAC3                                    |        |        | ±3   | ±6          | LSB    | 1 LSB = 150 mA/2 <sup>11</sup>                                                                                                                   |
| Integral Nonlinearity                           | INL    | –0.99  |      | +1.5        | LSB    | Guaranteed 11-bit monotonic,<br>1 LSB = 150 mA/2 <sup>11</sup>                                                                                   |
| Differential Nonlinearity                       | DNL    |        |      |             |        |                                                                                                                                                  |
| Zero-Scale Error                                |        |        | ±50  |             | µA     |                                                                                                                                                  |
| Zero-Scale Error Drift<br>IDAC0, IDAC1          |        |        | ±300 |             | nA/°C  |                                                                                                                                                  |
| IDAC2, IDAC3                                    |        |        | ±800 |             | nA/°C  |                                                                                                                                                  |
| Noise Current                                   |        |        | 2    |             | µA     | IDACxCON[5:2] = 0                                                                                                                                |
| Pull-Down Current                               |        | –220   | –165 | –100        | µA     | When enabled                                                                                                                                     |
| Settling Time                                   |        |        |      |             |        | IDACxCON[5:2] = 0                                                                                                                                |
| To 0.1%                                         |        |        | 100  |             | µs     | ±4 mA change from midscale                                                                                                                       |
| To 1%                                           |        |        | 50   |             | µs     | ±4 mA change from midscale                                                                                                                       |
| Full Scale to 0 mA                              |        |        | 20   |             | µs     | Pull-down enabled                                                                                                                                |
| Overheat Shutdown                               |        |        | 135  |             | °C     | Junction temperature                                                                                                                             |
| PVDD ACPSRR                                     |        |        |      |             |        | IDACxCON[5:2] = 0                                                                                                                                |
| 100 Hz                                          |        |        | 51   |             | dB     |                                                                                                                                                  |
| 1 kHz                                           |        |        | 45   |             | dB     |                                                                                                                                                  |
| 10 kHz                                          |        |        | 25   |             | dB     |                                                                                                                                                  |
| 100 kHz                                         |        |        | 10   |             | dB     |                                                                                                                                                  |
| COMPARATOR                                      |        |        |      |             |        |                                                                                                                                                  |
| Input                                           |        |        |      |             |        |                                                                                                                                                  |
| Offset Voltage                                  |        |        | ±10  |             | mV     |                                                                                                                                                  |
| Bias Current                                    |        |        | 1    |             | nA     |                                                                                                                                                  |
| Voltage Range <sup>1</sup>                      |        | AGNDx  |      | AVDDx – 1.2 | V      |                                                                                                                                                  |
| Capacitance                                     |        |        | 7    |             | pF     |                                                                                                                                                  |
| Hysteresis <sup>1</sup>                         |        | 8.5    |      | 15          | mV     | When enabled in software                                                                                                                         |
| Response Time                                   |        |        | 7    |             | µs     | AFECOMP[2:1] = 0                                                                                                                                 |
| TEMPERATURE SENSOR                              |        |        |      |             |        |                                                                                                                                                  |
| Resolution                                      |        |        | 0.5  |             | °C     | Indicates die temperature, see<br>Figure 9                                                                                                       |
| Accuracy <sup>1</sup>                           |        | 1.34   |      | 1.43        | V      | When precision calibrated by the<br>user <sup>6</sup><br>ADC measured voltage for<br>temperature sensor channel without<br>calibration, T = 25°C |
| POWER-ON RESET                                  | POR    |        | 2.85 | 2.9         | V      |                                                                                                                                                  |
| External Reset Minimum Pulse Width <sup>1</sup> |        | 1.5    |      |             | µs     | Minimum pulse width required on<br>external reset pin to trigger a reset<br>sequence                                                             |
| WATCHDOG TIMER                                  | WDT    |        |      |             |        |                                                                                                                                                  |
| Timeout Period                                  |        |        | 32   |             | sec    | Default at power-up                                                                                                                              |
| FLASH/EE MEMORY                                 |        |        |      |             |        |                                                                                                                                                  |
| Endurance <sup>1</sup>                          |        | 10,000 |      |             | Cycles |                                                                                                                                                  |
| Data Retention <sup>1</sup>                     |        | 20     |      |             | Years  | T <sub>J</sub> = 85°C                                                                                                                            |

| Parameter                                                         | Symbol    | Min                         | Typ       | Max                         | Unit          | Test Conditions/Comments                                                                     |
|-------------------------------------------------------------------|-----------|-----------------------------|-----------|-----------------------------|---------------|----------------------------------------------------------------------------------------------|
| DIGITAL INPUTS                                                    |           |                             |           |                             |               |                                                                                              |
| Input Leakage Current                                             |           |                             |           |                             |               |                                                                                              |
| Logic 1 GPIO                                                      |           |                             | 1         |                             | nA            | $V_{IH} = V_{DD}$ , pull-up resistor disabled                                                |
| Logic 0 GPIO                                                      |           |                             | 10        |                             | nA            | $V_{IL} = 0\text{ V}$ , pull-up resistor disabled                                            |
| PRTADDRx                                                          |           |                             |           |                             |               |                                                                                              |
| Input Leakage Current                                             |           |                             | 16        |                             | $\mu\text{A}$ | $V_{IN} = 0$ to 1.8 V, due to weak pull-up resistors to 1.8 V                                |
| Input Voltage                                                     |           | 0.84                        |           | 1.5                         | V             | External resistor $91\text{ k}\Omega \pm 1\%$ to ground, range for CFP MSA high <sup>1</sup> |
| Input Capacitance, All Pins Except MCK, MDIO, PRTADDRx, and XTALx |           |                             | 10        |                             | pF            |                                                                                              |
| Input Capacitance                                                 |           |                             |           |                             |               |                                                                                              |
| MCK, PRTADDRx                                                     |           |                             | 6.5       |                             | pF            |                                                                                              |
| MDIO                                                              |           |                             | 8.5       |                             | pF            |                                                                                              |
| Pin Capacitance                                                   |           |                             |           |                             |               |                                                                                              |
| XTALI                                                             |           |                             | 5         |                             | pF            |                                                                                              |
| XTALO                                                             |           |                             | 5         |                             | pF            |                                                                                              |
| LOGIC INPUTS                                                      |           |                             |           |                             |               |                                                                                              |
| GPIO Input Voltage                                                |           |                             |           |                             |               |                                                                                              |
| Low                                                               | $V_{INL}$ |                             |           | $0.25 \times \text{IOVDDx}$ | V             |                                                                                              |
| High                                                              | $V_{INH}$ | $0.58 \times \text{IOVDDx}$ |           |                             | V             |                                                                                              |
| MDIO                                                              |           |                             |           |                             |               |                                                                                              |
| PRTADDRx Input Voltage                                            |           |                             |           |                             |               |                                                                                              |
| Low                                                               | $V_{INL}$ |                             |           | 0.36                        | V             |                                                                                              |
| High                                                              | $V_{INH}$ | 0.84                        |           |                             | V             |                                                                                              |
| MCK, MDIO Input Voltage                                           |           |                             |           |                             |               |                                                                                              |
| Low                                                               | $V_{INL}$ |                             |           | 0.36                        | V             |                                                                                              |
| High                                                              | $V_{INH}$ | 0.84                        |           |                             | V             |                                                                                              |
| XTALI Input Voltage                                               |           |                             |           |                             |               |                                                                                              |
| Low                                                               | $V_{INL}$ |                             | 1.1       |                             | V             |                                                                                              |
| High                                                              | $V_{INH}$ |                             | 1.7       |                             | V             |                                                                                              |
| Pull-Up Current                                                   |           | 30                          |           | 120                         | $\mu\text{A}$ | $V_{IN} = 0\text{ V}$ , see Figure 10                                                        |
| Pull-Down Current                                                 |           | 30                          |           | 100                         | $\mu\text{A}$ | $V_{IN} = 3.3\text{ V}$ , see Figure 10                                                      |
| LOGIC OUTPUTS                                                     |           |                             |           |                             |               |                                                                                              |
| GPIO Output Voltage <sup>7</sup>                                  |           |                             |           |                             |               |                                                                                              |
| High                                                              | $V_{OH}$  | $\text{IOVDDx} - 0.4$       |           |                             | V             | $I_{SOURCE} = 2\text{ mA}$                                                                   |
| Low                                                               | $V_{OL}$  |                             |           | 0.4                         | V             | $I_{SINK} = 2\text{ mA}$                                                                     |
| GPIO Short-Circuit Current <sup>1</sup>                           |           |                             | 11        |                             | mA            | See Figure 13                                                                                |
| MDIO                                                              |           |                             |           |                             |               |                                                                                              |
| Output Voltage                                                    |           |                             |           |                             |               |                                                                                              |
| High                                                              | $V_{OH}$  | 1.0                         |           |                             | V             | $I_{SOURCE} = 4\text{ mA}$                                                                   |
| Low                                                               | $V_{OL}$  |                             |           | 0.2                         | V             | $I_{SINK} = 4\text{ mA}$                                                                     |
| Delay Time                                                        |           |                             |           | 100                         | ns            | MCK to MDIO out                                                                              |
| OSCILLATORS                                                       |           |                             |           |                             |               |                                                                                              |
| Internal System Oscillator                                        |           |                             | 16        |                             | MHz           |                                                                                              |
| Accuracy                                                          |           |                             | $\pm 0.5$ | $\pm 3$                     | %             |                                                                                              |
| System PLL                                                        |           |                             | 80        |                             | MHz           | Main system clock                                                                            |
| External Crystal Oscillator                                       |           |                             | 16        |                             | MHz           | Can be selected in place of internal oscillator                                              |
| 32 kHz Internal Oscillator                                        |           |                             | 32.768    |                             | kHz           | Use for watchdog                                                                             |
| Accuracy                                                          |           |                             | $\pm 5$   | $\pm 20$                    | %             |                                                                                              |
| External Clock                                                    |           | 0.05                        |           | 80                          | MHz           | Can be selected in place of PLL                                                              |
| START-UP TIME                                                     |           |                             |           |                             |               |                                                                                              |
| At Power-On                                                       |           |                             | 40        |                             | ms            | Processor clock = 80 MHz                                                                     |
| After Other Reset                                                 |           |                             | 1.5       |                             | ms            | POR to first user code execution                                                             |
| From All Power-Down Modes                                         |           |                             | 1.25      |                             | $\mu\text{s}$ | Reset to first user code execution                                                           |

| Parameter                                       | Symbol | Min | Typ  | Max | Unit | Test Conditions/Comments                                                                                                            |
|-------------------------------------------------|--------|-----|------|-----|------|-------------------------------------------------------------------------------------------------------------------------------------|
| PROGRAMMABLE LOGIC ARRAY                        | PLA    |     |      |     |      |                                                                                                                                     |
| Propagation Delay                               |        |     |      |     |      |                                                                                                                                     |
| Pin                                             |        |     | 17   |     | ns   | From input pin to output pin                                                                                                        |
| Element                                         |        |     | 1.5  |     | ns   | Per PLA cell                                                                                                                        |
| EXTERNAL INTERRUPTS                             |        |     |      |     |      |                                                                                                                                     |
| Pulse Width <sup>1</sup>                        |        |     |      |     |      |                                                                                                                                     |
| Level Triggered                                 |        | 7   |      |     | ns   |                                                                                                                                     |
| Edge Triggered                                  |        | 1   |      |     | ns   |                                                                                                                                     |
| POWER REQUIREMENTS <sup>8</sup>                 |        |     |      |     |      |                                                                                                                                     |
| Power Supply Voltage Range                      |        |     |      |     |      |                                                                                                                                     |
| AVDDx to AGNDx and IOVDDx to DGNDx <sup>1</sup> |        | 2.9 | 3.3  | 3.6 | V    |                                                                                                                                     |
| Analog Power Supply Currents                    |        |     |      |     |      |                                                                                                                                     |
| AVDDx Current                                   |        |     | 6.3  |     | mA   | Analog peripherals in idle mode                                                                                                     |
| Digital Power Supply Current                    |        |     |      |     |      |                                                                                                                                     |
| IOVDDx Current in Normal Mode                   |        |     | 4    |     | mA   | All GPIO pull-up resistors enabled                                                                                                  |
| VDDx Current                                    |        |     |      |     |      |                                                                                                                                     |
| Normal Mode <sup>9</sup>                        |        |     | 29   |     | mA   | CD = 0 (80 MHz clock) executing typical code                                                                                        |
|                                                 |        |     | 20   |     | mA   | CD = 1 executing typical code                                                                                                       |
|                                                 |        |     | 10   |     | mA   | CD = 7 executing typical code                                                                                                       |
| CORE_SLEEP Mode <sup>9</sup>                    |        |     | 16   |     | mA   |                                                                                                                                     |
| SYS_SLEEP Mode <sup>9</sup>                     |        |     | 8    |     | mA   |                                                                                                                                     |
| Hibernate Mode <sup>9</sup>                     |        |     | 6.6  |     | mA   |                                                                                                                                     |
| Additional Power Supply Currents                |        |     |      |     |      |                                                                                                                                     |
| ADC                                             |        |     | 4.1  |     | mA   | Continuously converting at 100 kSPS                                                                                                 |
| ADC Input Buffer                                |        |     | 4.0  |     | mA   | Both buffers enabled                                                                                                                |
| IDAC                                            |        |     | 16.5 |     | mA   | Excluding load current                                                                                                              |
| DAC                                             |        |     | 340  |     | μA   | Per powered up DAC, excluding load current                                                                                          |
| Total Supply Current                            |        | 35  | 40   | 45  | mA   | VDD1, IOVDDx, AVDDx connected together; condition when entering user code: peripheral clocks on, peripherals idle, no load currents |
| Thermal Performance                             |        |     |      |     |      |                                                                                                                                     |
| Impedance Junction to Ambient                   |        |     | 45   |     | °C/W | JEDEC 2S2P                                                                                                                          |

<sup>1</sup> These numbers are not production tested but are guaranteed by design and/or characterization data at production release.

<sup>2</sup> Enabling the input buffer changes the ADC input characteristics as described in this subsection.

<sup>3</sup> The data in this section also applies for a load of  $R_L = 1\text{ k}\Omega$  and  $C_L = 100\text{ pF}$  to GND but only for 0 V to 2.5 V. However, this is not production tested.

<sup>4</sup> DAC linearity is calculated using a reduced code range of 100 to 3900.

<sup>5</sup> DAC gain error is calculated using a reduced code range of 100 to an internal  $2.5\text{ V }V_{\text{REF}}$ .

<sup>6</sup> Due to self heating, internal temperature measurements cannot be used to predict external temperatures. This value is only relevant after user calibration and only for internal and external conditions identical to those at calibration.

<sup>7</sup> The average current from all GPIO pins must not exceed 3 mA per pin.

<sup>8</sup> Power figures exclude any load currents to external circuits.

<sup>9</sup> See the ADuCM320 reference manual, [How to Set up and Use the ADuCM320](#).

AVDD = IOVDD = VDD1 = 2.9 V to 3.6 V maximum difference between supplies = 0.3 V, VREF = 2.5 V internal reference,  $f_{\text{CORE}} = 80 \text{ MHz}$ ,  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ , unless otherwise noted. PVDDx for IDACs = 1.8 V to 2.5 V. Power-up sequence must be VDD1, IOVDDx, AVDDx, and then PVDDx, but no delays in the sequence are required.

Table 2.

| Parameter                       | Symbol              | Min   | Typ        | Max   | Unit                         | Test Conditions/Comments                                                                                                                                                        |
|---------------------------------|---------------------|-------|------------|-------|------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADC BASIC SPECIFICATIONS        |                     |       |            |       |                              |                                                                                                                                                                                 |
| ADC Power-Up Time               |                     |       | 5          |       | $\mu\text{s}$                | Single-ended mode, unless otherwise stated                                                                                                                                      |
| Data Rate                       | $f_{\text{SAMPLE}}$ |       |            | 1     | MSPS                         |                                                                                                                                                                                 |
| DC Accuracy <sup>1</sup>        |                     | 14    |            |       | Bits                         |                                                                                                                                                                                 |
| Resolution <sup>1</sup>         |                     | 16    |            |       | Bits                         |                                                                                                                                                                                 |
| Integral Nonlinearity           | INL                 |       | $\pm 1.75$ |       | LSB                          |                                                                                                                                                                                 |
|                                 |                     |       | $\pm 1.75$ |       | LSB                          | 1 LSB = $2.5 \text{ V}/2^{14}$                                                                                                                                                  |
| Differential Nonlinearity       | DNL                 | -0.99 | $\pm 0.75$ | +1.5  | LSB                          | 2.5 V internal reference; 1 LSB = $2.5 \text{ V}/2^{14}$                                                                                                                        |
|                                 |                     |       | $\pm 0.75$ |       | LSB                          | 2.5 V external reference; 1 LSB = $2.5 \text{ V}/2^{14}$                                                                                                                        |
| DC Code Distribution            |                     |       | $\pm 3$    |       | LSB                          | 2.5 V internal reference; 1 LSB = $2.5 \text{ V}/2^{14}$                                                                                                                        |
|                                 |                     |       |            |       |                              | 2.5 V external reference; 1 LSB = $2.5 \text{ V}/2^{14}$                                                                                                                        |
|                                 |                     |       |            |       |                              | ADC input 1.25 V; 1 LSB = $2.5 \text{ V}/2^{14}$                                                                                                                                |
| ADC ENDPOINT ERRORS             |                     |       |            |       |                              |                                                                                                                                                                                 |
| Offset Error                    |                     |       |            |       | $\mu\text{V}$                | Using 2.5 V external reference                                                                                                                                                  |
| Input Buffer Off                |                     |       | $\pm 200$  |       | $\mu\text{V}/^\circ\text{C}$ |                                                                                                                                                                                 |
| Drift <sup>1</sup>              |                     | -2.25 |            | +1.2  | $\mu\text{V}$                |                                                                                                                                                                                 |
| Input Buffer On                 |                     |       | -250       |       | $\mu\text{V}$                | Using 2.5 V external reference                                                                                                                                                  |
| Drift <sup>1</sup>              |                     | -3    |            | +2    | $\mu\text{V}/^\circ\text{C}$ |                                                                                                                                                                                 |
| Match                           |                     |       | $\pm 1$    |       | LSB                          |                                                                                                                                                                                 |
| Full-Scale Error                |                     |       |            |       |                              | Matching compared to AIN8                                                                                                                                                       |
| Input Buffer Off                |                     |       | $\pm 400$  |       | $\mu\text{V}$                | Full-scale error drift minus offset error drift                                                                                                                                 |
| Gain Drift <sup>1</sup>         |                     | -4.3  |            | +2    | $\mu\text{V}/^\circ\text{C}$ |                                                                                                                                                                                 |
|                                 |                     |       |            |       |                              |                                                                                                                                                                                 |
| Input Buffer On                 |                     |       | -350       |       | $\mu\text{V}$                | Full-scale error drift minus offset error drift                                                                                                                                 |
| Gain Drift <sup>1</sup>         |                     | -4.5  |            | +3    | $\mu\text{V}/^\circ\text{C}$ |                                                                                                                                                                                 |
|                                 |                     |       |            |       |                              |                                                                                                                                                                                 |
| Match                           |                     |       | $\pm 1$    |       | LSB                          |                                                                                                                                                                                 |
| ADC DYNAMIC PERFORMANCE         |                     |       |            |       |                              |                                                                                                                                                                                 |
| Signal-to-Noise Ratio           | SNR                 |       |            |       |                              | $f_{\text{IN}} = 665.25 \text{ Hz}$ sine wave, $f_{\text{SAMPLE}} = 100 \text{ kSPS}$ ; input filter = $15 \Omega$ , $2 \text{ nF}$<br>Includes distortion and noise components |
| Input Buffer                    |                     |       |            |       |                              |                                                                                                                                                                                 |
| Disabled                        |                     |       | 80         |       | dB                           |                                                                                                                                                                                 |
| Enabled                         |                     |       | 74         |       | dB                           |                                                                                                                                                                                 |
| Total Harmonic Distortion       |                     |       |            |       |                              |                                                                                                                                                                                 |
| Input Buffer                    |                     |       |            |       |                              |                                                                                                                                                                                 |
| Disabled                        |                     |       | -86        |       | dB                           |                                                                                                                                                                                 |
| Enabled                         |                     |       | -83        |       | dB                           |                                                                                                                                                                                 |
| Peak Harmonic or Spurious Noise |                     |       | -88        |       | dB                           |                                                                                                                                                                                 |
| Channel-to-Channel Crosstalk    |                     |       | -90        |       | dB                           |                                                                                                                                                                                 |
|                                 |                     |       |            |       |                              | Measured on adjacent channels                                                                                                                                                   |
| ADC INPUT                       |                     |       |            |       |                              |                                                                                                                                                                                 |
| Input Voltage Ranges            |                     |       |            |       |                              | Input buffer not enabled                                                                                                                                                        |
| Single-Ended Mode <sup>1</sup>  |                     | AGND4 |            | VREF  |                              | Voltage between differential pins                                                                                                                                               |
| Differential Mode <sup>1</sup>  |                     | -VREF |            | +VREF | V                            |                                                                                                                                                                                 |
| Compliance <sup>1</sup>         |                     | AGND4 |            | AVDD4 | V                            |                                                                                                                                                                                 |
| Common Mode <sup>1</sup>        |                     | 0.9   |            | 1.6   | V                            |                                                                                                                                                                                 |

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                  | Symbol     | Min               | Typ                           | Max | Unit                                                                                              | Test Conditions/Comments                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-------------------|-------------------------------|-----|---------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Leakage Current<br>AIN0 to AIN4, AIN6 to AIN15<br>AIN5<br>Input Current                                                                                                                                                                                                                                                                                                                                                                    |            |                   | ±1.5<br>±20<br>±9<br>±6<br>±4 |     | nA<br>nA<br>µA/V<br>µA/V<br>µA/V                                                                  | Pin shared with comparator<br>At 1 MSPS; buffer off<br>≤800 kSPS; buffer off<br>500 kSPS; buffer off;<br>ADCCNVC[25:16] = 0x1E<br>During ADC acquisition                                                                                                                                                                                                                                                                                                                                                             |
| Input Capacitance                                                                                                                                                                                                                                                                                                                                                                                                                          |            |                   | 20                            |     | pF                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| ADC INPUT BUFFER <sup>2</sup><br>Voltage Compliance <sup>1</sup><br>Input Current                                                                                                                                                                                                                                                                                                                                                          |            | 0.15              |                               | 2.5 | V<br>nA                                                                                           | When enabled by software<br>Reduced accuracy below 0.15 V<br>V <sub>IN</sub> = 0.15 V to 2.5 V, ADC converting                                                                                                                                                                                                                                                                                                                                                                                                       |
| ON-CHIP VOLTAGE REFERENCE<br><br>Accuracy<br>Reference Temperature Coefficient <sup>1</sup><br>Power Supply Rejection Ratio<br>Internal V <sub>REF</sub> Power-On Time                                                                                                                                                                                                                                                                     |            |                   | 2.51                          |     | V                                                                                                 | 0.47 µF from VREF_1V2 to AGND4;<br>reference is measured with all<br>ADCs, VDACS, and IDACS enabled<br>T <sub>A</sub> = 25°C                                                                                                                                                                                                                                                                                                                                                                                         |
|                                                                                                                                                                                                                                                                                                                                                                                                                                            | PSRR       | −34               | −15                           | +4  | mV<br>ppm/°C<br>dB<br>ms                                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| EXTERNAL REFERENCE INPUT<br>Range <sup>1</sup><br>Input Current                                                                                                                                                                                                                                                                                                                                                                            |            | 1.8               |                               | 2.5 | V<br>µA                                                                                           | ADC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| BUFFERED REFERENCE OUTPUT<br>Output Voltage<br>Accuracy<br>Reference Temperature Coefficient <sup>1</sup><br><br>Output Impedance<br>Load Current <sup>1</sup>                                                                                                                                                                                                                                                                             |            |                   | 2.504<br>±8<br>−55<br>−5      | +40 | V<br>mV<br>µV/°C<br>Ω<br>mA                                                                       | T <sub>A</sub> = 25°C, load = 1.2 mA<br>100 nF from BUF_VREF2V5 to<br>AGND4<br>T <sub>A</sub> = 25°C                                                                                                                                                                                                                                                                                                                                                                                                                 |
| VDAC CHANNEL SPECIFICATIONS<br>DC Accuracy <sup>1</sup><br>Resolution <sup>1</sup><br>Relative Accuracy <sup>4</sup><br>Differential Nonlinearity <sup>4</sup><br><br>Offset Error<br><br>Drift<br>Gain Error <sup>5</sup><br><br>Drift<br>Mismatch<br>Analog Outputs<br>Output Voltage Range 1 <sup>1</sup><br>Output Voltage Range 2 <sup>1</sup><br>Output Impedance<br>DAC AC Characteristics<br>Output Settling Time<br>Glitch Energy | INL<br>DNL | 12<br>12<br>−0.99 | ±4                            | +1  | Bits<br>Bits<br>LSB<br>LSB<br>mV<br>µV/°C<br>%<br>%<br>ppm/°C<br>%<br>V<br>V<br>Ω<br>µs<br>nV-sec | R <sub>L</sub> = 5 kΩ, C <sub>L</sub> = 100 pF <sup>3</sup><br>1 LSB = 2.5 V/2 <sup>12</sup><br>Number of data bits<br>1 LSB = 2.5 V/2 <sup>12</sup><br>Guaranteed monotonic, 1 LSB =<br>2.5 V/2 <sup>12</sup><br>2.5 V internal reference, DAC<br>Output Code 0<br>0 V to internal V <sub>REF</sub> range<br>0 V to AVDD range<br>Excluding reference drift<br>% of full scale on DAC0<br>Settled to ±1 LSB<br>1 LSB change when the maximum<br>number of bits changes<br>simultaneously in the<br>DACxDAT register |
| IDAC CHANNEL SPECIFICATIONS<br>Resolution <sup>1</sup><br><br>Full-Scale Output <sup>1</sup><br>Supply Voltage Each Channel <sup>1</sup><br><br>Output Compliance Range<br>IDAC0, IDAC1<br>IDAC2, IDAC3                                                                                                                                                                                                                                    |            | 14<br><br>1.8     | 150                           | 2.5 | Bits<br>mA<br>V<br>V<br>V                                                                         | Combination of overlapping<br>11 bits and 5 bits<br>Separate PVDDx supply for each<br>channel<br>See Figure 11<br>See Figure 11                                                                                                                                                                                                                                                                                                                                                                                      |

| Parameter                                       | Symbol | Min    | Typ  | Max         | Unit   | Test Conditions/Comments                                                                                                                         |
|-------------------------------------------------|--------|--------|------|-------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| Full-Scale Error                                |        |        |      |             |        | IDAC set to 85% of full scale                                                                                                                    |
| IDAC0, IDAC1                                    |        |        |      | ±0.75       | %      | 25°C to 105°C range                                                                                                                              |
|                                                 |        |        |      | ±3.5        | %      |                                                                                                                                                  |
| IDAC2, IDAC3                                    |        |        |      | ±0.75       | %      |                                                                                                                                                  |
| Full-Scale Error Drift                          |        |        |      |             |        | Internal V <sub>REF</sub>                                                                                                                        |
| IDAC0, IDAC1                                    |        |        | 25   |             | µA/°C  |                                                                                                                                                  |
| –40°C to 105°C                                  |        |        | 5    |             | µA/°C  |                                                                                                                                                  |
| 25°C to 105°C                                   |        |        | 2    |             | µA/°C  |                                                                                                                                                  |
| IDAC2, IDAC3                                    |        |        |      |             |        | Internal V <sub>REF</sub>                                                                                                                        |
| Integral Nonlinearity                           | INL    |        | ±3   | ±6          | LSB    | 1 LSB = 150 mA/2 <sup>11</sup>                                                                                                                   |
| Differential Nonlinearity                       | DNL    | –0.99  |      | +1.5        | LSB    | Guaranteed 11-bit monotonic,<br>1 LSB = 150 mA/2 <sup>11</sup>                                                                                   |
| Zero-Scale Error                                |        |        | ±50  |             | µA     |                                                                                                                                                  |
| Zero-Scale Error Drift                          |        |        |      |             |        |                                                                                                                                                  |
| IDAC0, IDAC1                                    |        |        | ±300 |             | nA/°C  |                                                                                                                                                  |
| IDAC2, IDAC3                                    |        |        | ±800 |             | nA/°C  |                                                                                                                                                  |
| Noise Current                                   |        |        | 2    |             | µA     | IDACxCON[5:2] = 0                                                                                                                                |
| Pull-Down Current                               |        | –220   | –165 | –100        | µA     | When enabled                                                                                                                                     |
| Settling Time                                   |        |        |      |             |        | IDACxCON[5:2] = 0                                                                                                                                |
| To 0.1%                                         |        |        | 100  |             | µs     | ±4 mA change from midscale                                                                                                                       |
| To 1%                                           |        |        | 50   |             | µs     | ±4 mA change from midscale                                                                                                                       |
| Full Scale to 0 mA                              |        |        | 20   |             | µs     | Pull-down enabled                                                                                                                                |
| Overheat Shutdown                               |        |        | 135  |             | °C     | Junction temperature                                                                                                                             |
| PVDD ACPSRR                                     |        |        |      |             |        | IDACxCON[5:2] = 0                                                                                                                                |
| 100 Hz                                          |        |        | 51   |             | dB     |                                                                                                                                                  |
| 1 kHz                                           |        |        | 45   |             | dB     |                                                                                                                                                  |
| 10 kHz                                          |        |        | 25   |             | dB     |                                                                                                                                                  |
| 100 kHz                                         |        |        | 10   |             | dB     |                                                                                                                                                  |
| COMPARATOR                                      |        |        |      |             |        |                                                                                                                                                  |
| Input                                           |        |        |      |             |        |                                                                                                                                                  |
| Offset Voltage                                  |        |        | ±10  |             | mV     |                                                                                                                                                  |
| Bias Current                                    |        |        | 1    |             | nA     |                                                                                                                                                  |
| Voltage Range <sup>1</sup>                      |        | AGNDx  |      | AVDDx – 1.2 | V      |                                                                                                                                                  |
| Capacitance                                     |        |        | 7    |             | pF     |                                                                                                                                                  |
| Hysteresis <sup>1</sup>                         |        | 8.5    |      | 15          | mV     | When enabled in software                                                                                                                         |
| Response Time                                   |        |        | 7    |             | µs     | AFECOMP[2:1] = 0                                                                                                                                 |
| TEMPERATURE SENSOR                              |        |        |      |             |        |                                                                                                                                                  |
| Resolution                                      |        |        | 0.5  |             | °C     | Indicates die temperature, see<br>Figure 9                                                                                                       |
| Accuracy <sup>1</sup>                           |        | 1.34   |      | 1.43        | V      | When precision calibrated by the<br>user <sup>6</sup><br>ADC measured voltage for<br>temperature sensor channel without<br>calibration, T = 25°C |
| POWER-ON RESET                                  | POR    |        | 2.85 | 2.9         | V      |                                                                                                                                                  |
| External Reset Minimum Pulse Width <sup>1</sup> |        | 1.5    |      |             | µs     | Minimum pulse width required on<br>external reset pin to trigger a reset<br>sequence                                                             |
| WATCHDOG TIMER                                  | WDT    |        |      |             |        |                                                                                                                                                  |
| Timeout Period                                  |        |        | 32   |             | sec    | Default at power-up                                                                                                                              |
| FLASH/EE MEMORY                                 |        |        |      |             |        |                                                                                                                                                  |
| Endurance <sup>1</sup>                          |        | 10,000 |      |             | Cycles |                                                                                                                                                  |
| Data Retention <sup>1</sup>                     |        | 20     |      |             | Years  | T <sub>J</sub> = 85°C                                                                                                                            |

| Parameter                                                         | Symbol    | Min                         | Typ       | Max                         | Unit          | Test Conditions/Comments                                                                     |
|-------------------------------------------------------------------|-----------|-----------------------------|-----------|-----------------------------|---------------|----------------------------------------------------------------------------------------------|
| <b>DIGITAL INPUTS</b>                                             |           |                             |           |                             |               |                                                                                              |
| Input Leakage Current                                             |           |                             |           |                             |               |                                                                                              |
| Logic 1 GPIO                                                      |           |                             | 1         |                             | nA            | $V_{IH} = V_{DD}$ , pull-up resistor disabled                                                |
| Logic 0 GPIO                                                      |           |                             | 10        |                             | nA            | $V_L = 0\text{ V}$ , pull-up resistor disabled                                               |
| PRTADDRx                                                          |           |                             |           |                             |               |                                                                                              |
| Input Leakage Current                                             |           |                             | 16        |                             | $\mu\text{A}$ | $V_{IN} = 0$ to 1.8 V, due to weak pull-up resistors to 1.8 V                                |
| Input Voltage                                                     |           | 0.84                        |           | 1.5                         | V             | External resistor $91\text{ k}\Omega \pm 1\%$ to ground, range for CFP MSA high <sup>1</sup> |
| Input Capacitance, All Pins Except MCK, MDIO, PRTADDRx, and XTALx |           |                             | 10        |                             | pF            |                                                                                              |
| Input Capacitance                                                 |           |                             |           |                             |               |                                                                                              |
| MCK, PRTADDRx                                                     |           |                             | 6.5       |                             | pF            |                                                                                              |
| MDIO                                                              |           |                             | 8.5       |                             | pF            |                                                                                              |
| Pin Capacitance                                                   |           |                             |           |                             |               |                                                                                              |
| XTALI                                                             |           |                             | 5         |                             | pF            |                                                                                              |
| XTALO                                                             |           |                             | 5         |                             | pF            |                                                                                              |
| <b>LOGIC INPUTS</b>                                               |           |                             |           |                             |               |                                                                                              |
| GPIO Input Voltage                                                |           |                             |           |                             |               |                                                                                              |
| Low                                                               | $V_{INL}$ |                             |           | $0.25 \times \text{IOVDDx}$ | V             |                                                                                              |
| High                                                              | $V_{INH}$ | $0.58 \times \text{IOVDDx}$ |           |                             | V             |                                                                                              |
| MDIO                                                              |           |                             |           |                             |               |                                                                                              |
| PRTADDRx Input Voltage                                            |           |                             |           |                             |               |                                                                                              |
| Low                                                               | $V_{INL}$ |                             |           | 0.36                        | V             |                                                                                              |
| High                                                              | $V_{INH}$ | 0.84                        |           |                             | V             |                                                                                              |
| MCK, MDIO Input Voltage                                           |           |                             |           |                             |               |                                                                                              |
| Low                                                               | $V_{INL}$ |                             |           | 0.36                        | V             |                                                                                              |
| High                                                              | $V_{INH}$ | 0.84                        |           |                             | V             |                                                                                              |
| XTALI Input Voltage                                               |           |                             |           |                             |               |                                                                                              |
| Low                                                               | $V_{INL}$ |                             | 1.1       |                             | V             |                                                                                              |
| High                                                              | $V_{INH}$ |                             | 1.7       |                             | V             |                                                                                              |
| Pull-Up Current                                                   |           | 30                          |           | 120                         | $\mu\text{A}$ | $V_{IN} = 0\text{ V}$ , see Figure 10                                                        |
| Pull-Down Current                                                 |           | 30                          |           | 100                         | $\mu\text{A}$ | $V_{IN} = 3.3\text{ V}$ , see Figure 10                                                      |
| <b>LOGIC OUTPUTS</b>                                              |           |                             |           |                             |               |                                                                                              |
| GPIO Output Voltage <sup>7</sup>                                  |           |                             |           |                             |               |                                                                                              |
| High                                                              | $V_{OH}$  | $\text{IOVDDx} - 0.4$       |           |                             | V             | $I_{SOURCE} = 2\text{ mA}$                                                                   |
| Low                                                               | $V_{OL}$  |                             |           | 0.4                         | V             | $I_{SINK} = 2\text{ mA}$                                                                     |
| GPIO Short-Circuit Current <sup>1</sup>                           |           |                             | 11        |                             | mA            | See Figure 13                                                                                |
| MDIO                                                              |           |                             |           |                             |               |                                                                                              |
| Output Voltage                                                    |           |                             |           |                             |               |                                                                                              |
| High                                                              | $V_{OH}$  | 1.0                         |           |                             | V             | $I_{SOURCE} = 4\text{ mA}$                                                                   |
| Low                                                               | $V_{OL}$  |                             |           | 0.2                         | V             | $I_{SINK} = 4\text{ mA}$                                                                     |
| Delay Time                                                        |           |                             |           | 100                         | ns            | MCK to MDIO out                                                                              |
| <b>OSCILLATORS</b>                                                |           |                             |           |                             |               |                                                                                              |
| Internal System Oscillator                                        |           |                             | 16        |                             | MHz           |                                                                                              |
| Accuracy                                                          |           |                             | $\pm 0.5$ | $\pm 3$                     | %             |                                                                                              |
| System PLL                                                        |           |                             | 80        |                             | MHz           | Main system clock                                                                            |
| External Crystal Oscillator                                       |           |                             | 16        |                             | MHz           | Can be selected in place of internal oscillator                                              |
| 32 kHz Internal Oscillator                                        |           |                             | 32.768    |                             | kHz           | Use for watchdog                                                                             |
| Accuracy                                                          |           |                             | $\pm 5$   | $\pm 20$                    | %             |                                                                                              |
| External Clock                                                    |           | 0.05                        |           | 80                          | MHz           | Can be selected in place of PLL                                                              |
| <b>START-UP TIME</b>                                              |           |                             |           |                             |               |                                                                                              |
| At Power-On                                                       |           |                             | 40        |                             | ms            | Processor clock = 80 MHz                                                                     |
| After Other Reset                                                 |           |                             | 1.5       |                             | ms            | POR to first user code execution                                                             |
| From All Power-Down Modes                                         |           |                             | 1.25      |                             | $\mu\text{s}$ | Reset to first user code execution                                                           |

| Parameter                                       | Symbol | Min | Typ  | Max | Unit | Test Conditions/Comments                                                                                                            |
|-------------------------------------------------|--------|-----|------|-----|------|-------------------------------------------------------------------------------------------------------------------------------------|
| PROGRAMMABLE LOGIC ARRAY                        | PLA    |     |      |     |      |                                                                                                                                     |
| Propagation Delay                               |        |     |      |     |      |                                                                                                                                     |
| Pin                                             |        |     | 17   |     | ns   | From input pin to output pin                                                                                                        |
| Element                                         |        |     | 1.5  |     | ns   | Per PLA cell                                                                                                                        |
| EXTERNAL INTERRUPTS                             |        |     |      |     |      |                                                                                                                                     |
| Pulse Width <sup>1</sup>                        |        |     |      |     |      |                                                                                                                                     |
| Level Triggered                                 |        | 7   |      |     | ns   |                                                                                                                                     |
| Edge Triggered                                  |        | 1   |      |     | ns   |                                                                                                                                     |
| POWER REQUIREMENTS <sup>8</sup>                 |        |     |      |     |      |                                                                                                                                     |
| Power Supply Voltage Range                      |        |     |      |     |      |                                                                                                                                     |
| AVDDx to AGNDx and IOVDDx to DGNDx <sup>1</sup> |        | 2.9 | 3.3  | 3.6 | V    |                                                                                                                                     |
| Analog Power Supply Currents                    |        |     |      |     |      |                                                                                                                                     |
| AVDDx Current                                   |        |     | 6.3  |     | mA   | Analog peripherals in idle mode                                                                                                     |
| Digital Power Supply Current                    |        |     |      |     |      |                                                                                                                                     |
| IOVDDx Current in Normal Mode                   |        |     | 4    |     | mA   | All GPIO pull-up resistors enabled                                                                                                  |
| VDDx Current                                    |        |     |      |     |      |                                                                                                                                     |
| Normal Mode <sup>9</sup>                        |        |     | 29   |     | mA   | CD = 0 (80 MHz clock) executing typical code                                                                                        |
|                                                 |        |     | 20   |     | mA   | CD = 1 executing typical code                                                                                                       |
|                                                 |        |     | 10   |     | mA   | CD = 7 executing typical code                                                                                                       |
| CORE_SLEEP Mode <sup>9</sup>                    |        |     | 16   |     | mA   |                                                                                                                                     |
| SYS_SLEEP Mode <sup>9</sup>                     |        |     | 8    |     | mA   |                                                                                                                                     |
| Hibernate Mode <sup>9</sup>                     |        |     | 6.6  |     | mA   |                                                                                                                                     |
| Additional Power Supply Currents                |        |     |      |     |      |                                                                                                                                     |
| ADC                                             |        |     | 4.1  |     | mA   | Continuously converting at 100 kSPS                                                                                                 |
| ADC Input Buffer                                |        |     | 4.0  |     | mA   | Both buffers enabled                                                                                                                |
| IDAC                                            |        |     | 16.5 |     | mA   | Excluding load current                                                                                                              |
| DAC                                             |        |     | 340  |     | μA   | Per powered up DAC, excluding load current                                                                                          |
| Total Supply Current                            |        | 35  | 40   | 45  | mA   | VDD1, IOVDDx, AVDDx connected together; condition when entering user code: peripheral clocks on, peripherals idle, no load currents |
| Thermal Performance                             |        |     |      |     |      |                                                                                                                                     |
| Impedance Junction to Ambient                   |        |     | 45   |     | °C/W | JEDEC 2S2P                                                                                                                          |

<sup>1</sup> These numbers are not production tested but are guaranteed by design and/or characterization data at production release.

<sup>2</sup> Enabling the input buffer changes the ADC input characteristics as described in this subsection.

<sup>3</sup> The data in this section also applies for a load of  $R_L = 1 \text{ k}\Omega$  and  $C_L = 100 \text{ pF}$  to GND but only for 0 V to 2.5 V. However, this is not production tested.

<sup>4</sup> DAC linearity is calculated using a reduced code range of 100 to 3900.

<sup>5</sup> DAC gain error is calculated using a reduced code range of 100 to an internal 2.5 V  $V_{REF}$ .

<sup>6</sup> Due to self heating, internal temperature measurements cannot be used to predict external temperatures. This value is only relevant after user calibration and only for internal and external conditions identical to those at calibration.

<sup>7</sup> The average current from all GPIO pins must not exceed 3 mA per pin.

<sup>8</sup> Power figures exclude any load currents to external circuits.

<sup>9</sup> See the ADuCM320 reference manual, [How to Set up and Use the ADuCM320](#)

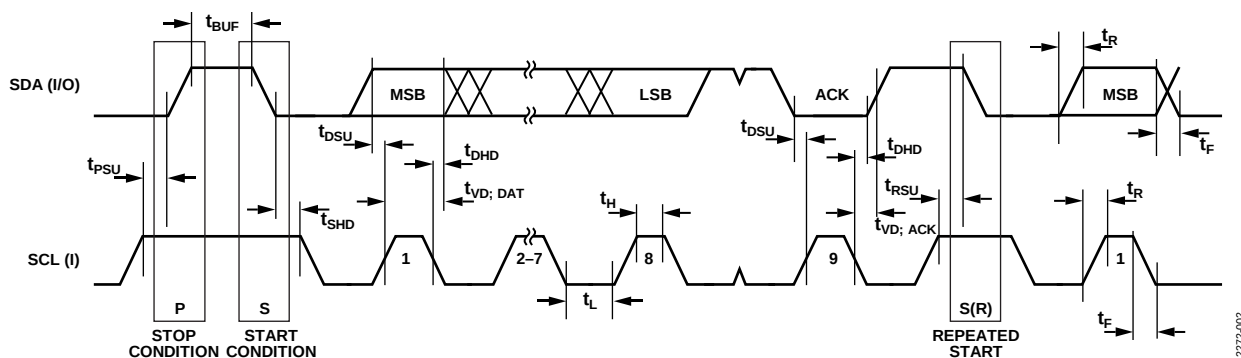
## TIMING SPECIFICATIONS

*I<sup>2</sup>C Timing*Table 3. I<sup>2</sup>C Timing in Standard Mode (100 kHz)

| Parameter     | Description                                                               | Slave |     |      | Unit    |
|---------------|---------------------------------------------------------------------------|-------|-----|------|---------|
|               |                                                                           | Min   | Typ | Max  |         |
| $t_L$         | SCL low pulse width                                                       | 4.7   |     |      | $\mu$ s |
| $t_H$         | SCL high pulse width                                                      | 4.0   |     |      | ns      |
| $t_{SHD}$     | Start condition hold time                                                 | 4.0   |     |      | $\mu$ s |
| $t_{DSU}$     | Data setup time                                                           | 250   |     |      | ns      |
| $t_{DHD}$     | Data hold time (SDA held internally for 300 ns after falling edge of SCL) | 0     |     | 3.45 | $\mu$ s |
| $t_{RSU}$     | Setup time for repeated start                                             | 4.7   |     |      | $\mu$ s |
| $t_{PSU}$     | Stop condition setup time                                                 | 4.0   |     |      | $\mu$ s |
| $t_{BUF}$     | Bus-free time between a stop condition and a start condition              | 4.7   |     |      | $\mu$ s |
| $t_R$         | Rise time for both SLC and SDA                                            |       |     | 1    | $\mu$ s |
| $t_F$         | Fall time for both SLC and SDA                                            |       | 15  | 300  | ns      |
| $t_{VD; DAT}$ | Data valid time                                                           |       |     | 3.45 | $\mu$ s |
| $t_{VD; ACK}$ | Data valid acknowledge time                                               |       |     | 3.45 | $\mu$ s |

Table 4. I<sup>2</sup>C Timing in Fast Mode (400 kHz)

| Parameter     | Description                                                               | Slave |     |     | Unit    |
|---------------|---------------------------------------------------------------------------|-------|-----|-----|---------|
|               |                                                                           | Min   | Typ | Max |         |
| $t_L$         | SCL low pulse width                                                       | 1.3   |     |     | $\mu$ s |
| $t_H$         | SCL high pulse width                                                      | 0.6   |     |     | ns      |
| $t_{SHD}$     | Start condition hold time                                                 | 0.3   |     |     | $\mu$ s |
| $t_{DSU}$     | Data setup time                                                           | 100   |     |     | ns      |
| $t_{DHD}$     | Data hold time (SDA held internally for 300 ns after falling edge of SCL) | 0     |     |     | $\mu$ s |
| $t_{RSU}$     | Setup time for repeated start                                             | 0.6   |     |     | $\mu$ s |
| $t_{PSU}$     | Stop condition setup time                                                 | 0.3   |     |     | $\mu$ s |
| $t_{BUF}$     | Bus-free time between a stop condition and a start condition              | 1.3   |     |     | $\mu$ s |
| $t_R$         | Rise time for both SCL and SDA                                            | 20    |     | 300 | ns      |
| $t_F$         | Fall time for both SCL and SDA                                            |       | 15  | 300 | ns      |
| $t_{VD; DAT}$ | Data valid time                                                           |       |     | 0.9 | $\mu$ s |
| $t_{VD; ACK}$ | Data valid acknowledge time                                               |       |     | 0.9 | $\mu$ s |

Figure 2. I<sup>2</sup>C Compatible Interface Timing

12272-002

**SPI Timing****Table 5. SPI Master Mode Timing (Phase Mode = 1)**

| Parameter | Description                            | Min | Typ                              | Max | Unit |
|-----------|----------------------------------------|-----|----------------------------------|-----|------|
| $t_{SL}$  | SCLK low pulse width                   |     | $(SPIDIV + 1) \times t_{HCLK}/2$ |     | ns   |
| $t_{SH}$  | SCLK high pulse width                  |     | $(SPIDIV + 1) \times t_{HCLK}/2$ |     | ns   |
| $t_{DAV}$ | Data output valid after SCLK edge      | 0   | 3                                |     | ns   |
| $t_{DSU}$ | Data input setup time before SCLK edge |     | $\frac{1}{2}$ SCLK               |     | ns   |
| $t_{DHD}$ | Data input hold time after SCLK edge   |     | SCLK                             |     | ns   |
| $t_{DF}$  | Data output fall time                  |     | SCLK                             |     | ns   |
| $t_{DR}$  | Data output rise time                  |     | 25                               |     | ns   |
| $t_{SR}$  | SCLK rise time                         |     | 25                               |     | ns   |
| $t_{SF}$  | SCLK fall time                         |     | 20                               |     | ns   |

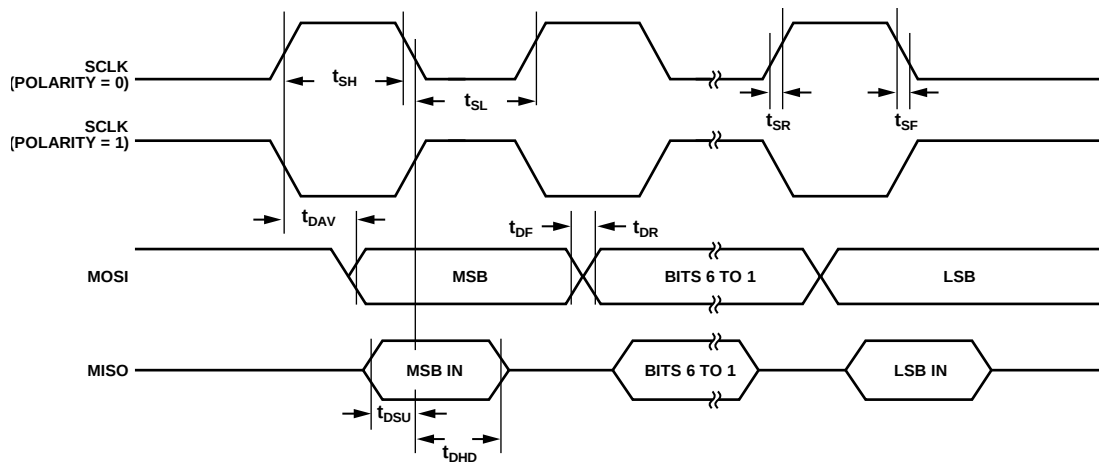


Figure 3. SPI Master Mode Timing (Phase Mode = 1)

12727-003

Table 6. SPI Master Mode Timing (Phase Mode = 0)

| Parameter  | Description                            | Min | Typ                              | Max | Unit |
|------------|----------------------------------------|-----|----------------------------------|-----|------|
| $t_{SL}$   | SCLK low pulse width                   |     | $(SPIDIV + 1) \times t_{HCLK}/2$ |     | ns   |
| $t_{SH}$   | SCLK high pulse width                  |     | $(SPIDIV + 1) \times t_{HCLK}/2$ |     | ns   |
| $t_{DAV}$  | Data output valid after SCLK edge      | 0   | 3                                |     | ns   |
| $t_{DOSU}$ | Data output setup before SCLK edge     |     | $\frac{1}{2}$ SCLK               |     | ns   |
| $t_{DSU}$  | Data input setup time before SCLK edge |     | SCLK                             |     | ns   |
| $t_{DHD}$  | Data input hold time after SCLK edge   |     | SCLK                             |     | ns   |
| $t_{DF}$   | Data output fall time                  |     | 25                               |     | ns   |
| $t_{DR}$   | Data output rise time                  |     | 25                               |     | ns   |
| $t_{SR}$   | SCLK rise time                         |     | 20                               |     | ns   |
| $t_{SF}$   | SCLK fall time                         |     | 20                               |     | ns   |

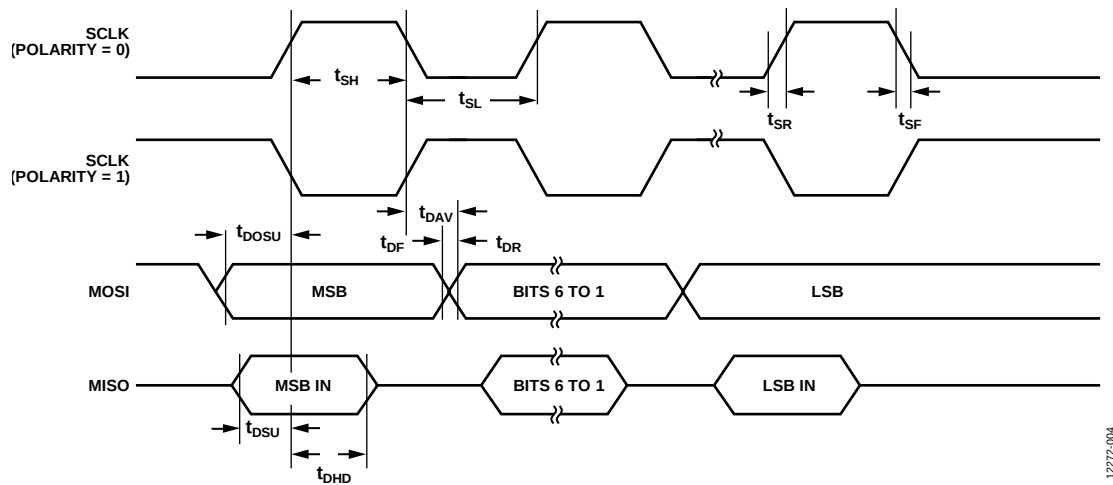


Figure 4. SPI Master Mode Timing (Phase Mode = 0)

12272-004

Table 7. SPI Slave Mode Timing (Phase Mode = 1)

| Parameter            | Description                                      | Min   | Typ                            | Max | Unit |
|----------------------|--------------------------------------------------|-------|--------------------------------|-----|------|
| $t_{\overline{CS}}$  | $\overline{CS}$ to SCLK edge                     | 10    |                                |     | ns   |
| $t_{\overline{CSM}}$ | $\overline{CS}$ high time between active periods | SCLKx |                                |     | ns   |
| $t_{SL}$             | SCLK low pulse width                             |       | $(SPIDIV + 1) \times t_{HCLK}$ |     | ns   |
| $t_{SH}$             | SCLK high pulse width                            |       | $(SPIDIV + 1) \times t_{HCLK}$ |     | ns   |
| $t_{DAV}$            | Data output valid after SCLK edge                |       | 20                             |     | ns   |
| $t_{DSU}$            | Data input setup time before SCLK edge           | 10    |                                |     | ns   |
| $t_{DHD}$            | Data input hold time after SCLK edge             | 10    |                                |     | ns   |
| $t_{DF}$             | Data output fall time                            |       | 25                             |     | ns   |
| $t_{DR}$             | Data output rise time                            |       | 25                             |     | ns   |
| $t_{SR}$             | SCLK rise time                                   | 1     |                                |     | ns   |
| $t_{SF}$             | SCLK fall time                                   | 1     |                                |     | ns   |
| $t_{SFS}$            | $\overline{CS}$ high after SCLK edge             | 20    |                                |     | ns   |

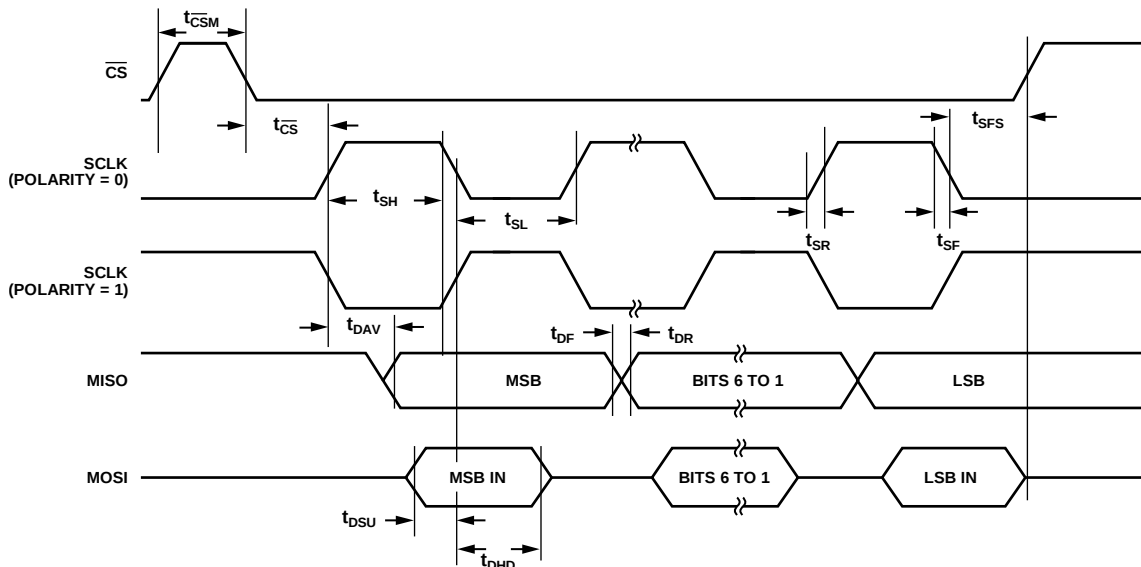


Figure 5. SPI Slave Mode Timing (Phase Mode = 1)

12272-005

Table 8. SPI Slave Mode Timing (Phase Mode = 0)

| Parameter            | Description                                      | Min   | Typ                            | Max | Unit |
|----------------------|--------------------------------------------------|-------|--------------------------------|-----|------|
| $t_{\overline{CS}}$  | $\overline{CS}$ to SCLK edge                     | 10    |                                |     | ns   |
| $t_{\overline{CSM}}$ | $\overline{CS}$ high time between active periods | SCLKx |                                |     | ns   |
| $t_{SL}$             | SCLK low pulse width                             |       | $(SPIDIV + 1) \times t_{HCLK}$ |     | ns   |
| $t_{SH}$             | SCLK high pulse width                            |       | $(SPIDIV + 1) \times t_{HCLK}$ |     | ns   |
| $t_{DAV}$            | Data output valid after SCLK edge                |       | 20                             |     | ns   |
| $t_{DSU}$            | Data input setup time before SCLK edge           | 10    |                                |     | ns   |
| $t_{DHD}$            | Data input hold time after SCLK edge             | 10    |                                |     | ns   |
| $t_{DF}$             | Data output fall time                            |       | 25                             |     | ns   |
| $t_{DR}$             | Data output rise time                            |       | 25                             |     | ns   |
| $t_{SR}$             | SCLK rise time                                   | 1     |                                |     | ns   |
| $t_{SF}$             | SCLK fall time                                   | 1     |                                |     | ns   |
| $t_{DOCS}$           | Data output valid after $\overline{CS}$ edge     | 20    |                                |     | ns   |
| $t_{SFS}$            | $\overline{CS}$ high after SCLK edge             | 10    |                                |     | ns   |

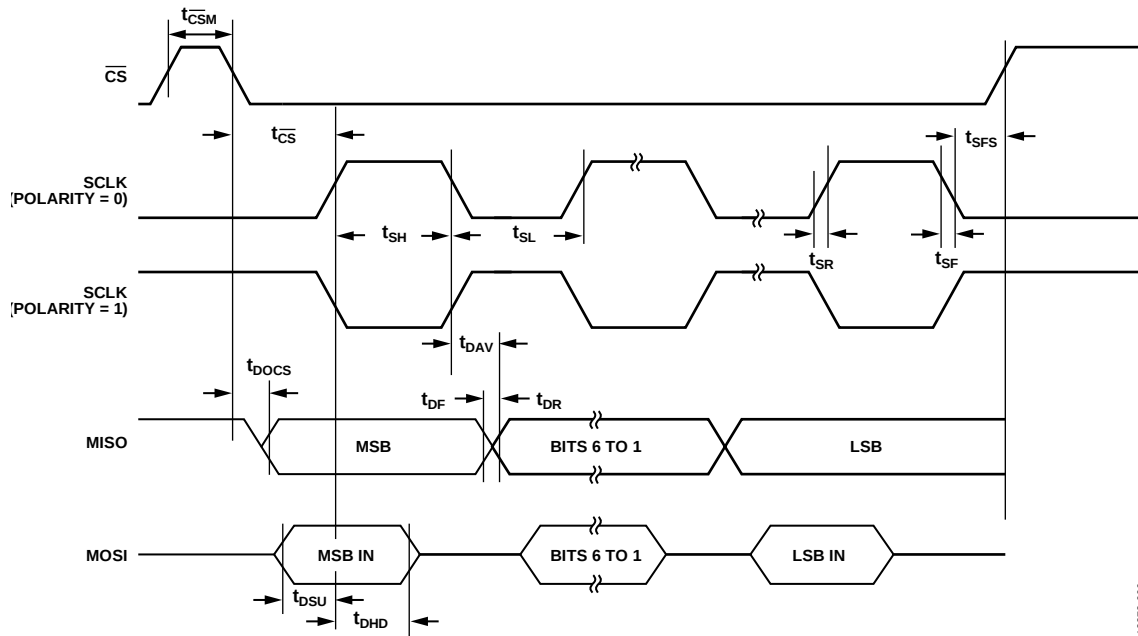


Figure 6. SPI Slave Mode Timing (Phase Mode = 0)

12272-006

Table 9. MDIO vs MDC Timing

| Parameter          | Description                | Min | Typ | Max | Unit |
|--------------------|----------------------------|-----|-----|-----|------|
| t <sub>SETUP</sub> | MDIO setup before MCK edge | 10  |     |     | ns   |
| t <sub>HOLD</sub>  | MDIO valid after MCK edge  | 10  |     |     | ns   |
| t <sub>DELAY</sub> | Data output after MCK edge |     |     | 100 | ns   |

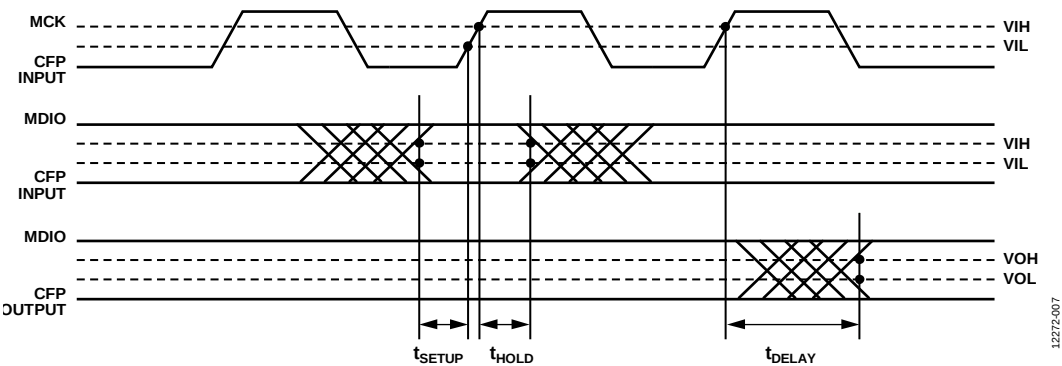


Figure 7. MDIO Timing

## ABSOLUTE MAXIMUM RATINGS

All requirements applicable to each pin must be met. Where multiple limits apply to a pin each one must be met individually. The limits apply according to the functionality of the pins at the time. Pins that can be either analog or digital, that is, that have two types indicated in the pin descriptions, must meet the limits for both types. For pin types, see Table 11.

When powered up, it is required that all ground pins plus ADC\_REFN be connected together to a node referred to as GND in Table 10. The limits that are listed must be reduced by any difference between any GNDs. Also, it is required that AVDD3 is connected to AVDD4 and that IOVDD1 to IOVDD3 are connected together.

**Table 10. Absolute Maximum Ratings**

| Parameter                                                   | Rating                   |
|-------------------------------------------------------------|--------------------------|
| Any Pin to GND                                              | −0.3 V to +3.9 V         |
| Any PVDDx Pin to GND                                        | −0.3 V to +2.8 V         |
| MDIO <sup>1</sup> , MCK, and PRTADDR0-4 in MDIO Mode to GND | −0.3 V to +2.1 V         |
| Between Any of AVDDx, IOVDDx, and VDD1 Pins                 | −0.3 V to +0.3 V         |
| Any Type I Pin to GND <sup>2</sup>                          | −0.3 V to IOVDDx + 0.3 V |
| Any Type AI or AO Pin to GND <sup>3</sup>                   | −0.3 V to AVDDx + 0.3 V  |
| Any IDACx, CDAMPx, IDACTST, IREF to GND                     | −0.3 V to PVDDx + 0.3 V  |
| ADC_REFP to GND                                             | −0.3 V to AVDDx + 0.3 V  |
| Total Positive GPIO Pin Currents                            | 0 mA to 30 mA            |
| Total Negative GPIO Pin Currents                            | −30 mA to 0 mA           |
| Maximum Power Dissipation                                   | 1 W                      |
| Operating Ambient Temperature Range                         | −40°C to +105°C          |
| Storage Temperature Range                                   | −65°C to +160°C          |
| Operating Junction Temperature Range                        | −40°C to +120°C          |
| ESD HBM                                                     | 2 kV                     |
| ESD FICDM                                                   | 1 kV                     |

<sup>1</sup> Note this pin is always in MDIO mode.

<sup>2</sup> This limit does not apply if no current can be drawn by external circuits on IOVDDx because then IOVDD follows to a suitable level.

<sup>3</sup> This limit does not apply if no current can be drawn by external circuits on AVDDx because then AVDD follows to a suitable level.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION



### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

|   | 1                          | 2                              | 3                                        | 4                                                                 | 5                                            | 6                         | 7                                    | 8                                    | 9                                          | 10                                      | 11                             |
|---|----------------------------|--------------------------------|------------------------------------------|-------------------------------------------------------------------|----------------------------------------------|---------------------------|--------------------------------------|--------------------------------------|--------------------------------------------|-----------------------------------------|--------------------------------|
| A | IDAC_TST                   | IDAC0                          | PVDD0                                    | PVDD2                                                             | IDAC2                                        | PGND                      | IDAC3                                | PVDD3                                | PVDD1                                      | IDAC1                                   | IREF                           |
| B | IOVDD1                     | RESET                          | P3.3/<br>PRTADDR3/<br>PLAI[15]           | CDAMP0                                                            | CDAMP2                                       | PGND                      | CDAMP3                               | CDAMP1                               | P1.0/SIN/<br>ECLKIN/<br>PLAI[4]            | P1.1/SOUT/<br>PLACK1/<br>PLAI[5]        | P1.2/<br>PWM0/<br>PLAI[6]      |
| C | IOGND1                     | P0.0/<br>SCLK0/<br>PLAI[0]     | P2.3/BM                                  | P2.2/<br>IRQ4/POR/<br>CLKOUT/<br>PLAI[10]                         | P2.0/IRQ2/<br>PWMTRIP/<br>PLACK2/<br>PLAI[8] | P1.3/<br>PWM1/<br>PLAI[7] | P1.4/<br>PWM2/<br>SCLK1/<br>PLAO[10] | P1.5/<br>PWM3/<br>MISO1/<br>PLAO[11] | P1.6/<br>PWM4/<br>MOSI1/<br>PLAO[12]       | P1.7/IRQ1/<br>PWM5/<br>CS1/<br>PLAO[13] | P3.4/<br>PRTADDR4/<br>PLAO[26] |
| D | P0.2/<br>MOSI0/<br>PLAI[2] | P0.1/<br>MISO0/<br>PLAI[1]     | P3.2/<br>PRTADDR2/<br>PLAI[14]           | <div>ADuCM320</div> <div>TOP VIEW</div> <div>(Not to Scale)</div> |                                              |                           |                                      |                                      | P2.4/IRQ5/<br>ADCONV/<br>PWM6/<br>PLAO[18] | DGND2                                   | IOVDD2                         |
| E | P0.5/<br>SDA0/<br>PLAO[3]  | P0.4/<br>SCL0/<br>PLAO[2]      | P0.3/<br>IRQ0/CS0/<br>PLACK0/<br>PLAI[3] |                                                                   |                                              |                           |                                      |                                      | SWCLK                                      | SWDIO                                   | IOGND2                         |
| F | P2.6/<br>IRQ7/<br>PLAO[20] | P0.7/<br>SDA1/<br>PLAO[5]      | P0.6/<br>SCL1/<br>PLAO[4]                |                                                                   |                                              |                           |                                      |                                      | AVDD_<br>REG0                              | AVDD_<br>REG1                           | VREF_1V2                       |
| G | P2.7/<br>IRQ8/<br>PLAO[21] | P3.1/<br>PRTADDR1/<br>PLAI[13] | P3.0/<br>PRTADDR0/<br>PLAI[12]           |                                                                   |                                              |                           |                                      |                                      | AIN15/<br>P4.7                             | AIN13/<br>P4.5                          | AVDD4                          |
| H | P3.5/<br>MCK/<br>PLAO[27]  | XTALO                          | MDIO                                     |                                                                   |                                              |                           |                                      |                                      | AIN14/<br>P4.6                             | AIN12/<br>P4.4                          | AGND4                          |
| J | IOVDD3                     | XTALI                          | VDAC7/<br>P5.2                           | VDAC4                                                             | AGND1                                        | AIN0                      | AIN1                                 | AIN2                                 | AIN7                                       | AIN10                                   | AIN11/<br>BUF_<br>VREF2V5      |
| K | IOGND3                     | DVDD_2V5                       | VDAC6/<br>P5.1                           | VDAC3/<br>P5.0                                                    | VDAC1                                        | VDD1                      | AGND2                                | AIN3                                 | AIN6                                       | AIN9/<br>P4.3                           | ADC_<br>REFP                   |
| L | DGND1                      | DVDD_1V8                       | VDAC5                                    | VDAC2/<br>P3.7/<br>PLAO[29]                                       | VDAC0/<br>P5.3                               | AVDD3                     | AGND3                                | AIN4                                 | AIN5                                       | AIN8/<br>P4.2                           | ADC_<br>REFN                   |

12272-008

Figure 8. Pin Configuration

Table 11. Pin Function Descriptions

| Pin No. | Mnemonic                     | Type <sup>1</sup> | Description                                                                                                                                                                                         |
|---------|------------------------------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B2      | RESET                        | I                 | Reset Input (Active Low). An internal pull-up resistor is included.                                                                                                                                 |
| C2      | P0.0/SCLK0/PLAI[0]           | I/O               | Digital I/O Port 0.0 (P0.0).<br>SPI0 Clock (SCLK0).<br>Input to PLA Element 0 (PLAI[0]).                                                                                                            |
| D2      | P0.1/MISO0/PLAI[1]           | I/O               | Digital I/O Port 0.1 (P0.1).<br>SPI0 Master In, Slave Out (MISO0).<br>Input to PLA Element 1 (PLAI[1]).                                                                                             |
| D1      | P0.2/MOSI0/PLAI[2]           | I/O               | Digital I/O Port 0.2 (P0.2).<br>SPI0 Master Out, Slave In (MOSI0).<br>Input to PLA Element 2 (PLAI[2]).                                                                                             |
| E3      | P0.3/IRQ0/CS0/PLACK0/PLAI[3] | I/O               | Digital I/O Port 0.3 (P0.3).<br>External Interrupt 0 (IRQ0).<br>SPI0 Chip Select 0 (CS0). When using SPI0, configure this pin as CS0.<br>PLA Clock 0 (PLACK0).<br>Input to PLA Element 3 (PLAI[3]). |
| E2      | P0.4/SCL0/PLAO[2]            | I/O               | Digital I/O Port 0.4 (P0.4).<br>I <sup>2</sup> C0 Serial Clock (SCL0).<br>Output of PLA Element 2 (PLAO[2]).                                                                                        |
| E1      | P0.5/SDA0/PLAO[3]            | I/O               | Digital I/O Port 0.5 (P0.5).<br>I <sup>2</sup> C0 Serial Data (SDA0).<br>Output of PLA Element 3 (PLAO[3]).                                                                                         |

| Pin No. | Mnemonic                                            | Type <sup>1</sup> | Description                                                                                                                                                                                                                                 |
|---------|-----------------------------------------------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F3      | P0.6/SCL1/PLAO[4]                                   | I/O               | Digital I/O Port 0.6 (P0.6).<br>I <sup>2</sup> C1 Serial Clock (SCL1).<br>Output of PLA Element 4 (PLAO[4]).                                                                                                                                |
| F2      | P0.7/SDA1/PLAO[5]                                   | I/O               | Digital I/O Port 0.7 (P0.7).<br>I <sup>2</sup> C1 Serial Data (SDA1).<br>Output of PLA Element 5 (PLAO[5]).                                                                                                                                 |
| B9      | P1.0/SIN/ECLKIN/PLAI[4]                             | I/O               | Digital I/O Port 1.0 (P1.0).<br>UART Input (SIN).<br>External Input Clock (ECLKIN).<br>Input to PLA Element 4 (PLAI[4]).                                                                                                                    |
| B10     | P1.1/SOUT/PLACK1/PLAI[5]                            | I/O               | Digital I/O Port 1.1 (P1.1).<br>UART Output (SOUT)<br>PLA Clock 1 (PLACK1).<br>Input to PLA Element 5 (PLAI[5]).                                                                                                                            |
| B11     | P1.2/PWM0/PLAI[6]                                   | I/O               | Digital I/O Port 1.2 (P1.2).<br>PWM Output 0 (PWM0).<br>Input to PLA Element 6 (PLAI[6]).                                                                                                                                                   |
| C6      | P1.3/PWM1/PLAI[7]                                   | I/O               | Digital I/O Port 1.3 (P1.3).<br>PWM Output 1 (PWM1).<br>Input to PLA Element 7 (PLAI[7]).                                                                                                                                                   |
| C7      | P1.4/PWM2/SCLK1/PLAO[10]                            | I/O               | Digital I/O Port 1.4 (P1.4).<br>PWM Output 2 (PWM2).<br>SPI1 Clock (SCLK1).<br>Output of PLA Element 10 (PLAO[10]).                                                                                                                         |
| C8      | P1.5/PWM3/MISO1/PLAO[11]                            | I/O               | Digital I/O Port 1.5 (P1.5).<br>PWM Output 3 (PWM3).<br>SPI1 Master In, Slave Out (MISO1).<br>Output of PLA Element 11 (PLAO[11]).                                                                                                          |
| C9      | P1.6/PWM4/MOSI1/PLAO[12]                            | I/O               | Digital I/O Port 1.6 (P1.6).<br>PWM Output 4 (PWM4).<br>SPI1 Master Out, Slave Input (MOSI1).<br>Output of PLA Element 12 (PLAO[12]).                                                                                                       |
| C10     | P1.7/IRQ1/PWM5/CS1/PLAO[13]                         | I/O               | Digital I/O Port 1.7 (P1.7).<br>External Interrupt 1 (IRQ1).<br>PWM Output 5 (PWM5).<br>SPI1 Chip Select 1 (CS1). When using SPI1, configure this pin as CS1.<br>Output of PLA Element 13 (PLAO[13]).                                       |
| C5      | P2.0/IRQ2/PWMTRIP/PLACK2/PLAI[8]                    | I/O               | Digital I/O Port 2.0 (P2.0).<br>External Interrupt 2 (IRQ2).<br>PWM Trip (PWMTRIP).<br>PLA Input Clock 2 (PLACK2).<br>Input to PLA Element 8 (PLAI[8]).                                                                                     |
| C4      | P2.2/IRQ4/ $\overline{\text{POR}}$ /CLKOUT/PLAI[10] | I/O               | Digital I/O Port 2.2 (P2.2).<br>External Interrupt 4 (IRQ4).<br>Reset Output ( $\overline{\text{POR}}$ ). This pin function is an output and it is the default for Pin C4.<br>Clock Output (CLKOUT).<br>Input to PLA Element 10 (PLAI[10]). |
| C3      | P2.3/BM                                             | I/O               | Digital I/O Port 2.3 (P2.3).<br>Boot Mode (BM). This pin determines the start-up sequence after every reset.<br>Pull-up is enabled at power-up.                                                                                             |

| Pin No. | Mnemonic                        | Type <sup>1</sup> | Description                                                                                                                                                                        |
|---------|---------------------------------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D9      | P2.4/IRQ5/ADCCONV/PWM6/PLAO[18] | I/O               | Digital I/O Port 2.4 (P2.4).<br>External Interrupt 5 (IRQ5).<br>External Input to Start ADC Conversions (ADCCONV).<br>PWM Output 6 (PWM6).<br>Output of PLA Element 18 (PLAO[18]). |
| F1      | P2.6/IRQ7/PLAO[20]              | I/O               | Digital I/O Port 2.6 (P2.6).<br>External Interrupt 7 (IRQ7).<br>Output of PLA Element 20 (PLAO[20]).                                                                               |
| G1      | P2.7/IRQ8/PLAO[21]              | I/O               | Digital I/O Port 2.7 (P2.7).<br>External Interrupt 8 (IRQ8).<br>Output of PLA Element 21 (PLAO[21]).                                                                               |
| G3      | P3.0/PRTADDR0/PLAI[12]          | I/O               | Digital I/O Port 3.0 (P3.0).<br>MDIO Port Address Bit 0 (PRTADDR0). See the digital inputs parameter in Table 1 for details.<br>Input to PLA Element 12 (PLAI[12]).                |
| G2      | P3.1/PRTADDR1/PLAI[13]          | I/O               | Digital I/O Port 3.1 (P3.1).<br>MDIO Port Address Bit 1 (PRTADDR1). See the digital inputs parameter in Table 1 for details.<br>Input to PLA Element 13 (PLAI[13]).                |
| D3      | P3.2/PRTADDR2/PLAI[14]          | I/O               | Digital I/O Port 3.2 (P3.2).<br>MDIO Port Address Bit 2 (PRTADDR2). See the digital inputs parameter in Table 1 for details.<br>Input to PLA Element 14 (PLAI[14]).                |
| B3      | P3.3/PRTADDR3/PLAI[15]          | I/O               | Digital I/O Port 3.3 (P3.3).<br>MDIO Port Address Bit 3 (PRTADDR3). See the digital inputs parameter in Table 1 for details.<br>Output of PLA Element 15 (PLAI[15]).               |
| C11     | P3.4/PRTADDR4/PLAO[26]          | I/O               | Digital I/O Port 3.4 (P3.4).<br>MDIO Port Address Bit 4 (PRTADDR4). See the digital inputs parameter in Table 1 for details.<br>Output of PLA Element 26 (PLAO[26]).               |
| H1      | P3.5/MCK/PLAO[27]               | I/O               | Digital I/O Port 3.5 (P3.5).<br>MDIO Clock (MCK) See the digital inputs parameter in Table 1 for more details.<br>Output of PLA Element 27 (PLAO[27]).                             |
| H3      | MDIO                            | I/O               | MDIO Data.                                                                                                                                                                         |
| E9      | SWCLK                           | I                 | Serial Wire Debug Clock.                                                                                                                                                           |
| E10     | SWDIO                           | I/O               | Serial Wire Bidirectional Data.                                                                                                                                                    |
| F11     | VREF_1V2                        | S                 | 1.2 V Reference. This pin cannot be used to source current externally. Connect VREF_1V2 to AGNDx via a 470 nF capacitor.                                                           |
| A11     | IREF                            | AI                | IDAC Reference Current. This pin generates the reference current for the IDACs and is set by an external resistor, R <sub>EXT</sub> . Connect R <sub>EXT</sub> from IREF to AGND4. |
| J6      | AIN0                            | AI                | Analog Input 0.                                                                                                                                                                    |
| J7      | AIN1                            | AI                | Analog Input 1.                                                                                                                                                                    |
| J8      | AIN2                            | AI                | Analog Input 2.                                                                                                                                                                    |
| K8      | AIN3                            | AI                | Analog Input 3.                                                                                                                                                                    |
| L8      | AIN4                            | AI                | Analog Input 4.                                                                                                                                                                    |
| L9      | AIN5                            | AI                | Analog Input 5. AIN5 can be the –ve input for the comparator.                                                                                                                      |
| K9      | AIN6                            | AI                | Analog Input 6. AIN6 is also the +ve input for the comparator.                                                                                                                     |
| J9      | AIN7                            | AI                | Analog Input 7.                                                                                                                                                                    |
| L10     | AIN8/P4.2                       | AI/I/O            | Analog Input 8 (AIN8).<br>Digital I/O Port 4.2 (P4.2).                                                                                                                             |
| K10     | AIN9/P4.3                       | AI/I/O            | Analog Input 9 (AIN9).<br>Digital I/O Port 4.3 (P4.3).                                                                                                                             |
| J10     | AIN10                           | AI                | Analog Input 10.                                                                                                                                                                   |

| Pin No. | Mnemonic            | Type <sup>1</sup> | Description                                                                                                                                                                           |
|---------|---------------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| J11     | AIN11/BUF_VREF2V5   | AI/AO             | Analog Input 11 (AIN11).<br>Buffered 2.5 V Bias (BUF_VREF2V5). The maximum load = 1.2 mA. Connect BUF_VREF2V5 to AGNDx via a 100 nF capacitor.                                        |
| H10     | AIN12/P4.4          | AI/I/O            | Analog Input 12 (AIN12).<br>Digital I/O Port 4.4 (P4.4).                                                                                                                              |
| G10     | AIN13/P4.5          | AI/I/O            | Analog Input 13 (AIN13).<br>Digital I/O Port 4.5 (P4.5).                                                                                                                              |
| H9      | AIN14/P4.6          | AI/I/O            | Analog Input 14 (AIN14).<br>Digital I/O Port 4.6 (P4.6).                                                                                                                              |
| G9      | AIN15/P4.7          | AI/I/O            | Analog Input 15 (AIN15).<br>Digital I/O Port 4.7 (P4.7).                                                                                                                              |
| L5      | VDAC0/P5.3          | AO/I/O            | Voltage DAC0 Output (VDAC0).<br>Digital I/O Port 5.3 (P5.3).                                                                                                                          |
| K5      | VDAC1               | AO                | Voltage DAC1 Output.                                                                                                                                                                  |
| L4      | VDAC2/P3.7/PLAO[29] | AO/I/O            | Voltage DAC2 Output (VDAC2).<br>Digital I/O Port 3.7 (P3.7).<br>Output of PLA Element 29 (PLAO[29]).                                                                                  |
| K4      | VDAC3/P5.0          | AO/I/O            | Voltage DAC3 Output (VDAC3).<br>Digital I/O Port 5.0 (P5.0).                                                                                                                          |
| J4      | VDAC4               | AO                | Voltage DAC4 Output (VDAC4).                                                                                                                                                          |
| L3      | VDAC5               | AO                | Voltage DAC5 Output (VDAC5).                                                                                                                                                          |
| K3      | VDAC6/P5.1          | AO/I/O            | Voltage DAC6 Output (VDAC6).<br>Digital I/O Port 5.1 (P5.1).                                                                                                                          |
| J3      | VDAC7/P5.2          | AO/I/O            | Voltage DAC7 Output (VDAC7).<br>Digital I/O Port 5.2 (P5.2).                                                                                                                          |
| A2      | IDAC0               | AO                | IDAC0. 0 mA to 150 mA full-scale output.                                                                                                                                              |
| A3      | PVDD0               | S                 | Power for IDAC0.                                                                                                                                                                      |
| B4      | CDAMP0              | AI                | Damping Capacitor 0. Connect damping capacitor from this pin to PVDD0.                                                                                                                |
| A10     | IDAC1               | AO                | IDAC1. 0 mA to 150 mA full-scale output.                                                                                                                                              |
| A9      | PVDD1               | S                 | Power for IDAC1.                                                                                                                                                                      |
| B8      | CDAMP1              | AI                | Damping Capacitor 1. Connect damping capacitor from this pin to PVDD1.                                                                                                                |
| A5      | IDAC2               | AO                | IDAC2. 0 mA to 150 mA full-scale output.                                                                                                                                              |
| A4      | PVDD2               | S                 | Power for IDAC2.                                                                                                                                                                      |
| B5      | CDAMP2              | AI                | Damping Capacitor 2. Connect damping capacitor from this pin to PVDD2.                                                                                                                |
| A7      | IDAC3               | AO                | IDAC3. 0 mA to 150 mA full-scale output.                                                                                                                                              |
| A8      | PVDD3               | S                 | Power for IDAC3.                                                                                                                                                                      |
| B7      | CDAMP3              | AI                | Damping Capacitor 3. Connect damping capacitor from this pin to PVDD3.                                                                                                                |
| B6      | PGND                | S                 | Power Supply Ground for IDACs.                                                                                                                                                        |
| A6      | PGND                | S                 | Power Supply Ground for IDACs.                                                                                                                                                        |
| A1      | IDAC_TST            | AI/AO             | Pin for IDAC Test Purposes. Leave IDAC_TST unconnected.                                                                                                                               |
| L2      | DVDD_1V8            | AO                | 1.8 V Digital Supply. A 470 nF capacitor to DGND1 must be connected to this pin to stabilize the internal 1.8 V regulator that supplies flash memory and the ARM Cortex-M3 processor. |
| K2      | DVDD_2V5            | AO                | 2.5 V Digital Supply. A 470 nF capacitor to IOGND3 must be connected to this pin to stabilize the internal 2.5 V regulator that supplies the analog digital control.                  |
| F9      | AVDD_REG0           | AO                | Analog Regulator 0 Supply. A 470 nF capacitor to AGND4 must be connected to this pin to stabilize the internal 2.5 V regulator that supplies the ADC.                                 |
| F10     | AVDD_REG1           | AO                | Analog Regulator 1 Supply. Output of 2.5 V on-chip LDO regulator. A 470 nF capacitor to AGND4 must be connected to this pin. This regulator supplies the IDACs.                       |
| L1      | DGND1               | S                 | Digital Ground 1 for DVDD_1V8.                                                                                                                                                        |
| D10     | DGND2               | S                 | Digital Ground 2. Connect to DGND1.                                                                                                                                                   |
| B1      | IOVDD1              | S                 | 3.3 V GPIO Supply.                                                                                                                                                                    |

| Pin No. | Mnemonic | Type <sup>1</sup> | Description                                                                                                                                                                     |
|---------|----------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D11     | IOVDD2   | S                 | 3.3 V GPIO Supply and Interdie Communications.                                                                                                                                  |
| J1      | IOVDD3   | S                 | 3.3 V GPIO Supply.                                                                                                                                                              |
| C1      | IOGND1   | S                 | Ground for IOVDD1.                                                                                                                                                              |
| E11     | IOGND2   | S                 | Ground for IOVDD2.                                                                                                                                                              |
| K1      | IOGND3   | S                 | Ground for IOVDD3 and Interdie Communications.                                                                                                                                  |
| J5      | AGND1    | S                 | Analog Ground for VDD1.                                                                                                                                                         |
| K7      | AGND2    | S                 | ESD Ground for Pad Ring.                                                                                                                                                        |
| L7      | AGND3    | S                 | Ground for AVDD3.                                                                                                                                                               |
| H11     | AGND4    | S                 | Ground for AVDD4, AVDD_REG0, and AVDD_REG1.                                                                                                                                     |
| K6      | VDD1     | S                 | 3.3 V Supply for Digital Die.                                                                                                                                                   |
| L6      | AVDD3    | S                 | VDAC and IDAC Supply (3.3 V).                                                                                                                                                   |
| G11     | AVDD4    | S                 | ADC Supply (3.3 V).                                                                                                                                                             |
| L11     | ADC_REFN | AO/A              | Decoupling Capacitor Connection for ADC Reference Buffer. Connect this pin to AGND4.                                                                                            |
| K11     | ADC_REFP | AO/A              | Decoupling Capacitor Connection for ADC Reference Buffer. Connect this pin to a 4.7 $\mu$ F capacitor to the ADC_REFN pin. ADC_REFP can be overdriven by an external reference. |
| H2      | XTALO    | O                 | Output from the Crystal Oscillator Inverter. When not using an external crystal, leave XTALO unconnected.                                                                       |
| J2      | XTALI    | I                 | Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits. When not using an external crystal, connect XTALI to DGND.                         |

<sup>1</sup> AI is analog input, AO is analog output, I is digital input, O is digital output, S is supply.

## TYPICAL PERFORMANCE CHARACTERISTICS

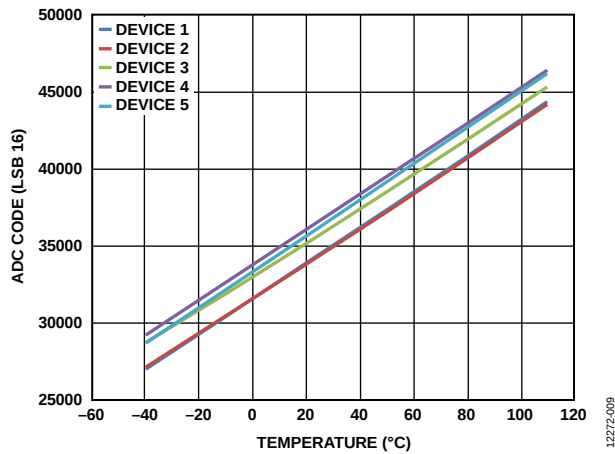


Figure 9. Typical Temperature Measurement vs. Internal Temperature  
( $V_{DD} = 3.3\text{ V}$ , 50 kSPS)

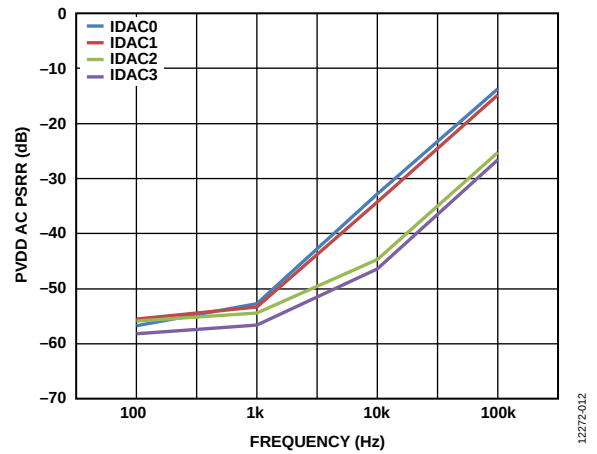


Figure 12. Typical PVDD AC PSRR vs. Frequency

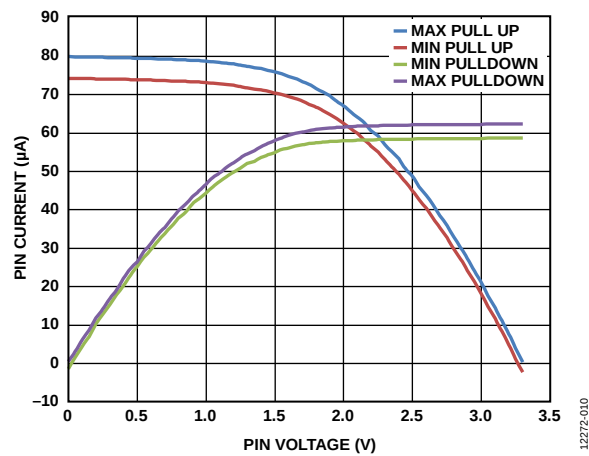


Figure 10. Typical Pull-Up/Pull-Down Pin Current vs. Pin Voltage  
( $V_{DD} = 3.3\text{ V}$ , 25°C)

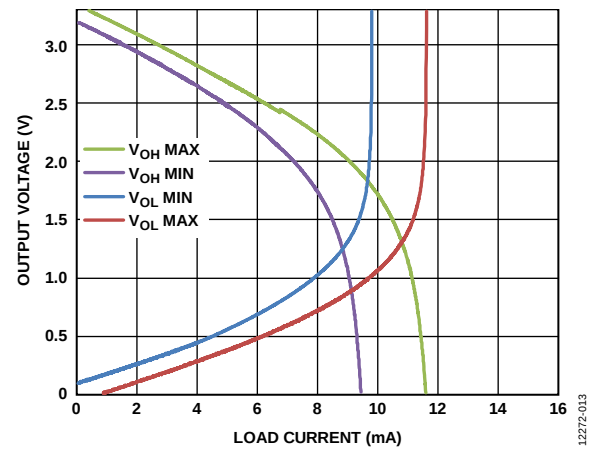


Figure 13. Typical Output Voltage vs. Load Current

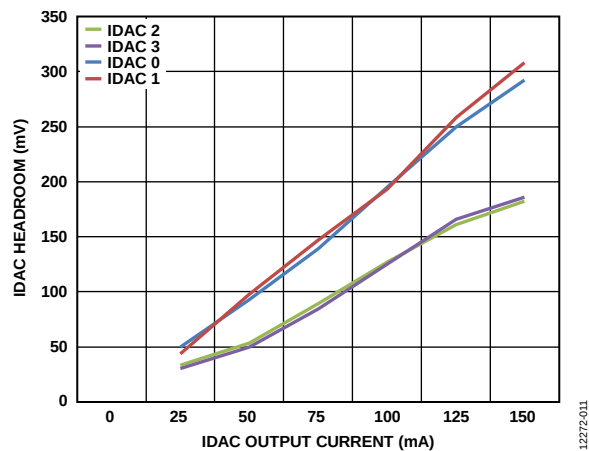


Figure 11. Typical IDAC Headroom vs. IDAC Output Current

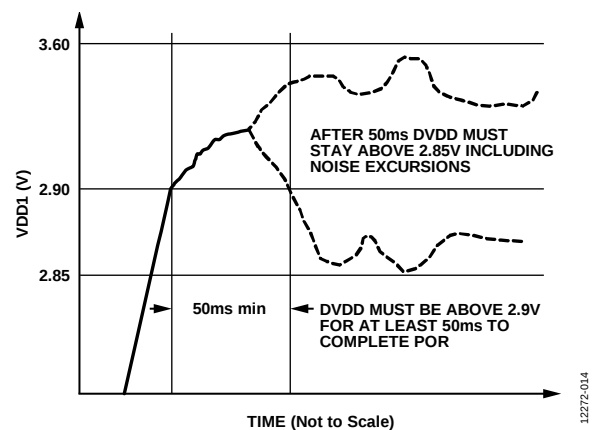


Figure 14. VDD1 Power-On Requirements

## RECOMMENDED CIRCUIT AND COMPONENT VALUES

Figure 15 shows a typical connection diagram for the [ADuCM320](#).

Supplies and regulators must be adequately decoupled with capacitors connected between the AVDDx, PVDDx, DVDD\_x, AVDD\_REGx, IOVDDx, and VDD1 balls and their associated GND balls (AGNDx, PGND, IOGNDx, and DGNDx). Table 11 indicates which ground balls are paired with which supply balls.

There are four digital supply balls, IOVDD1, IOVDD2, IOVDD3, and VDD1. Decouple these balls with a 100 nF capacitor placed as near as possible to each of the four balls and their associated GND balls (IOGNDx and AGND1, respectively). In addition, place a 10  $\mu$ F capacitor conveniently near to these balls.

Similarly, the analog supply pins, AVDD3 and AVDD4, each require a 100 nF capacitor placed as near as possible to each ball and its associated AGNDx ball, and place a 10  $\mu$ F capacitor conveniently near to these balls.

The IDACs source their output currents from the PVDDx supply balls. Each PVDDx supply ball must have a 100 nF capacitor near to each ball and their associated GND balls (PGND). In addition, place at least one 10  $\mu$ F capacitor at the source of the PVDDx supply.

The IDAC output filters depend on a 10 nF capacitor being placed between the CDAMPx and PVDDx.

The ADC reference requires a 4.7  $\mu$ F capacitor placed between ADC\_REFP and ADC\_REFN and located as near as possible to each ball. ADC\_REFN must be connected directly to AGND4.

The [ADuCM320](#) contains four internal regulators. These regulators require external decoupling capacitors. The DVDD\_1V8 and DVDD\_2V5 balls each require a 470 nF capacitor to DGND1 and IOGND3, respectively. AVDD\_REG0 and AVDD\_REG1 each require a decoupling capacitor to AGND4.

To generate an accurate and low drift reference current, connect the IREF ball to AGND4 via a low ppm 3.16 k $\Omega$  resistor.

Take care in the layout to ensure that currents flowing from the ground end of each decoupling capacitor to its associated ground ball share as little track as possible with other ground currents on the printed circuit board.

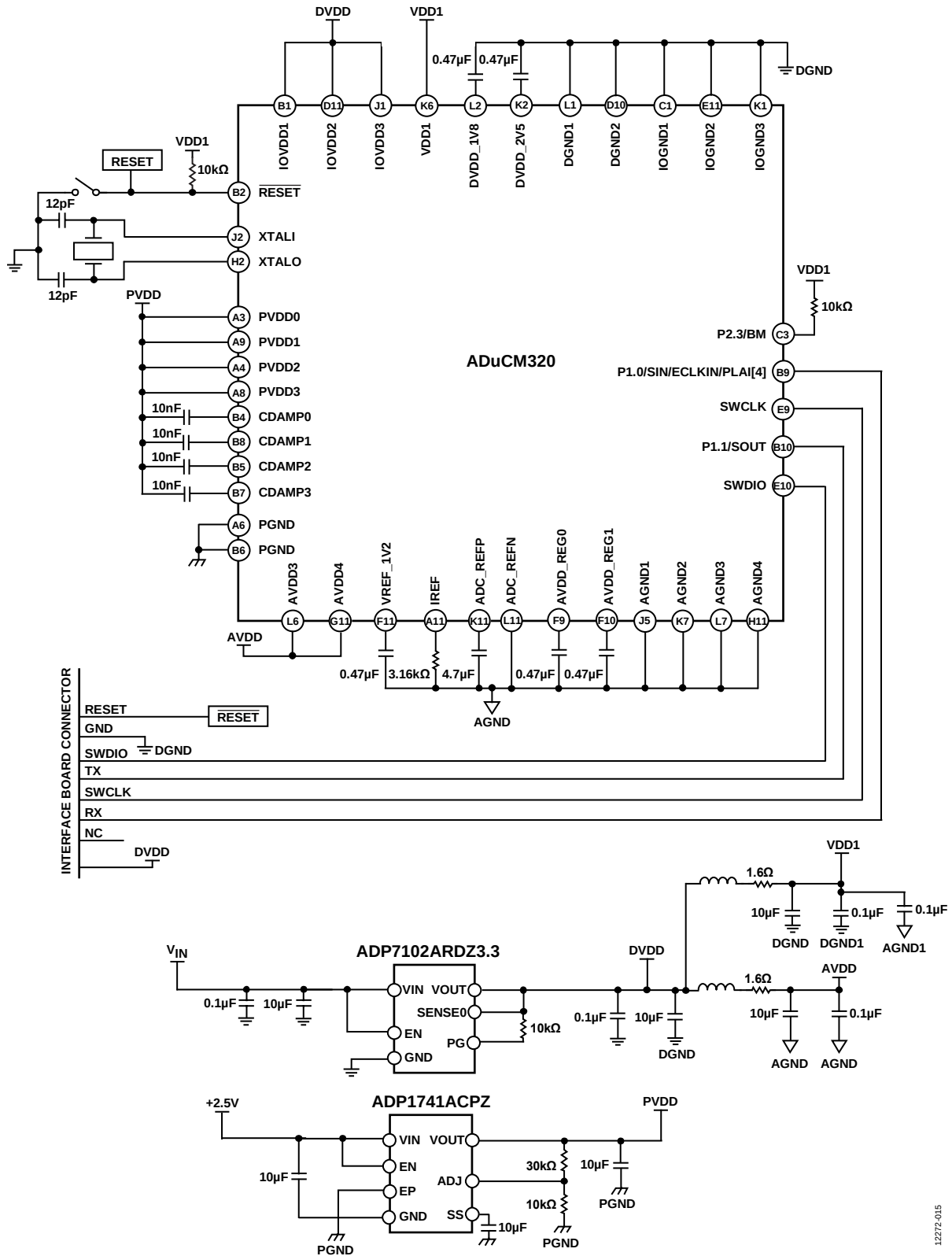
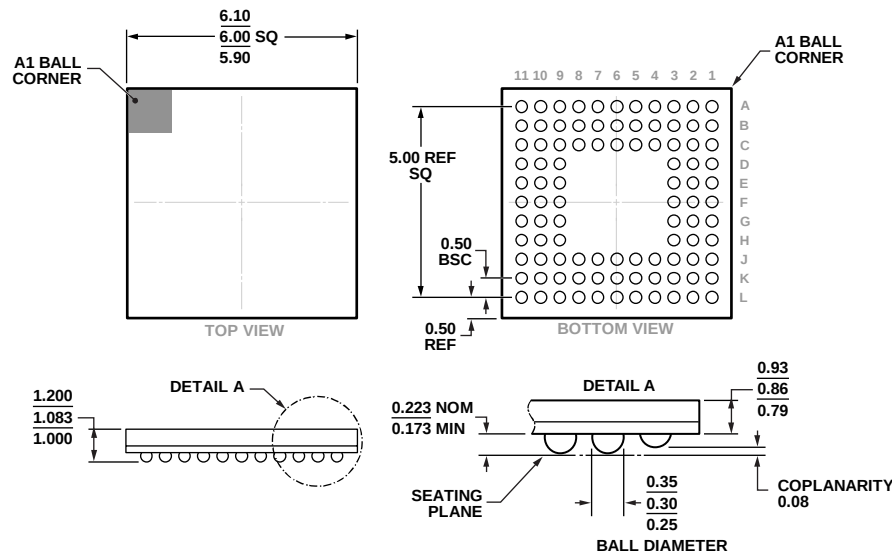


Figure 15. Recommended Circuit and Component Values

12272-015

## PACKAGING AND ORDERING INFORMATION

### OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-195-AC  
WITH THE EXCEPTION TO BALL COUNT.

Figure 16. 96-Ball Chip Scale Package Ball Grid Array [CSP\_BGA]  
(BC-96-2)

Dimensions shown in millimeters

04-02-2013-A

### ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                                  | Package Option | Ordering Quantity |
|--------------------|-------------------|------------------------------------------------------|----------------|-------------------|
| ADuCM320BBCZ       | −40°C to +105°C   | 96-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-96-2        | 429               |
| ADuCM320BBCZ-RL    | −40°C to +105°C   | 96-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-96-2        | 2,500             |
| EV-ADuCM320QSPZ    |                   | Evaluation Board with QuickStart Development System  |                | 1                 |

<sup>1</sup> Z = RoHS Compliant Part.

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).