



MAY 2015

FQB1P50 P-Channel QFET[®] MOSFET

FQB1P50

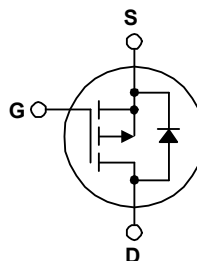
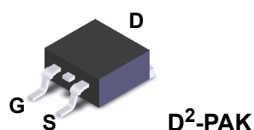
P-Channel QFET[®] MOSFET - 500 V, - 1.5 A, 10.5 Ω

Description

This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- - 1.5 A, - 500 V, $R_{DS(on)} = 10.5 \Omega$ (Max.) @ $V_{GS} = -10$ V, $I_D = -0.75$ A
- Low Gate Charge (Typ. 11 nC)
- Low C_{rss} (Typ. 6.0 pF)
- 100% Avalanche Tested
- RoHS Compliant



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQB1P50TM	Unit
V_{DSS}	Drain-Source Voltage	-500	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	-1.5	A
	- Continuous ($T_C = 100^\circ\text{C}$)	-0.95	A
I_{DM}	Drain Current - Pulsed (Note 1)	-6.0	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	110	mJ
I_{AR}	Avalanche Current (Note 1)	-1.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	6.3	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-4.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	3.13	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	63	W
	- Derate above 25°C	0.51	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FQB1P50TM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	1.98	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (1 in ² pad of 2 oz copper), Max.	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB1P50	FQB1P50TM	D2-PAK	330mm	24mm	800

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	--	-	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -500\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	μA
		$V_{DS} = -400\text{ V}, T_C = 125^\circ\text{C}$	--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -0.75\text{ A}$	--	8.0	10.5	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -50\text{ V}, I_D = -0.75\text{ A}$	--	1.26	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	270	350	pF
C_{oss}	Output Capacitance		--	40	50	pF
C_{rss}	Reverse Transfer Capacitance		--	6.0	8.0	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -250\text{ V}, I_D = -1.5\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4)	--	9.0	30	ns
t_r	Turn-On Rise Time		--	25	60	ns
$t_{d(off)}$	Turn-Off Delay Time		--	27	65	ns
t_f	Turn-Off Fall Time		--	30	70	ns
Q_g	Total Gate Charge	$V_{DS} = -400\text{ V}, I_D = -1.5\text{ A},$ $V_{GS} = -10\text{ V}$ (Note 4)	--	11	14	nC
Q_{gs}	Gate-Source Charge		--	2.0	--	nC
Q_{gd}	Gate-Drain Charge		--	5.6	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

Drain-Source Diode Characteristics and Maximum Ratings					
I _S	Maximum Continuous Drain-Source Diode Forward Current	--	--	-1.5	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-6.0	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -1.5 A		--	--
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = -1.5 A, dI _F / dt = 100 A/μs		--	200
Q _{rr}	Reverse Recovery Charge			--	0.7
				--	--

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 88\text{ mH}$, $I_{AS} = -1.5\text{ A}$, $V_{DD} = -50\text{ V}$, $R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq -1.5\text{ A}$, $dI/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature

Typical Characteristics

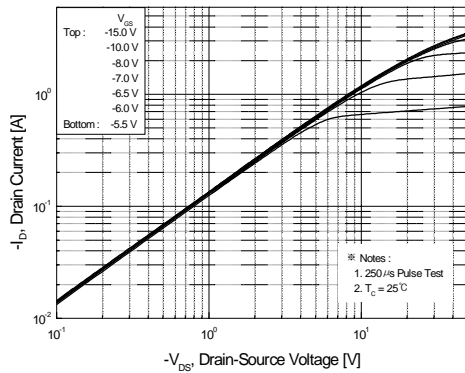


Figure 1. On-Region Characteristics

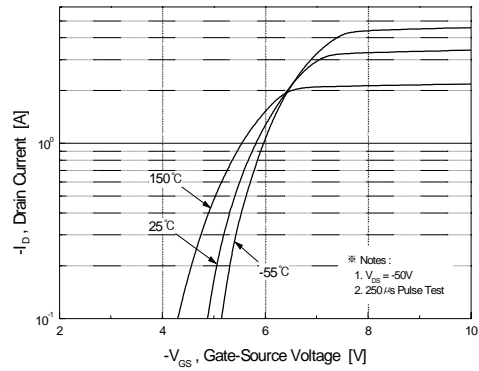


Figure 2. Transfer Characteristics

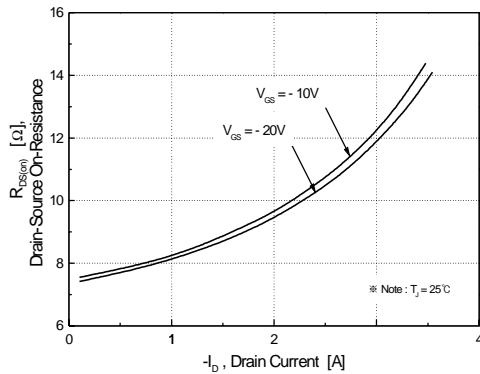


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

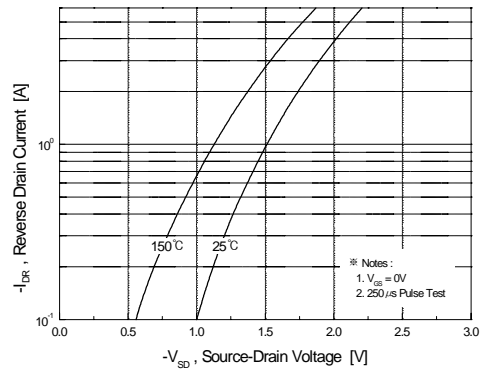


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

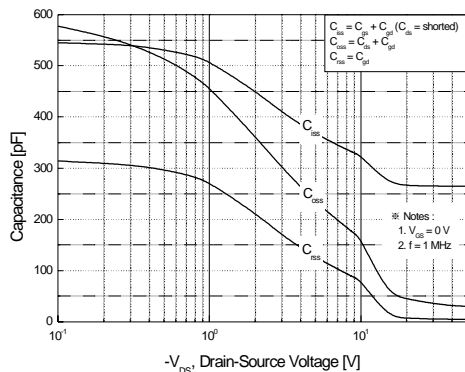


Figure 5. Capacitance Characteristics

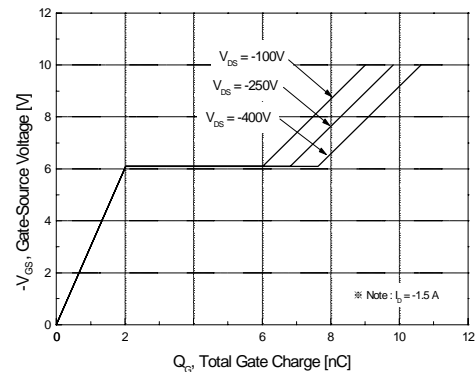


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

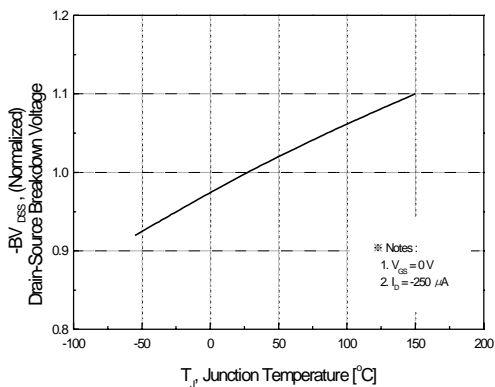


Figure 7. Breakdown Voltage Variation vs. Temperature

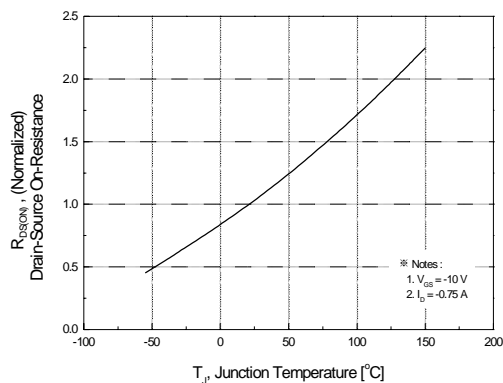


Figure 8. On-Resistance Variation vs. Temperature

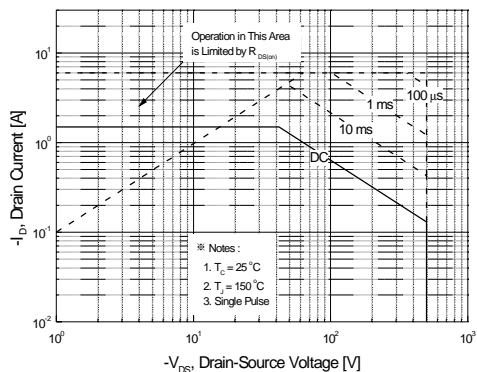


Figure 9. Maximum Safe Operating Area

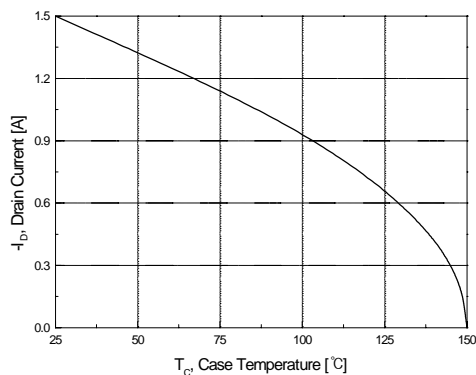


Figure 10. Maximum Drain Current vs. Case Temperature

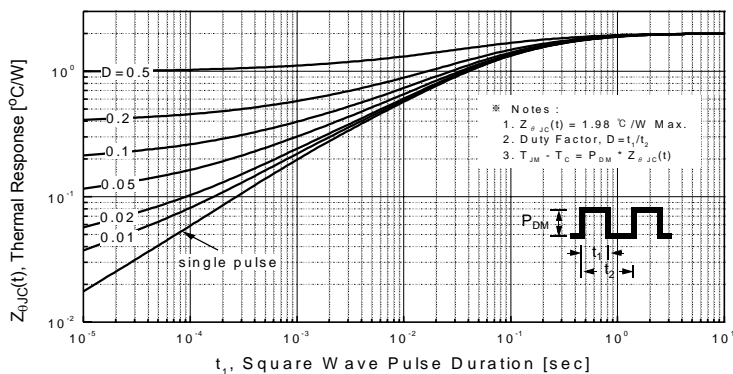


Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

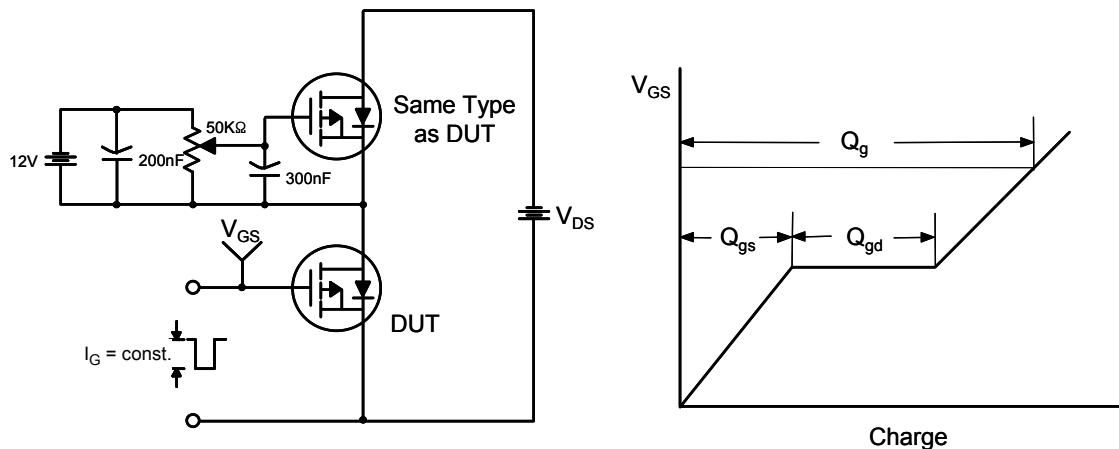


Figure 13. Resistive Switching Test Circuit & Waveforms

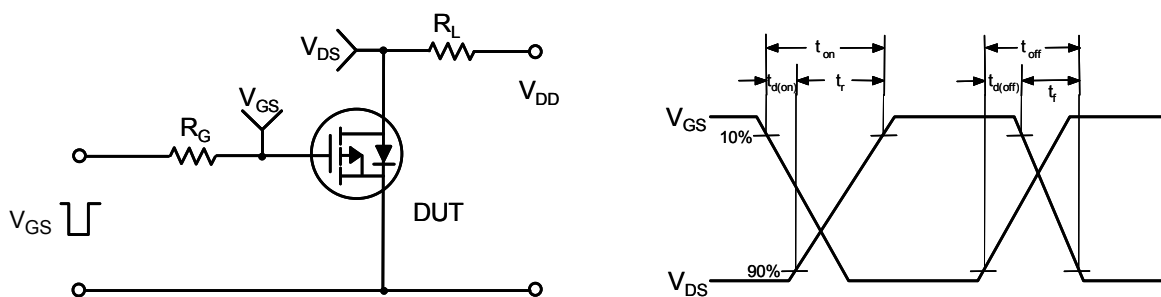


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

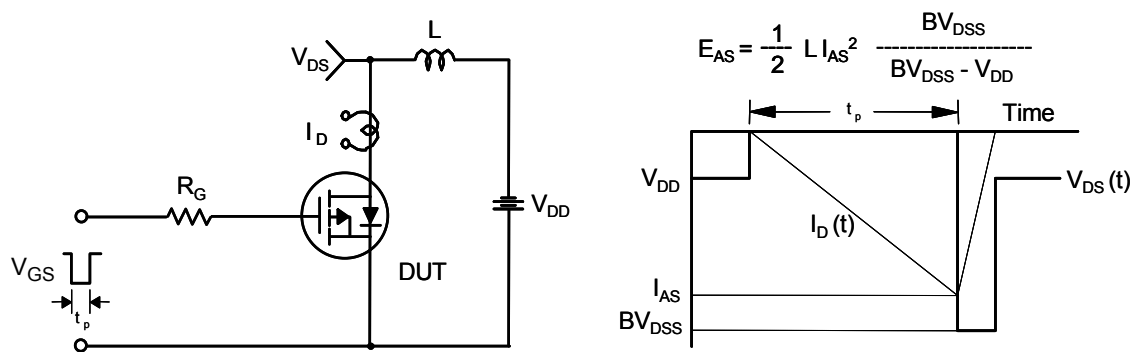
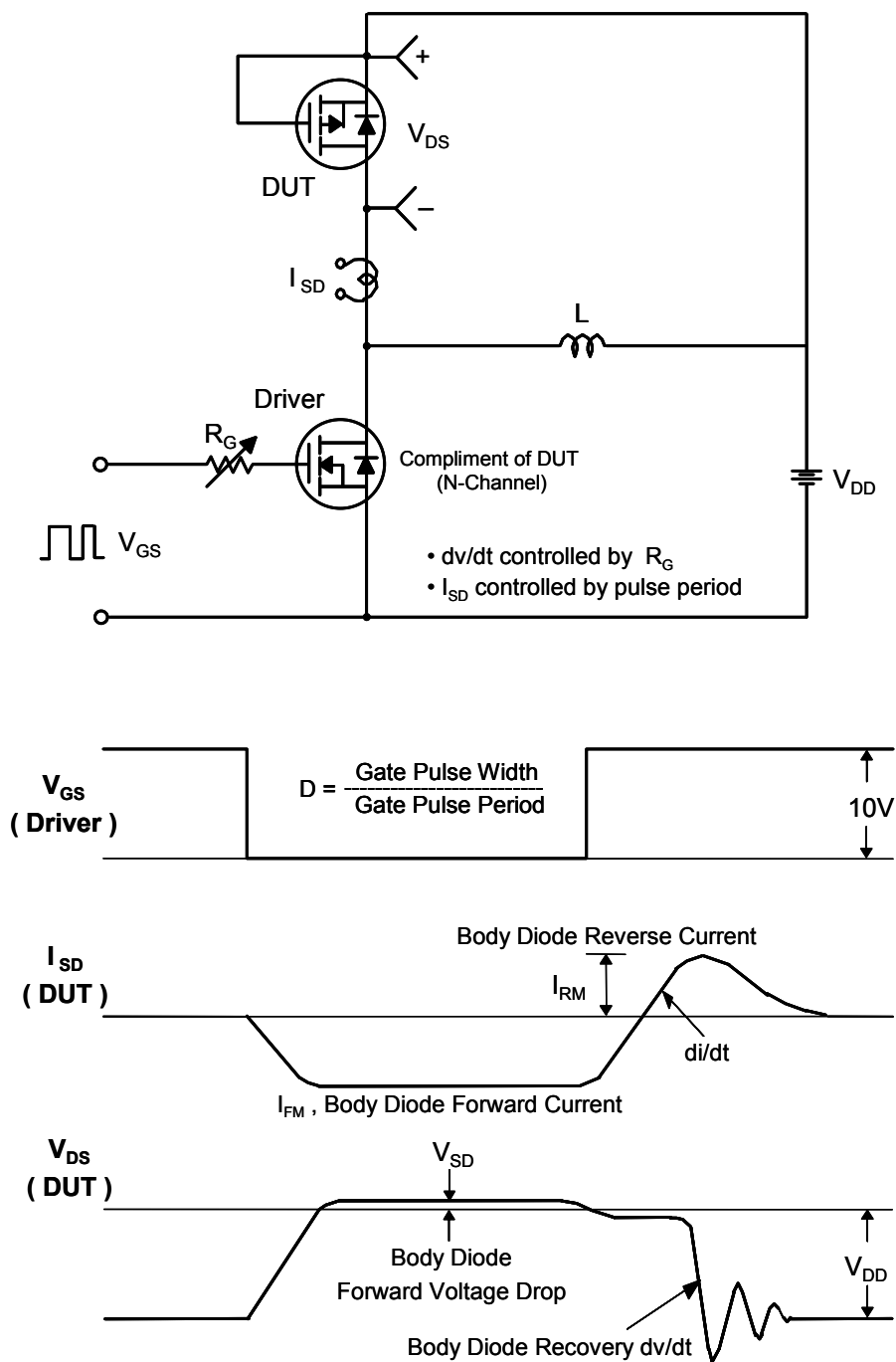
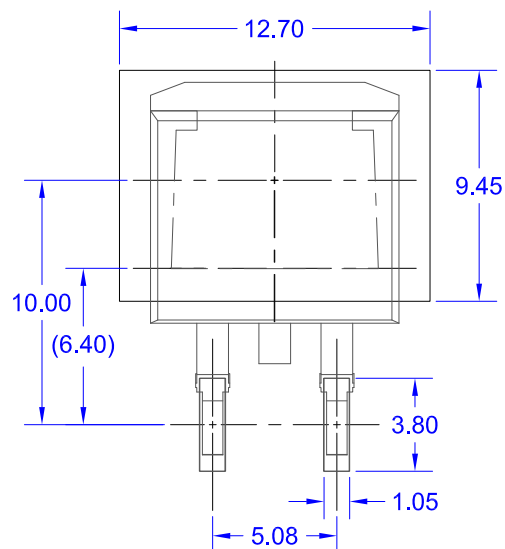
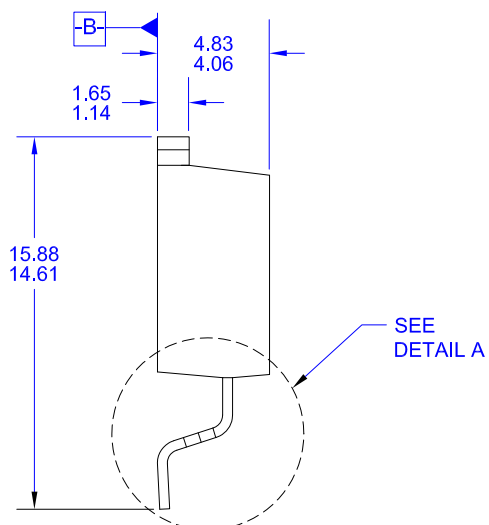
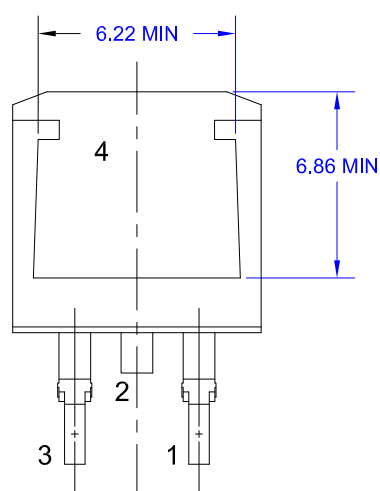


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

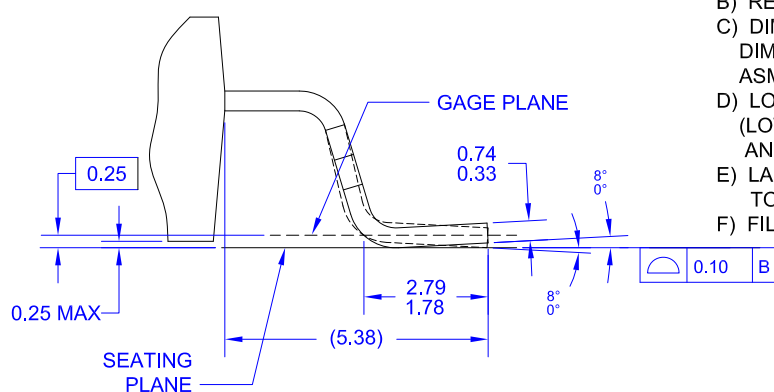




LAND PATTERN RECOMMENDATION
UNLESS NOTED, ALL DIMS TYPICAL



- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) REFERENCE JEDEC, TO-263, VARIATION AB.
- C) DIMENSIONING AND TOLERANCING PER DIMENSIONING AND TOLERANCING PER ASME Y14.5 - 2009.
- D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
- E) LANDPATTERN RECOMMENDATION PER IPC TO254P1524X482-3N
- F) FILENAME: TO263A02REV7



DETAIL A, ROTATED 90°
SCALE: 2X





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