

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar with an I²C-bus interface.

The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred via a serial two-line bidirectional bus (I²C). Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadmium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

Features

- Serial input/output I²C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32.768 kHz)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range					
clock (pin 16 to pin 15)	V _{DD} -V _{SS1}	1.1	—	6.0	V
I ² C interface (pin 16 to pin 8)	V _{DD} -V _{SS2}	2.5	—	6.0	V
Crystal oscillator frequency	f _{osc}	—	32.768	—	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).

PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

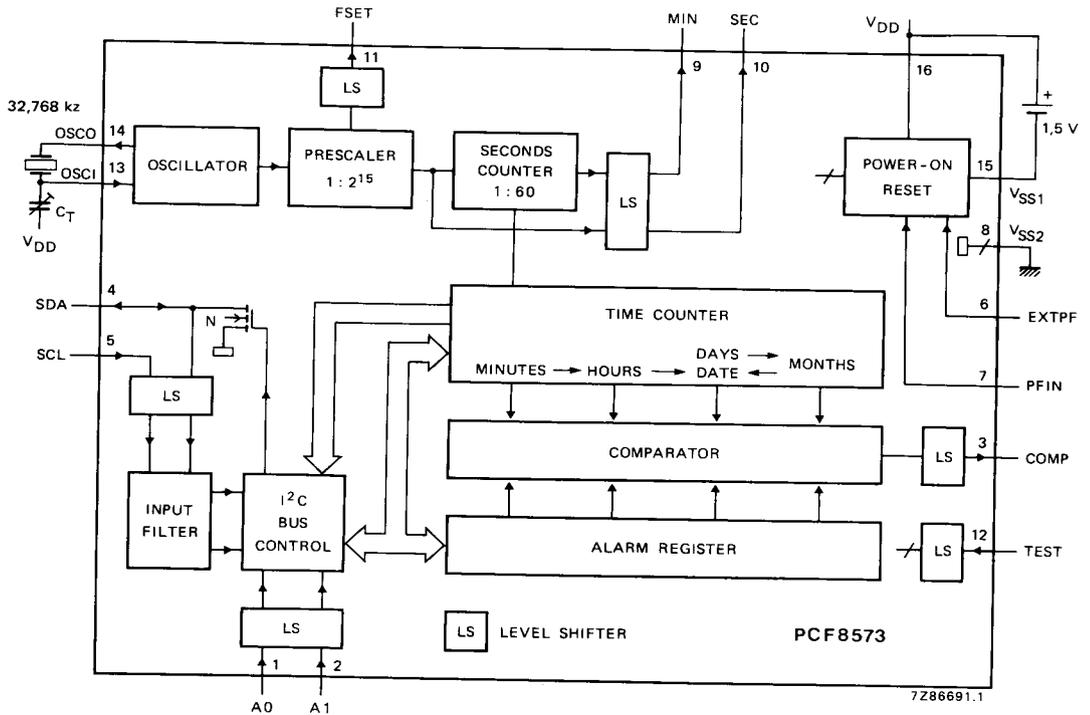


Fig.1 Block diagram.

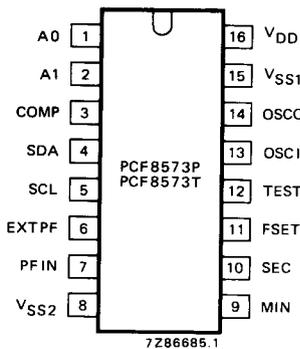


Fig.2 Pinning diagram.

PINNING

1	A0	address input
2	A1	address input
3	COMP	comparator output
4	SDA	serial data line
5	SCL	serial clock line
6	EXTPF	enable power fail flag input
7	PFIN	power fail flag input
8	VSS2	negative supply 2 (I ² C interface)
9	MIN	one pulse per minute output
10	SEC	one pulse per second output
11	FSET	oscillator tuning output
12	TEST	test input; must be connected to VSS2 when not in use
13	OSCI	oscillator input
14	OSCO	oscillator input/output
15	VSS1	negative supply 1 (clock)
16	VDD	common positive supply

FUNCTIONAL DESCRIPTION**Oscillator**

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32.768 kHz crystal connected between OSC1 and OSC0. A trimmer is connected between OSC1 and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I²C-bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH-to-LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note to Table 1

- Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I²C-bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I²C-bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I²C-bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I²C-bus.

FUNCTIONAL DESCRIPTION (continued)**Power on/power fail detection**

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1} , or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1} . The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)

1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I²C-bus. A power on reset for the I²C-bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2} .

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{DD} = V_{SS2}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig.3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

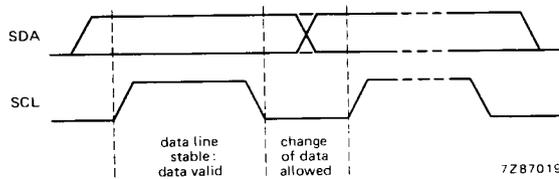


Fig.3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

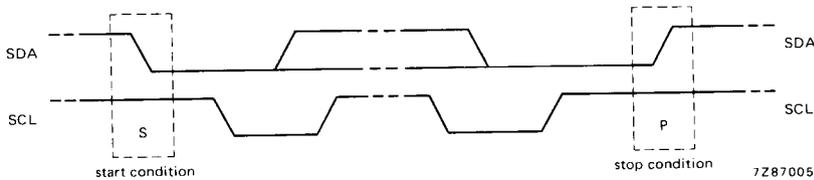


Fig.4 Definition of start and stop conditions.

System configuration (see Fig.5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

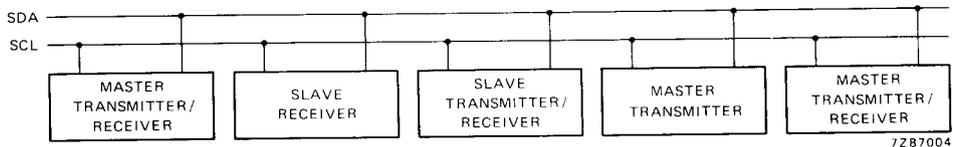
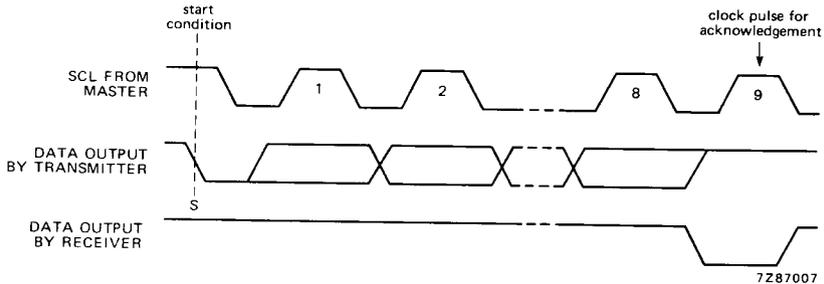


Fig.5 System configuration.

CHARACTERISTICS OF THE I²C-bus (continued)**Acknowledge** (see Fig.6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig.10 and Fig.11).

Fig.6 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD} .

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	—	—	100	kHz
Tolerable spike width on bus	t_{SW}	—	—	100	ns
Bus free time	t_{BUF}	4.7	—	—	μs
Start condition set-up time	$t_{SU}; STA$	4.7	—	—	μs
Start condition hold time	$t_{HD}; STA$	4.0	—	—	μs
SCL LOW time	t_{LOW}	4.7	—	—	μs
SCL HIGH time	t_{HIGH}	4.0	—	—	μs
SCL and SDA rise time	t_r	—	—	1.0	μs
SCL and SDA fall time	t_f	—	—	0.3	μs
Data set-up time	$t_{SU}; DAT$	250	—	—	ns
Data hold time	$t_{HD}; DAT$	0	—	—	ns
SCL LOW to data out valid	$t_{VD}; DAT$	—	—	3.4	μs
Stop condition set-up time	$t_{SU}; STO$	4.0	—	—	μs

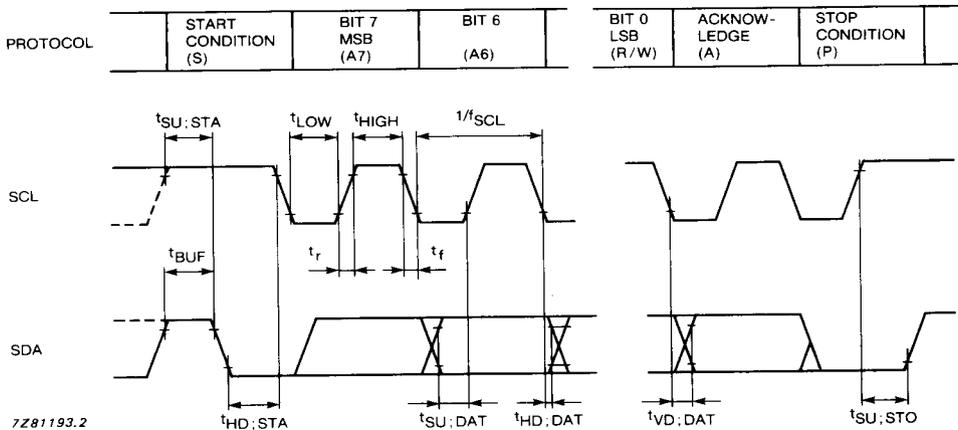


Fig.7 I²C-bus timing diagram.

ADDRESSING

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig.8.

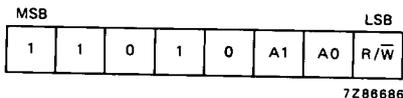


Fig.8 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C-bus configuration for different clock/calendar READ and WRITE cycles is shown in Figs 9, 10 and 11.

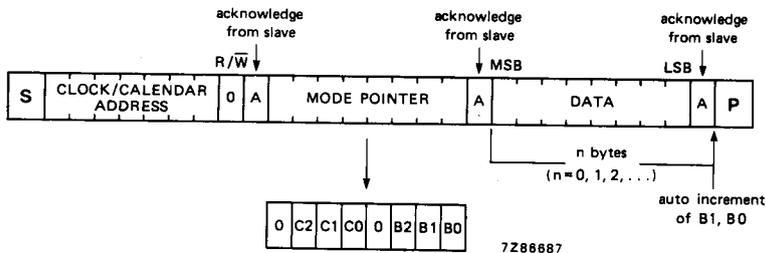


Fig.9 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nibble is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. -30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB		DATA				LSB		addressed to:
upper digit		lower digit				LA		
UD	UC	UB	UA	LD	LC		LB	
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where:

"X" is the don't care bit

"D" is the data bit

Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

	mode pointer							acknowledge on byte		
	C2	C1	C0		B2	B1	B0	address	mode pointer	data
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where:

"X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB				DATA				LSB	addressed to
upper digit				lower digit					
UD	UC	UB	UA	LD	LC	LB	LA		
0	0	D	D	D	D	D	D	hours	
0	D	D	D	D	D	D	D	minutes	
0	0	D	D	D	D	D	D	days	
0	0	0	D	D	D	D	D	months	
0	0	0	*	**	NODA	COMP	POWF	control/status flags	

Where:

"D" is the data bit

* = minutes

** = seconds.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	condition	symbol	min.	max.	unit
Supply voltage range					
pin 16 to pin 15		$V_{DD}-V_{SS1}$	-0.3	8.0	V
pin 16 to pin 8		$V_{DD}-V_{SS2}$	-0.3	8.0	V
Voltage input					
pins 4 and 5	note 1	V_I	$V_{SS2}-0.8$	$V_{DD}+0.8$	V
pins 6, 7, 13 and 14		V_I	$V_{SS1}-0.6$	$V_{DD}+0.6$	V
any other pin		V_I	$V_{SS2}-0.6$	$V_{DD}+0.6$	V
Input current		I_I	-	10	mA
Output current		I_O	-	10	mA
Power dissipation per output		P_O	-	100	mW
Total power dissipation		P_{tot}	-	200	mW
Operating ambient temperature range		T_{amb}	-40	+85	°C
Storage temperature range		T_{stg}	-55	+125	°C

Note to the Ratings

1. With input impedance of minimum 500 Ω .

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

$V_{SS2} = 0\text{ V}$; $T_{amb} = -40\text{ to }+85\text{ }^{\circ}\text{C}$ unless otherwise specified. Typical values at $T_{amb} = +25\text{ }^{\circ}\text{C}$

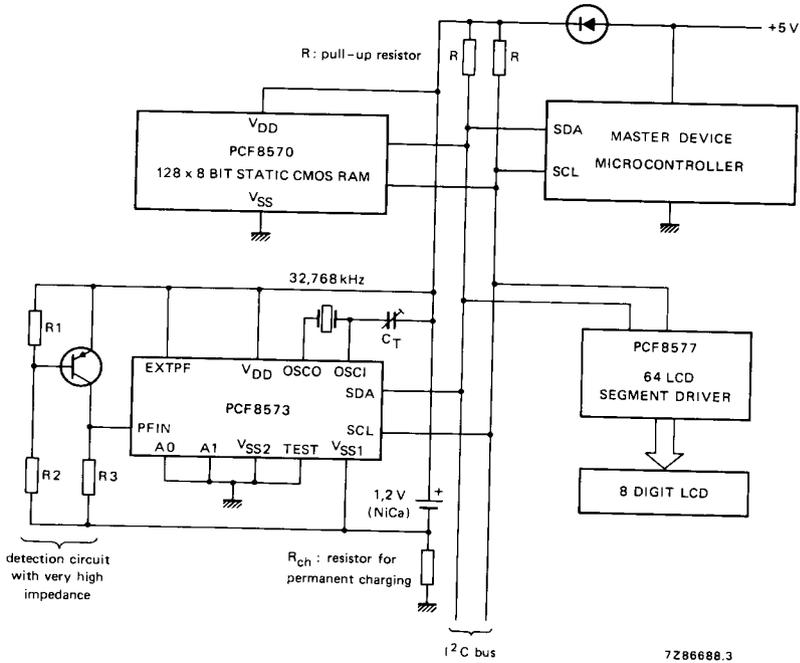
parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
I ² C interface		$V_{DD}-V_{SS2}$	2.5	5.0	6.0	V
clock	$t_{HD}; DAT \geq 300\text{ ns}$	$V_{DD}-V_{SS1}$	1.1	1.5	$V_{DD}-V_{SS2}$	V
Supply current						
V_{SS1} (pin 15)	$V_{DD}-V_{SS1} = 1.5\text{ V}$	$-I_{SS1}$	—	3	10	μA
	$V_{DD}-V_{SS1} = 5\text{ V}$	$-I_{SS1}$	—	12	50	μA
V_{SS2} (pin 8)	$V_{DD}-V_{SS2} = 5\text{ V}$; $I_O = 0$ all outputs	$-I_{SS2}$	—	—	50	μA
Input SCL; input/output SDA						
Input voltage LOW		V_{IL}	—	—	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	—	—	V
Leakage current	$V_I = V_{SS2}$ or V_{DD}	$ I_{LI} $	—	—	1	μA
Input capacitance		C_I	—	—	7	pF
Inputs A0, A1, TEST						
Input voltage LOW		V_{IL}	—	—	$0.2V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	—	—	V
Input leakage current	$V_I = V_{SS2}$ or V_{DD}	$\pm I_{LI}$	—	—	250	nA
Inputs EXTPF, PFIN						
Input voltage LOW		V_{IL}	0	—	$0.2V_{DD}-V_{SS1}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}-V_{SS1}$	—	—	V
Input leakage current	$V_I = V_{SS1}$ to V_{DD} $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_I = V_{SS1}$ to V_{DD}	$\pm I_{LI}$	—	—	1.0	μA
		$\pm I_{LI}$	—	—	0.1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output SDA (n channel open drain)						
Output "ON"	$I_O = 3 \text{ mA};$ $V_{DD}-V_{SS2} = 2.5 \text{ to}$ $\text{to } 6 \text{ V}$	V_{OL}	—	—	0.4	V
Leakage current	$V_{DD}-V_{SS2} = 6 \text{ V};$ $V_O = 6 \text{ V}$	$ I_{LI} $	—	—	1	μA
Outputs						
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)						
Output voltage LOW	$V_{DD}-V_{SS2} = 2.5 \text{ V};$ $I_O = 0.3 \text{ mA}$	V_{OL}	—	—	0.4	V
	$V_{DD}-V_{SS2} = 4 \text{ to } 6 \text{ V};$ $I_O = 1.6 \text{ mA}$	V_{OL}	—	—	0.4	V
Output voltage HIGH	$V_{DD}-V_{SS2} = 2.5 \text{ V};$ $-I_O = 0.1 \text{ mA}$	V_{OH}	$V_{DD}-0.4$	—	—	V
	$V_{DD}-V_{SS2} = 4 \text{ to } 6 \text{ V};$ $-I_O = 0.5 \text{ mA}$	V_{OH}	$V_{DD}-0.4$	—	—	V
Internal threshold voltage						
Power failure detection		V_{TH1}	1	1.2	1.4	V
Power "ON" reset		V_{TH2}	1.5	2.0	2.5	V
Rise and fall times of input signals						
Input EXTPF		t_r, t_f	—	—	1	μs
Input PFIN		t_r, t_f	—	—	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels						
rise time		t_r	—	—	1	μs
fall time		t_f	—	—	0.3	μs

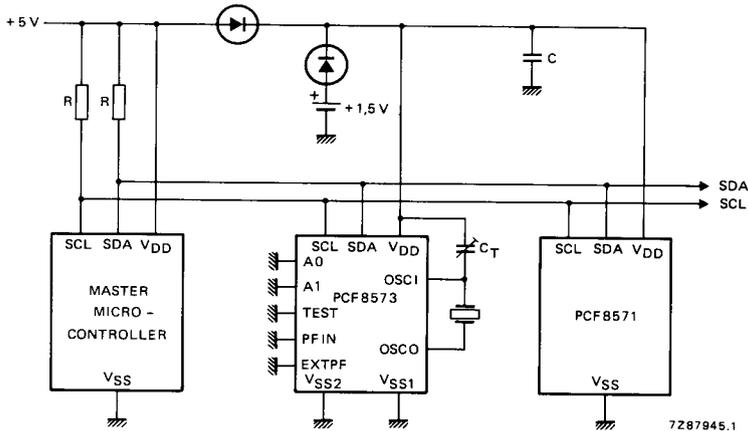
parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Integrated oscillator capacitance		C_{OUT}	—	40	—	pF
Oscillator feedback resistance		R_f	—	3	—	M Ω
Oscillator stability	$\Delta(V_{DD}-V_{SS1}) = 100$ mV; at $V_{DD}-V_{SS1} = 1.55$ V; $T_{amb} = 25$ °C	f/f_{osc}	—	2×10^{-7}	—	—
Quartz crystal parameters	$f = 32.768$ kHz					
Series resistance		R_S	—	—	40	k Ω
Parallel capacitance		C_L	—	10	—	pF
Trimmer capacitance		C_T	5	—	25	pF

APPLICATION INFORMATION



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Fig.12 Application example of the PCF8573 clock/calendar.



7287945.1

Fig.13 Application example of the PCF8573 with common VSS1 and VSS2 supply.

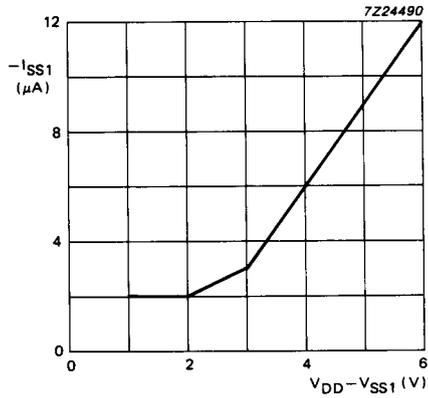
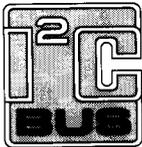


Fig. 14 Typical supply current ($-I_{SS1}$) as a function of clock supply voltage ($V_{DD}-V_{SS1}$) at $T_{amb} = -40$ to $+85$ °C.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.