5V/3.3V D FLIP-FLOP WITH SET AND RESET

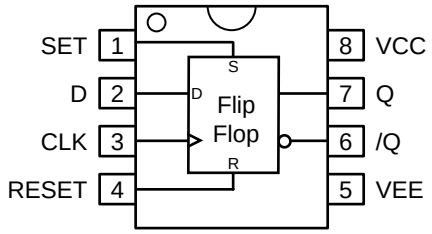
FEATURES

- **Guaranteed >3GHz bandwidth over temperature**
- **Guaranteed <440ps propagation delay**
- **3.3V and 5V power supply options**
- **75Ω internal input pulldown resistor**
- **Wide operating temperature range: –40°C to +85°C**
- **Available in 8-Pin (3mm) MSOP and SOIC package**

DESCRIPTION

The SY10EP31V is a D flip-flop with set and reset. The device is pin and functionally equivalent to the EL31 and LVEL31 devices. With AC performance much faster than the EL31 and LVEL31 devices, the EP31V is ideal for applications requiring the fastest AC performance available. Both SET and RESET inputs are asynchronous, level triggered signals. Data enters the master portion of the flip-flop when CLK is low and is transferred to the slave, and thus the outputs, upon a positive transition of the CLK.

PIN CONFIGURATION/BLOCK DIAGRAM



8-Pin MSOP and SOIC Packages

PIN NAMES

Pin	Function
CLK	ECL Clock Inputs
RESET	ECL Asynchronous Reset
SET	ECL Asynchronous Set
D	ECL Data Input
Q, /Q	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative, 0 Supply

TRUTH TABLE

D	SET	RESET	CLK	Q
L	L	L	Z	L
H	L	L	Z	H
X	H	L	X	H
X	L	H	X	L
X	H	H	X	UNDEF

Z = LOW to HIGH Transition

Rev.: A Amendment: /0
Issue Date: June 2001

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{CC}	Power Supply Voltage (V_{EE} = 0)		+6.0 to 0	V
V_{EE}	Power Supply Voltage (V_{CC} = 0)		–6.0 to 0	V
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE}) Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})		–6.0 to 0 +6.0 to 0	V V
I_{OUT}	Output Current	–Continuous –Surge	50 100	mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{store}	Storage Temperature Range		–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	–Still Air –500lfpm	TBD TBD	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)		TBD	°C/W

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

5V PECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = +5.0V ±10%, V_{EE} = 0V[2]

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current[3]	—	34	44	—	35	45	—	37	47	mA
V_{OH}	Output HIGH Voltage[4]	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Outuput LOW Voltage[4]	3050	3190	3315	3050	3255	3380	3050	3315	3440	mV
V_{IH}	Input HIGH Voltage	3790	—	4115	3855	—	4180	3915	—	4240	mV
V_{IL}	Input LOW Voltage	3065	—	3390	3130	—	3455	3190	—	3515	mV
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	µA

NOTES:

1. 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
2. Input and output parameters vary 1:1 with V_{CC}.
3. V_{CC} = 0V, V_{EE} = V_{EE}(Min) to V_{EE}(Max), all other pins floating.
4. All loading with 50Ω to V_{CC} – 2.0V.

3.3V LVPECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = +3.3V ±10%, V_{EE} = 0V[2]

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current[3]	—	34	44	—	35	45	—	37	47	mA
V_{OH}	Output HIGH Voltage[4]	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Outuput LOW Voltage[4]	1350	1490	1615	1350	1555	1680	1350	1615	1740	mV
V_{IH}	Input HIGH Voltage	2090	—	2415	2155	—	2480	2215	—	2540	mV
V_{IL}	Input LOW Voltage	1365	—	1690	1430	—	1755	1490	—	1815	mV
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	µA

NOTES:

1. 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
2. Input and output parameters vary 1:1 with V_{CC}.
3. V_{CC} = 0V, V_{EE} = V_{EE}(Min) to V_{EE}(Max), all other pins floating.
4. All loading with 50Ω to V_{CC} – 2.0V.

NECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 0V, V_{EE} = –3.3V to –5.0V ±10%[2]

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current[3]	—	34	44	—	35	45	—	37	47	mA
V_{OH}	Output HIGH Voltage[4]	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Outuput LOW Voltage[4]	–1950	–1810	–1685	–1950	–1745	–1620	–1950	–1685	–1560	mV
V_{IH}	Input HIGH Voltage	–1210	—	–885	–1145	—	–820	–1085	—	–760	mV
V_{IL}	Input LOW Voltage	–1935	—	–1610	–1870	—	–1545	–1810	—	–1485	mV
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	µA

NOTES:

1. 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
2. Input and output parameters vary 1:1 with V_{CC}.
3. V_{CC} = 0V, V_{EE} = V_{EE}(Min) to V_{EE}(Max), all other pins floating.
4. All loading with 50Ω to V_{CC} – 2.0V.

AC ELECTRICAL CHARACTERISTICS[1]

NECL operation: V_{CC} = 0V, V_{EE} = –3.3V to –5.0V ±10%; PECL operation: V_{EE} = 0V, V_{CC} = +3.3V to +5.0V ±10%

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Frequency[2]	3	—	—	3	—	—	3	—	—	GHz
t_{PLH} t_{PHL}	Propagation Delay to Output Differential CLK→ Q, /Q SET, RESET→ Q, /Q	 250 300	 330 380	 400 450	 270 330	 340 400	 410 410	 300 360	 370 430	 440 500	ps
t_{RR}	Set/Reset Recovery	225	—	—	225	—	—	225	—	—	ps
t_S	Setup Time	100	—	—	100	—	—	100	—	—	ps
t_H	Hold Time	150	—	—	150	—	—	150	—	—	ps
t_{PW}	Minimum Pulse Width SET, RESET	 550	 450	 —	 550	 450	 —	 550	 450	 —	ps ps
t_{JITTER}	Cycle-to-Cycle RMS Jitter	—	0.2	<1.0	—	0.2	<1.0	—	0.2	<1.0	ps(rms)
t_r t_f	Output Rise/Fall Times Q, /Q (20% to 80%)	50	120	180	60	130	200	70	150	220	ps

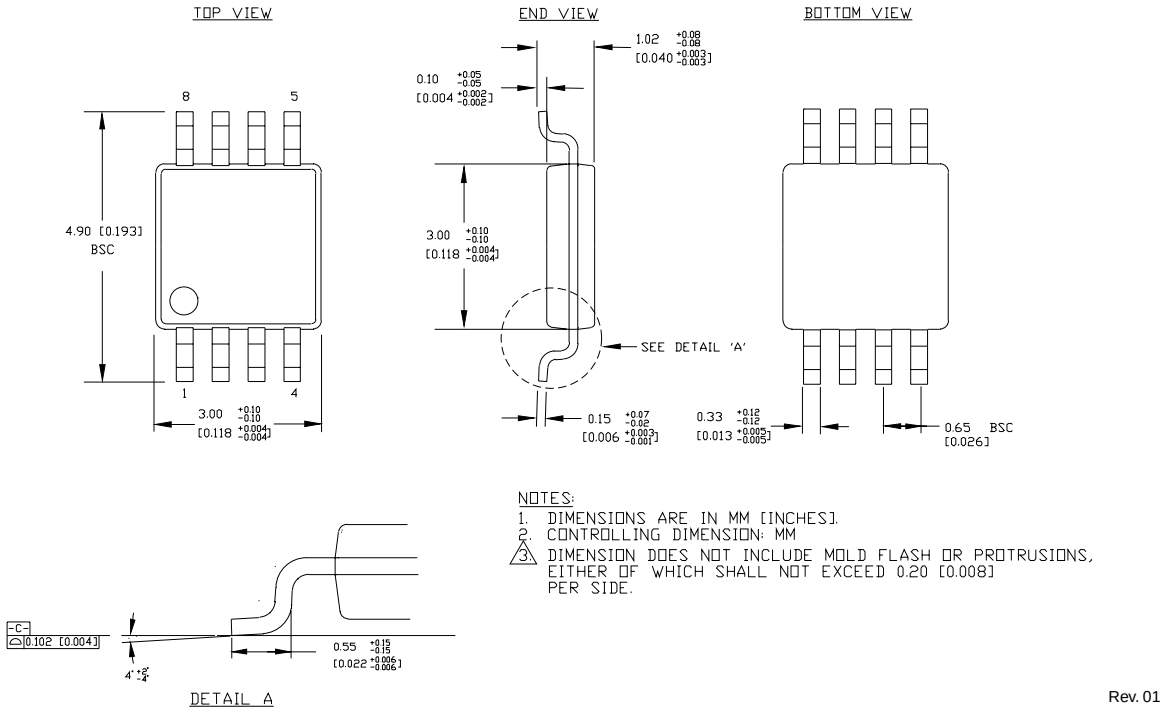
NOTES:

1. Measured using a 750mV source, 50% duty cycle clock source. All loading with 50Ω to V_{CC} –2.0V.
2. f_{MAX} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.

PRODUCT ORDERING INFORMATION

Ordering Code	Package Type	Operating Range	Package Marking
SY10EP31VKI	K8-1	Industrial	HP31
SY10EP31VKITR	K8-1	Industrial	HP31
SY10EP31VZI	Z8-1	Industrial	HEP31V
SY10EP31VZITR	Z8-1	Industrial	HEP31V

8 LEAD MSOP (K8-1)



NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

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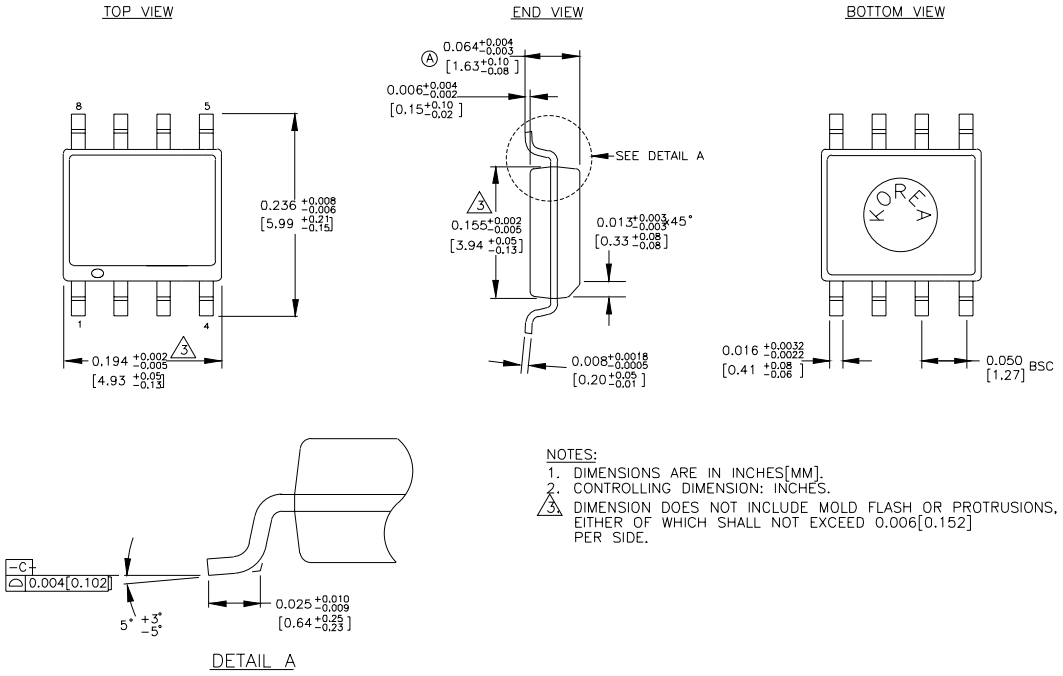
8 LEAD PLASTIC SOIC (Z8-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

Rev. 03

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