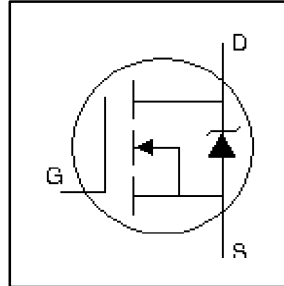


HEXFET® Power MOSFET

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V V_{GS} Rating
- Reduced C_{iss} , C_{oss} , C_{rss}
- Isolated Central Mounting Hole
- Dynamic dv/dt Rated
- Repetitive Avalanche Rated



$$V_{DSS} = 400V$$

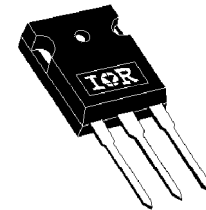
$$R_{DS(on)} = 0.20\Omega$$

$$I_D = 23A$$

Description

This new series of Low Charge HEXFET Power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced Hexfet technology the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability of HEXFETs offer the designer a new standard in power transistors for switching applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	23	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ 10V	14	
I_{DM}	Pulsed Drain Current ①	92	
P_D @ $T_C = 25^\circ C$	Power Dissipation	280	W
	Linear Derating Factor	2.2	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy ②	1200	mJ
I_{AR}	Avalanche Current ③	23	A
E_{AR}	Repetitive Avalanche Energy ①	28	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
T_J	Operating Junction and	-55 to + 150	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.45	$^\circ C/W$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	—	

IRFP360LC



Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	400	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.49	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	—	—	0.20	Ω	$V_{GS} = 10V, I_D = 14A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	13	—	—	S	$V_{DS} = 50V, I_D = 14A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 400V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 320V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	110	nC	$I_D = 23A$
Q_{gs}	Gate-to-Source Charge	—	—	28		$V_{DS} = 320V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	45		$V_{GS} = 10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	16	—		$V_{DD} = 200V$
t_r	Rise Time	—	75	—	ns	$I_D = 23A$
$t_{d(off)}$	Turn-Off Delay Time	—	42	—		$R_G = 4.3\Omega$
t_f	Fall Time	—	50	—		$R_D = 7.9\Omega$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	13	—		
C_{iss}	Input Capacitance	—	3400	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	540	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	42	—		$f = 1.0MHz$, See Fig. 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	23	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	92		
V_{SD}	Diode Forward Voltage	—	—	1.8	V	$T_J = 25^\circ\text{C}, I_S = 23A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	400	600	ns	$T_J = 25^\circ\text{C}, I_F = 23A$
Q_{rr}	Reverse Recovery Charge	—	5.7	8.6	μC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

③ $I_{SD} \leq 23A, di/dt \leq 170A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$

② $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}$, $L = 4.0mH$
 $R_G = 25\Omega, I_{AS} = 23A$. (See Figure 12)

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

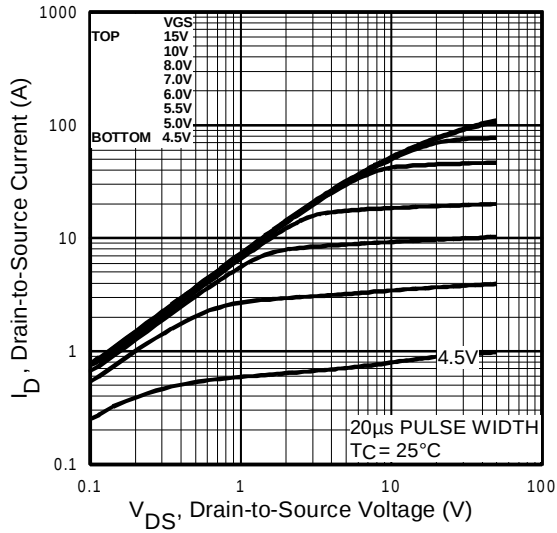


Fig 1. Typical Output Characteristics,
 $T_C = 25^\circ\text{C}$

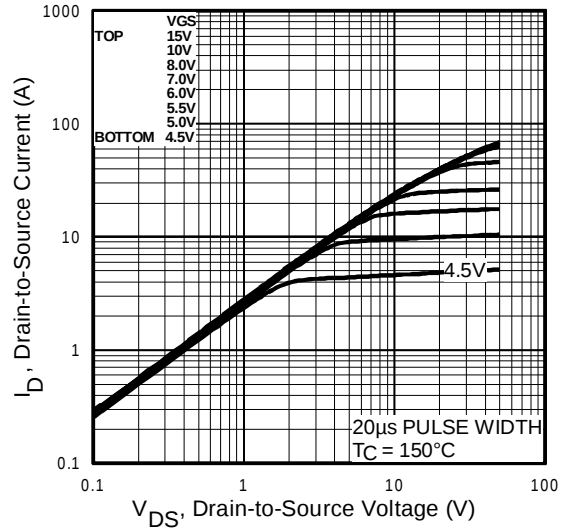


Fig 2. Typical Output Characteristics,
 $T_C = 150^\circ\text{C}$

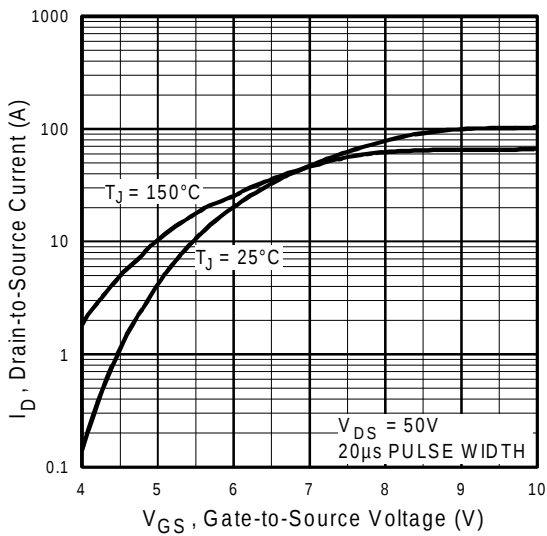


Fig 3. Typical Transfer Characteristics

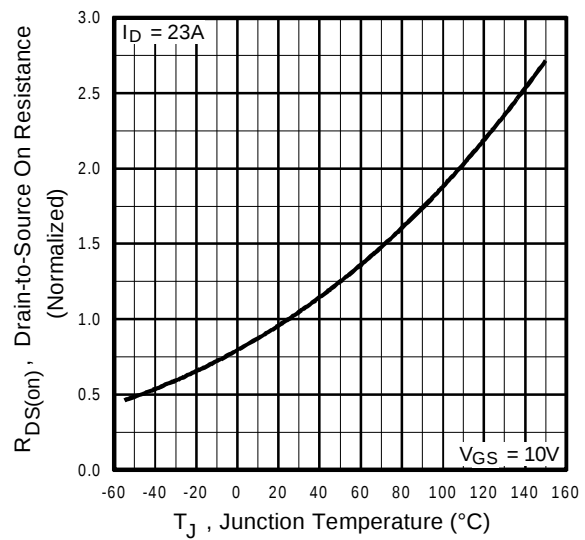


Fig 4. Normalized On-Resistance
Vs. Temperature

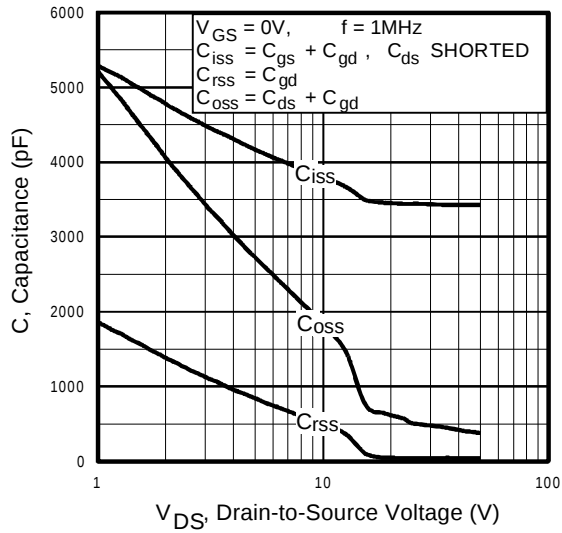


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

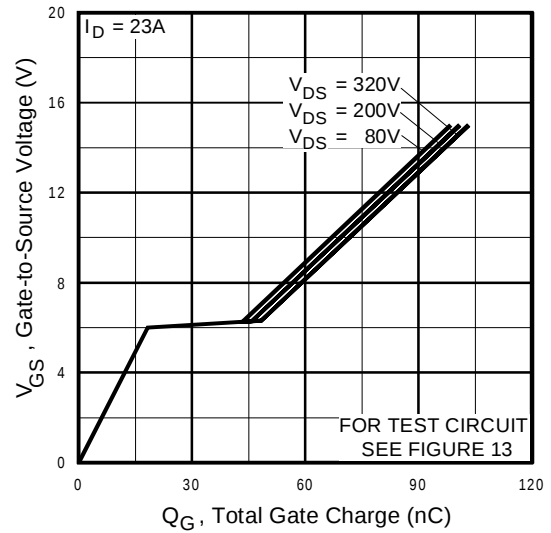


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

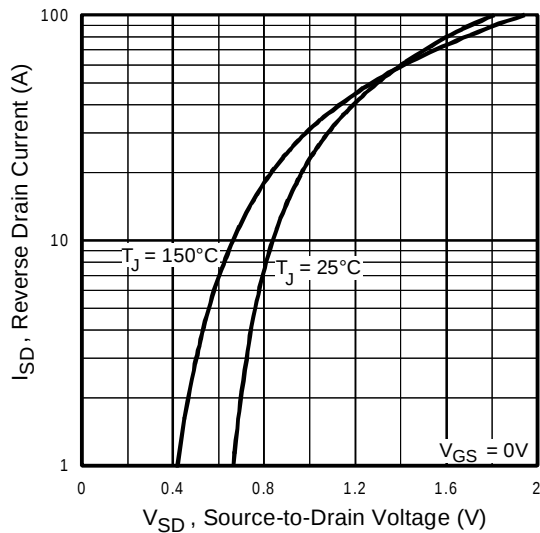


Fig 7. Typical Source-Drain Diode Forward Voltage

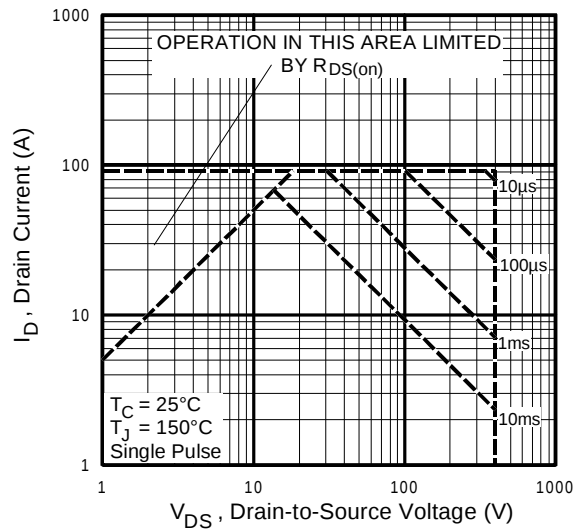


Fig 8. Maximum Safe Operating Area

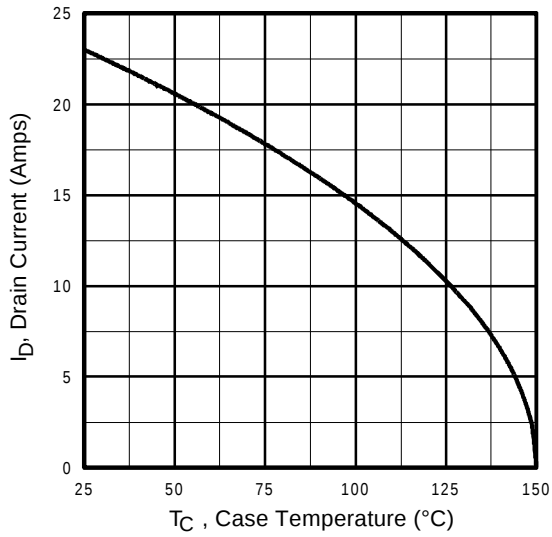


Fig 9. Maximum Drain Current Vs. Case Temperature

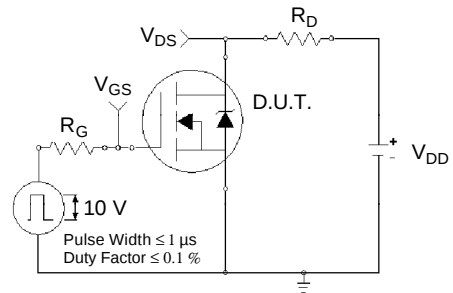


Fig 10a. Switching Time Test Circuit

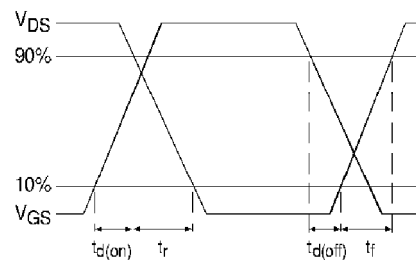


Fig 10b. Switching Time Waveforms

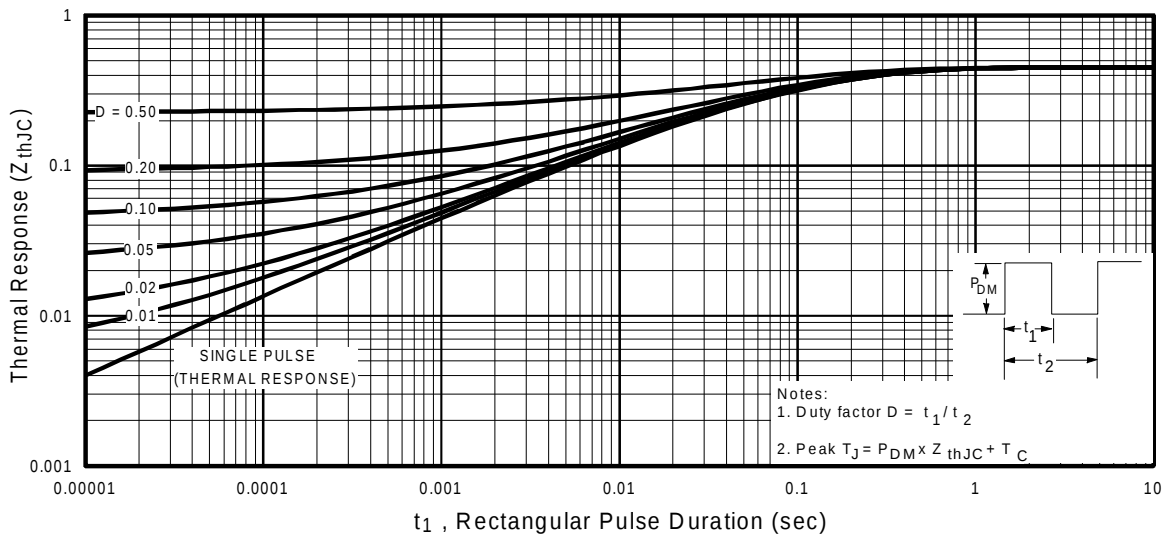


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

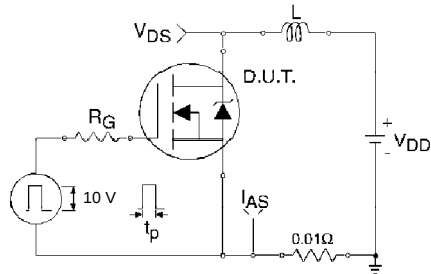


Fig 12a. Unclamped Inductive Test Circuit

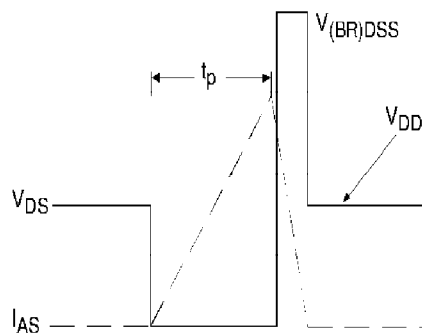


Fig 12b. Unclamped Inductive Waveforms

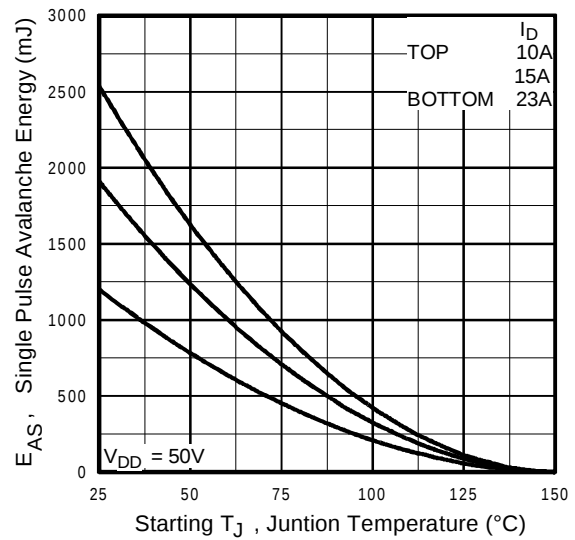


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

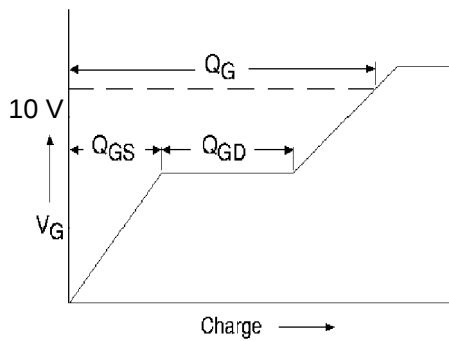


Fig 13a. Basic Gate Charge Waveform

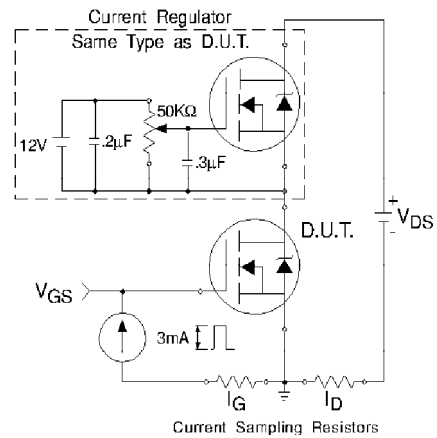
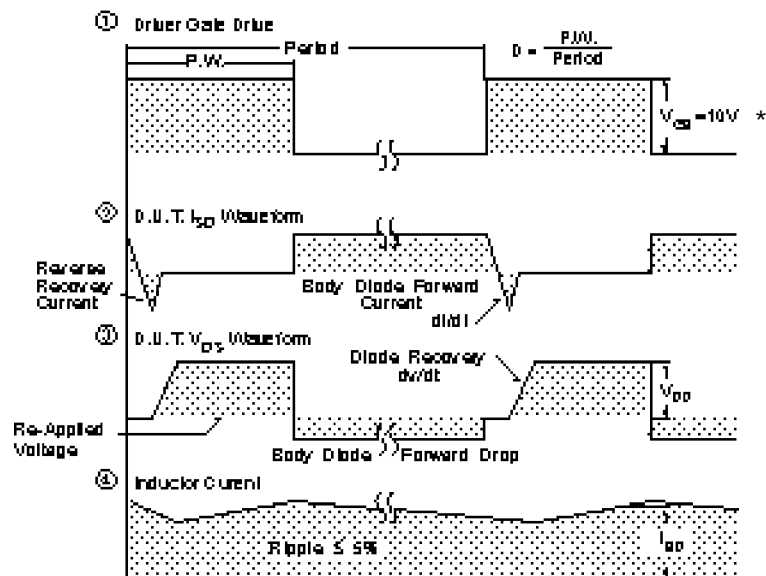
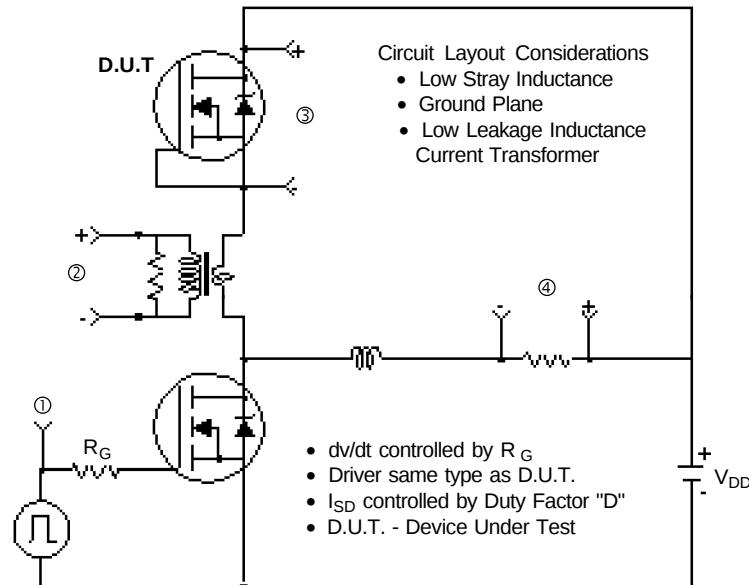


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Technical drawing of a 3-pin connector. The drawing includes a top view and a side view. Dimensions are provided in inches and millimeters.

Top View Dimensions:

- Overall width: 15.90 (.626)
- Width between pins: 15.30 (.602)
- Pin diameter: $\varnothing 0.25$ (.010)
- Pin spacing: 2X $\varnothing 5.50$ (.217)
- Pin diameter: 2X $\varnothing 4.50$ (.177)
- Pin length: 2X 5.45 (.215)
- Pin diameter: 2X $\varnothing 2.40$ (.094)
- Pin diameter: 2X $\varnothing 2.00$ (.079)
- Pin length: 2X 3.40 (.133)
- Pin diameter: 2X $\varnothing 3.00$ (.118)
- Pin length: 2X 14.80 (.583)
- Pin diameter: 2X $\varnothing 14.20$ (.559)
- Pin length: 2X 20.30 (.800)
- Pin diameter: 2X $\varnothing 19.70$ (.775)

Side View Dimensions:

- Overall height: 5.30 (.209)
- Height between pins: 4.70 (.185)
- Pin diameter: 2.50 (.098)
- Pin diameter: 1.50 (.059)
- Pin length: 4
- Pin diameter: 3X $\varnothing 0.80$ (.031)
- Pin diameter: 3X $\varnothing 0.40$ (.016)
- Pin length: 2.60 (.102)
- Pin diameter: 2.20 (.087)

Feature Callouts:

- B-
- A-
- C-
- D-

Feature Callouts:

- 1
- 2
- 3
- 4

EXAMPLE : THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 3A1Q

The diagram shows a MOSFET package with the following markings and labels:

- INTERNATIONAL RECTIFIER LOGO**: Points to the IOR logo on the package.
- PART NUMBER**: Points to the IRFPE30 marking on the package.
- ASSEMBLY LOT CODE**: Points to the 3A1Q marking on the package.
- DATE CODE (YYWW)**: Points to the 9302 marking on the package, with a note that YY = YEAR and WW = WEEK.

International IOR Rectifier

Data and specifications subject to change without notice.