



## 3.3V CMOS 12-BIT TRI-PORT BUS EXCHANGER WITH 5 VOLT TOLERANT I/O AND BUS-HOLD

**IDT74LVCH16260A**

### FEATURES:

- Typical  $t_{sk(0)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;  
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP  
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

### Drive Features for LVCH16260A:

- High Output Drivers:  $\pm 24mA$
- Reduced system switching noise

### APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

### DESCRIPTION:

The LVCH16260A tri-port bus exchanger is built using advanced dual metal CMOS technology. The LVCH16260A is a high-speed 12-bit latched

bus multiplexer/transceiver for use in high-speed microprocessor applications. This bus exchanger supports memory interleaving with latched outputs on the B ports and address multiplexing with latched inputs on the B ports.

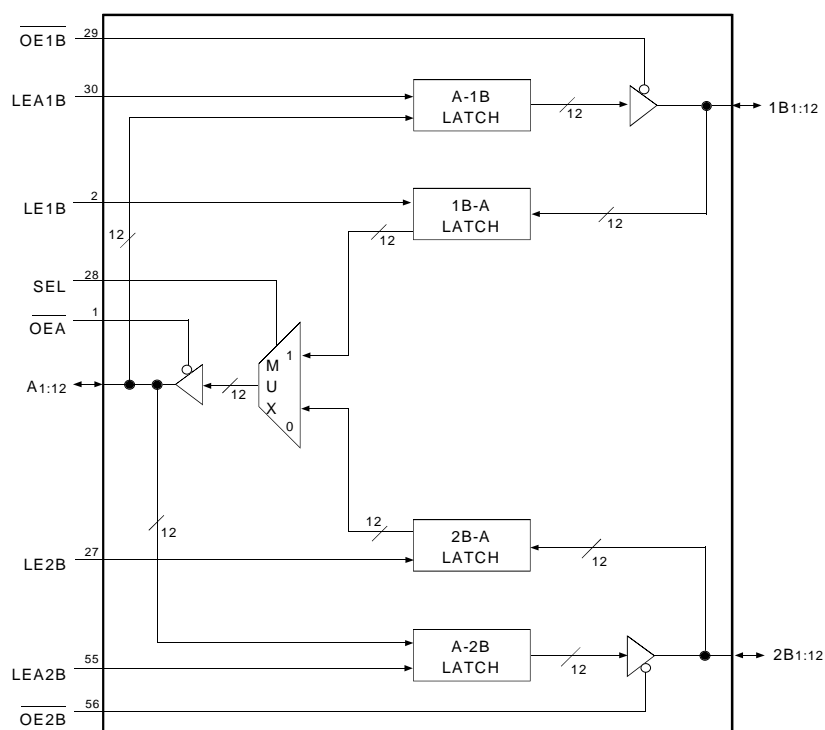
The LVCH16260A tri-port bus exchanger has three 12-bit ports. Data may be transferred between the A port and either/both of the B ports. The latch enable (LE1B, LE2B, LEA1B and LEA2B) inputs control data storage. When a latch-enable input is high, the latch is transparent. When a latch-enable input is low, the data at the input is latched and remains latched until the latch enable input is returned high. Independent output enables ( $\overline{OE1B}$  and  $\overline{OE2B}$ ) allow reading from one port while writing to the other port.

All pins of the 12-bit Bus Exchanger can be driven from either 3.3V or 5V devices. This feature allows the use of the device as a translator in a mixed 3.3V/5V supply system.

The LVCH16260A has been designed with a  $\pm 24mA$  output driver. The driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16260A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

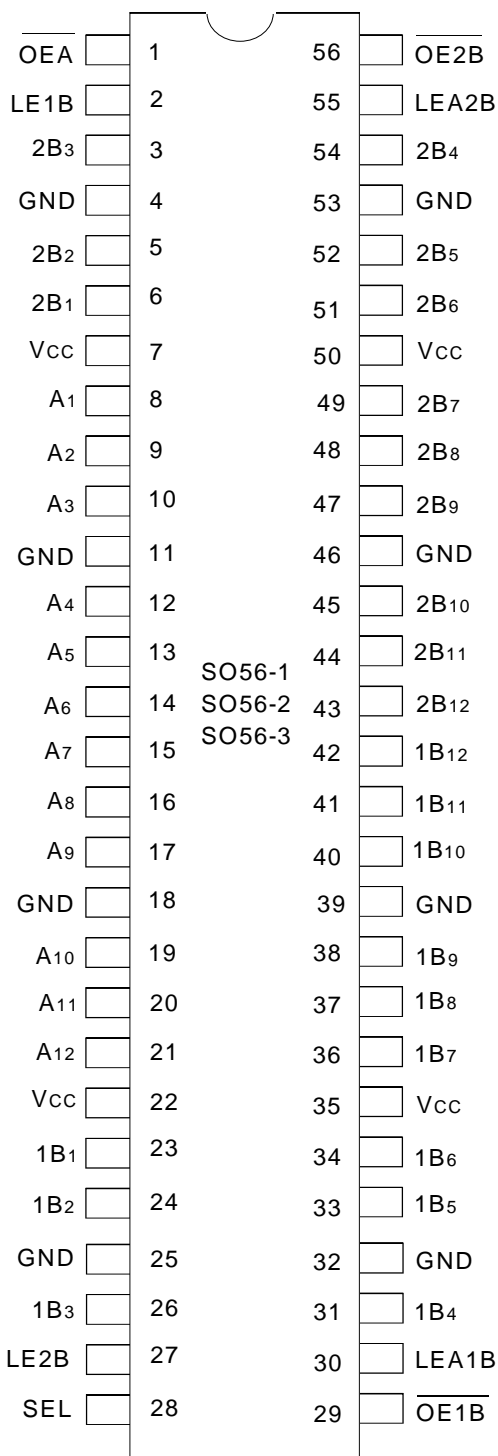
### Functional Block Diagram



**EXTENDED COMMERCIAL TEMPERATURE RANGE**

**MARCH 1999**

## PIN CONFIGURATION



SSOP/TSSOP/TVSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
TSTG	Storage Temperature	- 65 to +150	°C
I <sub>OUT</sub>	DC Output Current	- 50 to +50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	- 50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

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### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	6.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

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### NOTE:

- As applicable to the device type.

## FUNCTION TABLES (1)

Inputs						Outputs
1Bx	2Bx	SEL	LE1B	LE2B	$\overline{OE\bar{A}}$	Ax
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A <sub>0</sub> <sup>(2)</sup>
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A <sub>0</sub> <sup>(2)</sup>
X	X	X	X	X	H	Z

Inputs					Outputs	
Ax	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1Bx	2Bx
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	B <sub>0</sub> <sup>(2)</sup>
L	H	L	L	L	L	B <sub>0</sub> <sup>(2)</sup>
H	L	H	L	L	B <sub>0</sub> <sup>(2)</sup>	H
L	L	H	L	L	B <sub>0</sub> <sup>(2)</sup>	L
X	L	L	L	L	B <sub>0</sub> <sup>(2)</sup>	B <sub>0</sub> <sup>(2)</sup>
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

### NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance
- A<sub>0</sub>, B<sub>0</sub> = Output level before the indicated steady-state input conditions were established.

## PIN DESCRIPTION

Signal	I/O	Description
A(1:12)	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus. <sup>(1)</sup>
1B(1:12)	I/O	Bidirectional Data Port 1B. Connected to the even path or even bank of memory. <sup>(1)</sup>
2B(1:12)	I/O	Bidirectional Data Port 2B. Connected to the odd path or odd bank of memory. <sup>(1)</sup>
LEA1B	I	Latch Enable Input for A-1B Latch. The Latch is open when LEA1B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LEA1B.
LEA2B	I	Latch Enable Input for A-2B Latch. The Latch is open when LEA2B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LEA2B.
LE1B	I	Latch Enable Input for 1B-A Latch. The Latch is open when LE1B is HIGH. Data from the 1B port is latched on the HIGH to LOW transition of LE1B.
LE2B	I	Latch Enable Input for 2B-A Latch. The Latch is open when LE2B is HIGH. Data from the 2B port is latched on the HIGH to LOW transition of LE2B.
SEL	I	1B or 2B Path Selection. When HIGH, SEL enables data transfer from 1B Port to A Port. When LOW, SEL enables data transfer from 2B Port to A Port.
$\overline{OE\bar{A}}$	I	Output Enable for A Port (Active LOW).
$\overline{OE1B}$	I	Output Enable for 1B Port (Active LOW).
$\overline{OE2B}$	I	Output Enable for 2B Port (Active LOW).

### NOTE:

- These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		2	—	—	
$V_{IL}$	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		—	—	0.8	
$I_{IH}$ $I_{IL}$	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to $5.5\text{V}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OZH}$ $I_{OZL}$	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to $5.5\text{V}$	—	—	$\pm 10$	$\mu\text{A}$
$I_{OFF}$	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$ , $V_{IN}$ or $V_O \leq 5.5\text{V}$		—	—	$\pm 50$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$ , $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$V_H$	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or $V_{CC}$	—	—	10	$\mu\text{A}$
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$ other inputs at $V_{CC}$ or GND		—	—	500	$\mu\text{A}$

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### NOTES:

- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- This applies in the disabled state only.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_{BHH}$ $I_{BHL}$	Bus-Hold Input Sustain Current	$V_{CC} = 3.0\text{V}$	$V_I = 2.0\text{V}$	-75	—	—	$\mu\text{A}$
			$V_I = 0.8\text{V}$	75	—	—	
$I_{BHH}$ $I_{BHL}$	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	—	—	—	$\mu\text{A}$
			$V_I = 0.7\text{V}$	—	—	—	
$I_{BHHO}$ $I_{BHLO}$	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to $3.6\text{V}$	—	—	$\pm 500$	$\mu\text{A}$

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### NOTES:

- Pins with Bus-hold are identified in the pin description.
- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = – 0.1mA	VCC – 0.2	—	V
		VCC = 2.3V	IOH = – 6mA	2	—	
		VCC = 2.3V	IOH = – 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = – 24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

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### NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = – 40°C to +85°C.

## OPERATING CHARACTERISTICS, VCC = 3.3V ± 0.3V, TA = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per bus exchanger Outputs enabled	CL = 0pF, f = 10Mhz		pF
CPD	Power Dissipation Capacitance per bus exchanger Outputs disabled			pF

## SWITCHING CHARACTERISTICS <sup>(1)</sup>

Symbol	Parameter	VCC = 2.7V±0.2V		VCC = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay Ax to 1Bx or Ax to 2Bx	1.5	5.7	1.5	5	ns
tPLH tPHL	Propagation Delay 1Bx to Ax or 2Bx to Ax	1.5	6.1	1.5	5.2	ns
tPLH tPHL	Propagation Delay LExB to Ax	1.5	6.1	1.5	5.2	ns
tPLH tPHL	Propagation Delay LEA1B to 1Bx or LEA2B to 2Bx	1.5	6.1	1.5	5	ns
tPLH tPHL	Propagation Delay SEL to Ax	1.5	6.3	1.5	5.2	ns
tPZH tPZL	Output Enable Time OE $\overline{A}$ to Ax, OE1 $\overline{B}$ to 1Bx, or OE2 $\overline{B}$ to 2Bx	1.5	6.7	1.5	5.5	ns
tPHZ tPLZ	Output Disable Time OE $\overline{A}$ to Ax, OE1 $\overline{B}$ to 1Bx, or OE2 $\overline{B}$ to 2Bx	1.5	5.9	1.5	5.2	ns
tsu	Set-Up Time, HIGH or LOW Data to Latch	1	—	1	—	ns
tH	Hold Time, Latch to Data	1.2	—	1	—	ns
tw	Pulse Width, Latch HIGH	3	—	3	—	ns
tsk(o)	Output Skew <sup>(2)</sup>	—	—	—	500	ps

### NOTES:

1. See test circuits and waveforms. TA = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

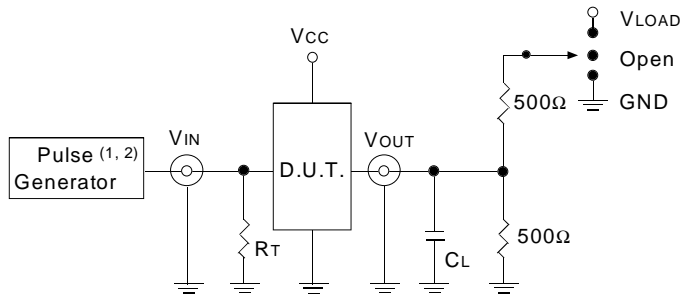
## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
$V_{LOAD}$	6	6	$2 \times V_{CC}$	V
$V_{IH}$	2.7	2.7	$V_{CC}$	V
$V_T$	1.5	1.5	$V_{CC} / 2$	V
$V_{LZ}$	300	300	150	mV
$V_{HZ}$	300	300	150	mV
$C_L$	50	50	30	pF

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### TEST CIRCUITS FOR ALL OUTPUTS



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#### DEFINITIONS:

$C_L$  = Load capacitance: includes jig and probe capacitance.  
 $R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

#### NOTE:

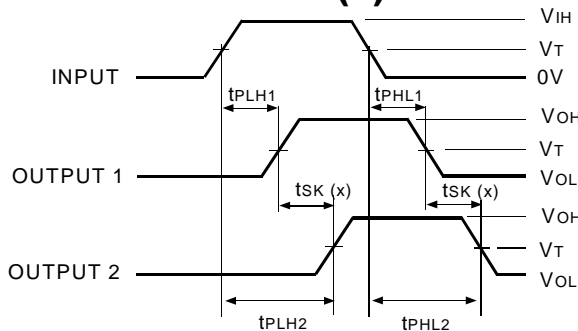
1. Pulse Generator for All Pulses: Rate  $\leq 10\text{MHz}$ ;  $t_F \leq 2.5\text{ns}$ ;  $t_R \leq 2.5\text{ns}$ .
2. Pulse Generator for All Pulses: Rate  $\leq 10\text{MHz}$ ;  $t_F \leq 2\text{ns}$ ;  $t_R \leq 2\text{ns}$ .

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	$V_{LOAD}$
Disable High Enable High	GND
All Other tests	Open

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### OUTPUT SKEW - $t_{SK}(x)$



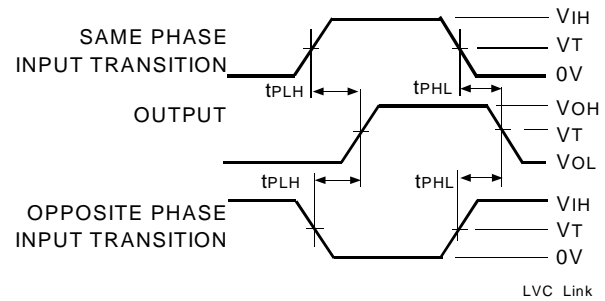
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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#### NOTES:

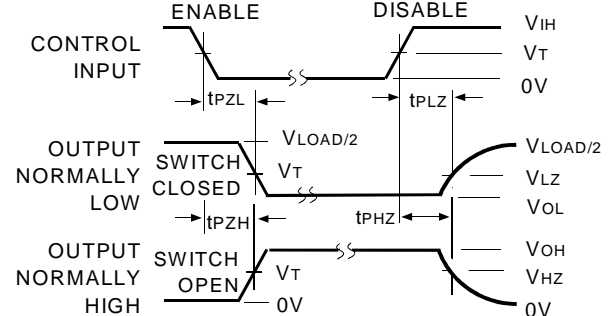
1. For  $t_{SK}(o)$  OUTPUT1 and OUTPUT2 are any two outputs.
2. For  $t_{SK}(b)$  OUTPUT1 and OUTPUT2 are in the same bank.

### PROPAGATION DELAY



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### ENABLE AND DISABLE TIMES

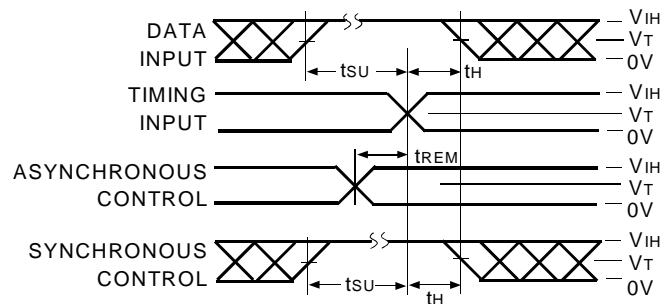


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#### NOTE:

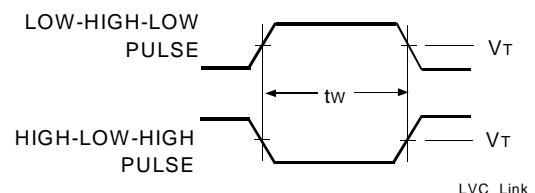
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

### SET-UP, HOLD, AND RELEASE TIMES



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### PULSE WIDTH



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## ORDERING INFORMATION

IDT	XX	LVC	X	XX	XXXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
					260A		12-Bit Tri-Port Bus Exchanger
				16			Double-Density with Resistors, $\pm 24\text{mA}$
			H				Bus-hold
		74					-40°C to +85°C



### CORPORATE HEADQUARTERS

2975 Stender Way  
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