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 ULTRA LOW CAPACITANCE TVS ARRAY
 

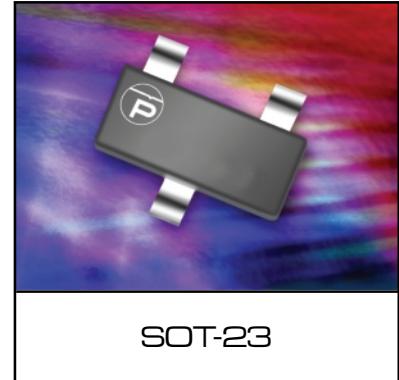
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**APPLICATIONS**

- ✓ Ethernet - 10/100 Base T
- ✓ Cellular Phones
- ✓ FireWire
- ✓ Audio/Video Inputs
- ✓ Portable Electronics

**IEC COMPATIBILITY (EN61000-4)**

- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns
- ✓ 61000-4-5 (Surge): 12A, 8/20 $\mu$ s - Level 1(Line-Ground) & Level 2(Line-Line)

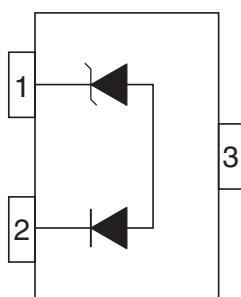

**FEATURES**

- ✓ ESD Protection > 40 kilovolts
- ✓ 500 Watts Peak Pulse Power per Line ( $t_p = 8/20\mu$ s)
- ✓ Low Clamping Voltage
- ✓ Available in Multiple Voltage Types Ranging from 3V to 36V
- ✓ **ULTRA LOW CAPACITANCE: 5pF**

**MECHANICAL CHARACTERISTICS**

- ✓ Molded JEDEC SOT-23
- ✓ Weight 14 milligrams (Approximate)
- ✓ Flammability rating UL 94V-0
- ✓ 8mm Tape and Reel Per EIA Standard 481
- ✓ Device Marking: Marking Code

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**PIN CONFIGURATION**


## DEVICE CHARACTERISTICS

### MAXIMUM RATINGS @ 25°C Unless Otherwise Specified

PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power - $t_p = 8/20\mu\text{s}$ (See Figure 1)	$P_{PP}$	500	W
Operating Temperature	$T_J$	-55°C to 150°C	°C
Storage Temperature	$T_{STG}$	-55°C to 150°C	°C

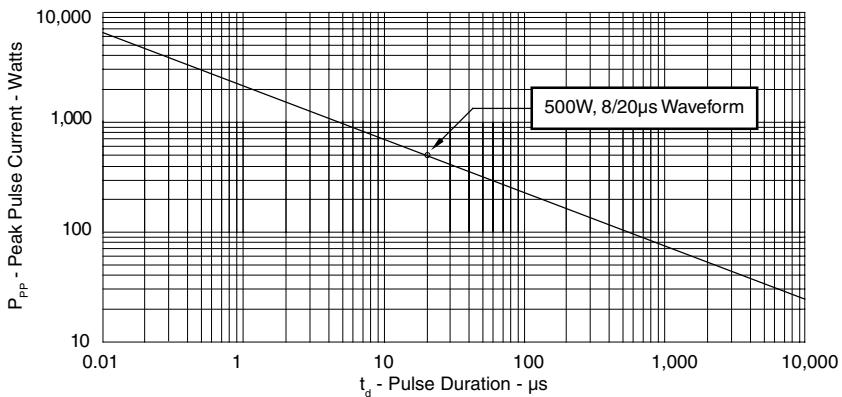
### ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified

PART NUMBER (Note 1)	DEVICE MARKING	RATED STAND-OFF VOLTAGE $V_{WM}$ VOLTS	MINIMUM BREAKDOWN VOLTAGE (See Note 2) $\text{@ } 1\text{mA}$ $V_{(BR)}$ VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) $\text{@ } I_F = 1\text{A}$ $V_C$ VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) $\text{@ } 8/20\mu\text{s}$ $V_C @ I_{PP}$	MAXIMUM LEAKAGE CURRENT $\text{@ } V_{WM}$ $I_D$ μA	TYPICAL CAPACITANCE $\text{@ } 0\text{V, } 1\text{ MHz}$ C pF
PSOT03LC	03L	3.3	4.0	7.0	10.9V @ 43.0A	125	5
PSOT05LC	05L	5.0	6.0	9.8	13.5V @ 42.0A	20	5
PSOT08LC	08L	8.0	8.5	13.4	16.9V @ 34.0A	10	5
PSOT12LC	12L	12.0	13.3	19.0	25.9V @ 21.0A	1	5
PSOT15LC	15L	15.0	16.7	24.0	30.0V @ 17.0A	1	5
PSOT24LC	24L	24.0	26.7	43.0	49.0V @ 12.0A	1	5
PSOT36LC	36L	36.0	40.0	51.0	76.8V @ 9.0A	1	5

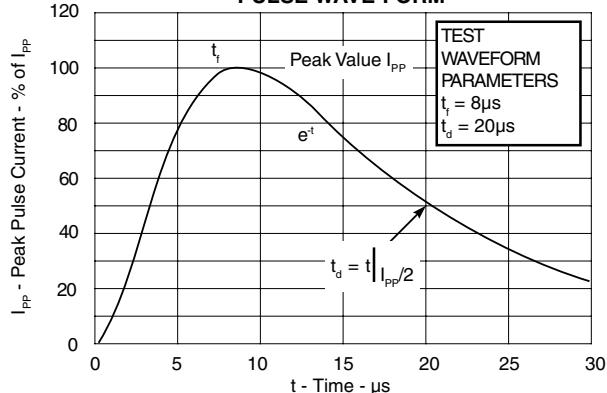
**Note 1:** Positive potential is applied from pin 1 to 2; pin 2 is ground.

**Note 2:** Do not test or surge from pin 2 to 1. PIV typically greater than 100V for the rectifier diode.

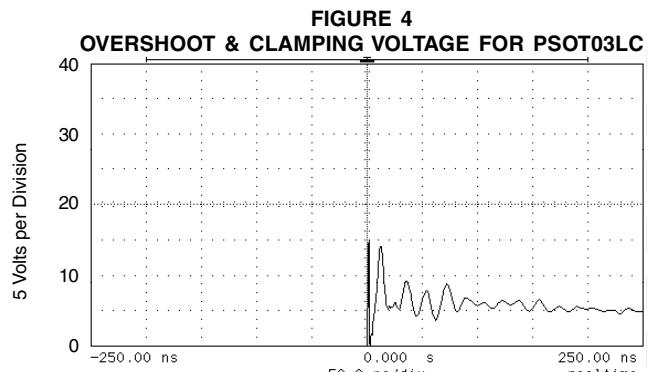
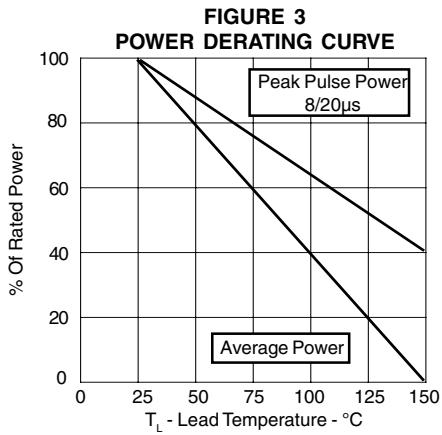
**FIGURE 1**  
PEAK PULSE POWER VS PULSE TIME



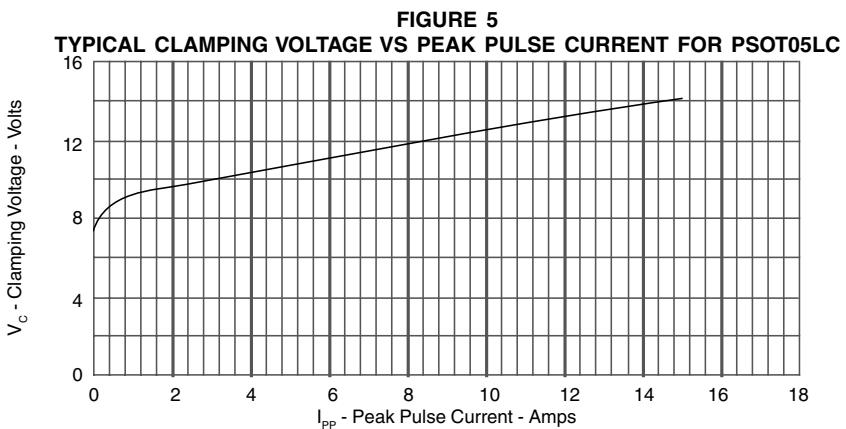
**FIGURE 2**  
PULSE WAVE FORM



## GRAPHS



ESD Test Pulse: 7 kilovolt, 1/30ns (waveform)



## APPLICATION NOTE

The PSOTxxLC Series are low capacitance TVS arrays designed to protect I/O or data lines from the damaging effects of ESD or EFT. This product series provides unidirectional & bidirectional protection, with a surge capability of 500 Watts  $P_{PP}$  per line for an 8/20 $\mu$ s waveform and ESD protection > 40 kilovolts.

### BIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 1)

Two PSOTxxLC devices, when used in parallel, provide protection in a common-mode configuration as depicted in Figure 1.

Circuit connectivity is as follows:

- ✓ I/O Line is connected to Device 1, Pin 1.
- ✓ I/O Line is connected to Device 2, Pin 2.
- ✓ Device 1, Pin 2 is connected to ground.
- ✓ Device 2, Pin 1 is connected to ground.
- ✓ Device 1 & 2, Pin 3 is not connected.

### BIDIRECTIONAL DIFFERENTIAL-MODE CONFIGURATION (Figure 1)

In addition, two PSOTxxLC devices, when used in parallel, provide protection in a differential-mode configuration for Ethernet applications as depicted in Figure 2.

Circuit connectivity is as follows:

- ✓ I/O Line 1 is connected to Device 1, Pin 1.
- ✓ I/O Line 1 is connected to Device 2, Pin 2.
- ✓ I/O Line 2 is connected to Device 1, Pin 1.
- ✓ I/O Line 2 is connected to Device 2, Pin 2.
- ✓ Device 1 & 2, Pin 3 is not connected.

### CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Figure 1 - Common-Mode I/O Port Protection

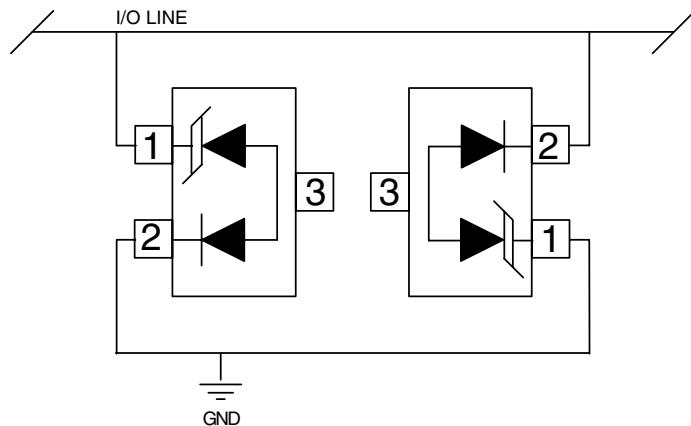
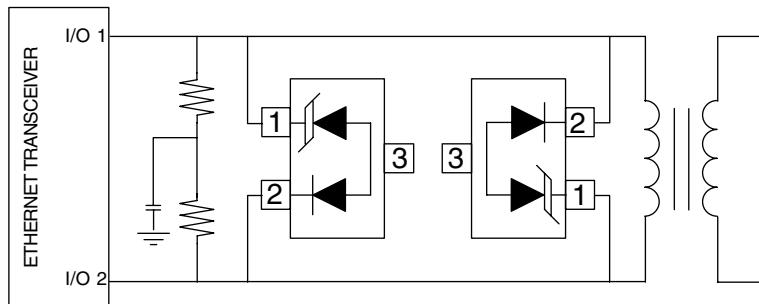
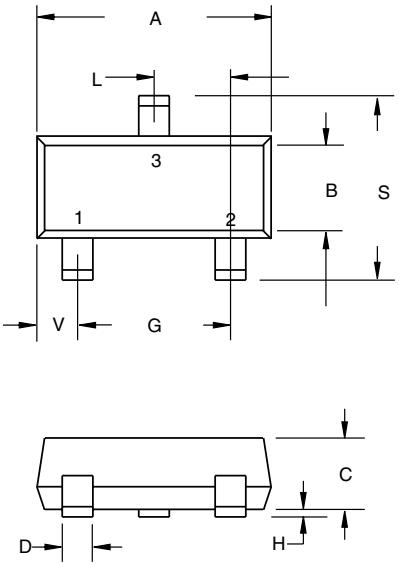


Figure 2 - Differential-Mode Ethernet Protection



## PACKAGE OUTLINE & DIMENSIONS

PACKAGE OUTLINE		SOT-23																																																																	
																																																																			
		<b>PACKAGE DIMENSIONS</b> <table border="1"> <thead> <tr> <th rowspan="2">DIM</th><th colspan="2">MILLIMETERS</th><th colspan="2">INCHES</th></tr> <tr> <th>MIN</th><th>MAX</th><th>MIN</th><th>MAX</th></tr> </thead> <tbody> <tr> <td>A</td><td>2.80</td><td>3.04</td><td>0.1102</td><td>0.1197</td></tr> <tr> <td>B</td><td>1.20</td><td>1.40</td><td>0.0472</td><td>0.0551</td></tr> <tr> <td>C</td><td>0.89</td><td>1.11</td><td>0.0350</td><td>0.0440</td></tr> <tr> <td>D</td><td>0.37</td><td>0.50</td><td>0.0150</td><td>0.0200</td></tr> <tr> <td>G</td><td>1.78</td><td>2.04</td><td>0.0701</td><td>0.0807</td></tr> <tr> <td>H</td><td>0.013</td><td>0.100</td><td>0.0005</td><td>0.0040</td></tr> <tr> <td>J</td><td>0.085</td><td>0.177</td><td>0.0034</td><td>0.0070</td></tr> <tr> <td>K</td><td>0.45</td><td>0.60</td><td>0.0180</td><td>0.0236</td></tr> <tr> <td>L</td><td>0.89</td><td>1.02</td><td>0.0350</td><td>0.0401</td></tr> <tr> <td>S</td><td>2.10</td><td>2.50</td><td>0.0830</td><td>0.0984</td></tr> <tr> <td>V</td><td>0.45</td><td>0.60</td><td>0.0177</td><td>0.0236</td></tr> </tbody> </table>		DIM	MILLIMETERS		INCHES		MIN	MAX	MIN	MAX	A	2.80	3.04	0.1102	0.1197	B	1.20	1.40	0.0472	0.0551	C	0.89	1.11	0.0350	0.0440	D	0.37	0.50	0.0150	0.0200	G	1.78	2.04	0.0701	0.0807	H	0.013	0.100	0.0005	0.0040	J	0.085	0.177	0.0034	0.0070	K	0.45	0.60	0.0180	0.0236	L	0.89	1.02	0.0350	0.0401	S	2.10	2.50	0.0830	0.0984	V	0.45	0.60	0.0177	0.0236
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<b>MOUNTING PAD</b>		<b>NOTES</b> <ol style="list-style-type: none"> <li>Dimensioning and tolerances per ANSI Y14.5M, 1985.</li> <li>Controlling Dimension: Inches</li> <li>Pin 3 is the cathode (Unidirectional Only).</li> <li>Dimensions are exclusive of mold flash and metal burrs.</li> </ol> <b>TAPE &amp; REEL ORDERING NOMENCLATURE</b> <ol style="list-style-type: none"> <li>Surface mount product is taped and reeled in accordance with EIA-481.</li> <li>Suffix -T7 = 7 Inch Reel - 3,000 pieces per 8mm tape, i.e., PSOT05LC-T7.</li> <li>Suffix -T13 = 13 Inch Reel - 10,000 pieces per 8mm tape, i.e., PSOT05LC-T13.</li> </ol> <p><b>Outline &amp; Dimensions: Rev 1 - 11/01, 06012</b></p>																																																																	

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