



DAC1201KP-V



Monolithic Microprocessor-Compatible 12-Bit Resolution DIGITAL-TO-ANALOG CONVERTER

FEATURES

- COMPLETE D/A CONVERTER:
INTERNAL REFERENCE
 $\pm 10V$ OUTPUT OPERATIONAL AMPLIFIER
- MICROPROCESSOR INTERFACE LOGIC FOR A 4-, 8-,
12- OR 16-BIT BUS
- MONOTONICITY GUARANTEED 0°C to +70°C
- SETTLING TIME 7 μ s, MAX
- $\pm 12V$ to $\pm 15V$ POWER SUPPLY OPERATION
- 28-PIN MOLDED PLASTIC DIP
- LOWEST COST BUFFERED 12-BIT DAC

DESCRIPTION

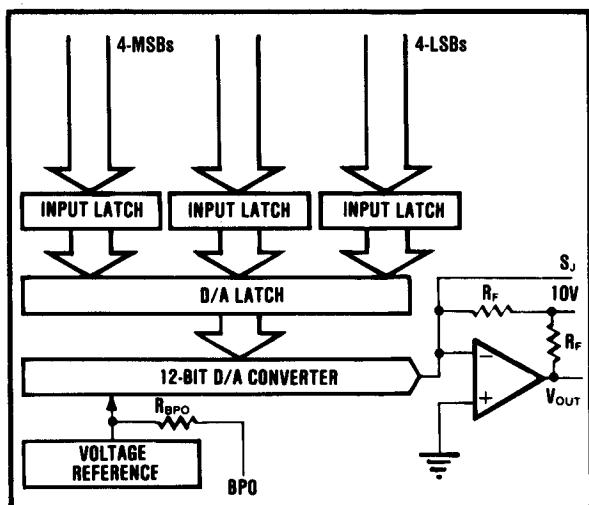
The low price of DAC1201 makes this 12-bit resolution D/A converter the best value available for commercial applications requiring a microprocessor interface.

The DAC1201 features microprocessor interface logic, TTL input compatibility, guaranteed monotonicity over 0°C to +70°C and settling time of 7 μ s maximum.

The interface logic is partitioned in 4-bit nibbles permitting 4-, 8-, 12- and 16-bit bus interface connections for right- or left-justified input words. Dual rank latches permit flexible timing operations for microprocessor control of the DAC1201.

This precision component is made possible using Burr-Brown's proprietary monolithic integrated circuit process which has been optimized for converter circuits. A stable subsurface reference zener, laser-trimmed thin-film ladder resistors, and high speed current switches combine to give superior performance over the rated temperature range.

DAC1201 is priced and specified for applications where high resolution and monotonicity are the key application parameters and where tightly specified performance over temperature is not required. Because of the low price, it is feasible to use this 12-bit D/A converter for new applications in communications systems, electronic controllers, medical instrumentation, electronic games and personal computer peripherals.



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SPECIFICATIONS

ELECTRICAL

Typical at $+25^{\circ}\text{C}$ and $\pm V_{\text{cc}} = 12\text{V}$ or 15V , $V_{\text{dd}} = +5\text{V}$ unless otherwise noted.

MODEL	DAC1201KP-V	UNITS
INPUTS		
DIGITAL INPUTS		
Input Code ⁽¹⁾	USB, BOB	
Resolution	12	Bits
Digital Logic Inputs ⁽²⁾ :		
V_{IH} , min to max	+2.4 to $+V_{\text{cc}}$	V
V_{IL} , min to max	0 to +0.8	V
I_{IH} , $V_{\text{I}} = +2.7\text{V}$, max	+20	μA
I_{IL} , $V_{\text{I}} = +0.4\text{V}$, max	± 30	μA
TRANSFER CHARACTERISTICS		
ACCURACY		
Linearity Error, max ⁽³⁾	± 0.018	% of FSR ⁽⁴⁾
Differential Linearity Error, max	± 0.024	% of FSR
Gain Error, max ⁽⁵⁾⁽⁶⁾	± 0.3	%
Unipolar Offset Error ⁽⁵⁾⁽⁷⁾	± 20	mV
Bipolar Offset Error, max ⁽⁵⁾⁽⁸⁾	± 40	mV
Monotonicity Over 0°C to $+70^{\circ}\text{C}$ ⁽⁹⁾	12	Bits
Sensitivity of Gain to Power		
Supply Variations:		
$+V_{\text{cc}}$ and $-V_{\text{cc}}$	± 0.002	% of FSR/% V_{cc}
V_{dd}	± 0.006	% of FSR/% V_{dd}
TEMPERATURE COEFFICIENTS		
Gain	± 10	ppm/ $^{\circ}\text{C}$
Bipolar Zero ⁽¹⁰⁾	± 6	ppm of FSR/ $^{\circ}\text{C}$
SETTLING TIME (to $\pm 0.012\%$ of FSR) ⁽¹¹⁾		
20V step and $2\text{k}\Omega$ load, max	7	μs
OUTPUT		
ANALOG OUTPUT		
Voltage Range, min ⁽¹²⁾	$\pm 5, \pm 10, +10$	V
Current, min ⁽¹³⁾	± 5	mA
Impedance	0.2	Ω
REFERENCE OUTPUT		
Voltage ⁽¹⁴⁾	+6.3	V
Source Current Available for External Loads, max	+1.5	mA
Temperature Coefficient	± 10	ppm/ $^{\circ}\text{C}$
POWER SUPPLY REQUIREMENTS		
RATED VOLTAGE		
$+V_{\text{cc}} - V_{\text{cc}}$ ⁽¹⁵⁾⁽¹⁶⁾	+15/-15	V
V_{dd} ⁽¹⁷⁾	+5	V
CURRENT (no load), max ⁽¹⁸⁾		
$+V_{\text{cc}} - V_{\text{cc}}$	+25/-35	mA
V_{dd}	+15	mA
TEMPERATURE RANGE		
For parameters specified over temp, min to max	0 to $+70$	$^{\circ}\text{C}$
Storage, min to max	-60 to $+100$	$^{\circ}\text{C}$

NOTES: (1) USB = Unipolar Straight Binary, BOB = Bipolar Offset Binary. (2) Digital inputs are TTL-compatible for V_{dd} over the range of $+4.5\text{V}$ to 5.5V . Digital input specs are guaranteed over 0°C to $+70^{\circ}\text{C}$. The specs are tested at 25°C only. (3) $\pm 0.018\%$ of FSR is 3/4LSB for 12 bits. (4) FSR means Full-Scale Range and is 20V for a $\pm 10\text{V}$ range. (5) Adjustable to zero with external potentiometer. (6) Adjusting the Gain Adjust potentiometer rotates the transfer function about 0V for unipolar operation and about minus full scale ($-FS$) for bipolar operation. (7) Error at input code 000_H for unipolar operation (output at 0V). (8) Error at input code 000_H for bipolar operation (output at minus full scale, $-FS$). (9) Guaranteed. Tested at 25°C only. (10) Drift at 0V output for bipolar operation (input code 100_H). (11) Guaranteed. Not tested. (12) Minimum supply voltage required for $\pm 10\text{V}$ output swing $\pm 13.5\text{V}$. Output swing for $\pm 11.4\text{V}$ supplies is at least -8V to $+8\text{V}$. (13) Output may be indefinitely shorted to Common without damage. (14) Tolerance is $\pm 5\%$. (15) The maximum voltage separation between ACOM and DCOM without affecting accuracy is $\pm 0.5\text{V}$. (16) Range

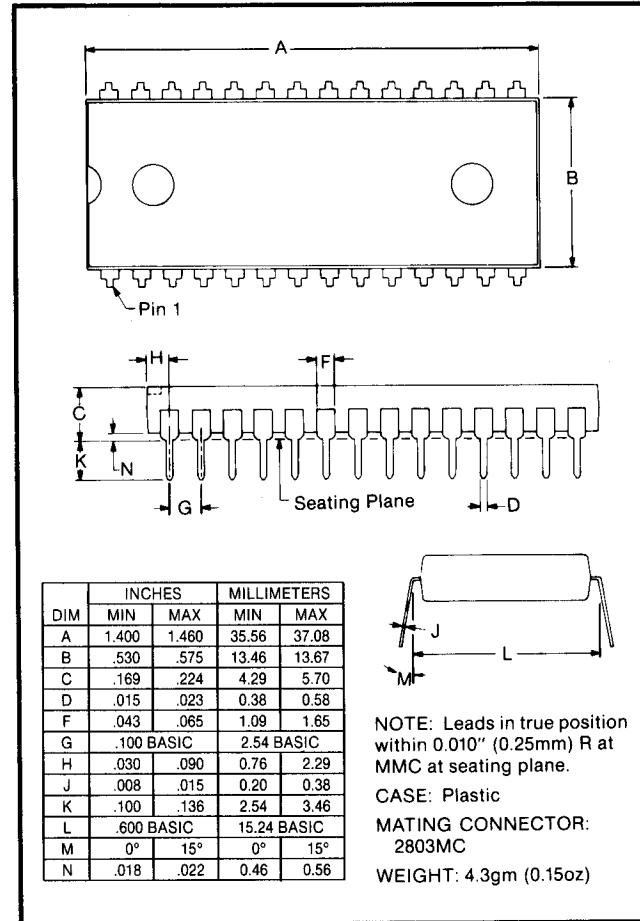
of operation is $\pm 11.4\text{V}$ to $\pm 16.5\text{V}$. (17) Range of operation is $+4.5\text{V}$ to $+5.5\text{V}$. (18) Typical power supply currents are approximately 70% of the maximum.

ABSOLUTE MAXIMUM RATINGS

+ V_{cc} to ACOM	0 to $+18\text{V}$
- V_{cc} to ACOM	0 to -18V
V_{dd} to DCOM	0 to $+7\text{V}$
V_{dd} to ACOM	$\pm 7\text{V}$
ACOM to DCOM	$\pm 7\text{V}$
Digital Inputs (pins 2-14, 16-19) to DCOM	-0.4V to $+18\text{V}$
External Voltage Applied to 10V Range Resistor	$\pm 12\text{V}$
REF OUT	Indefinite short to ACOM
External Voltage Applied to Analog Output	-5V to $+5\text{V}$
Power Dissipation	1000mW
Operating Temperature	0°C to $+70^{\circ}\text{C}$
Storage Temperature	-60°C to $+100^{\circ}\text{C}$

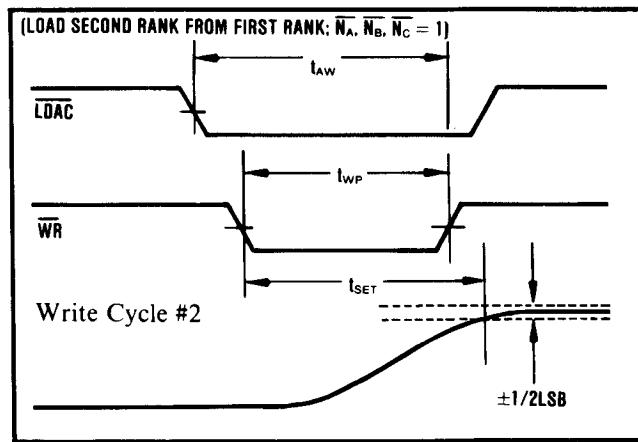
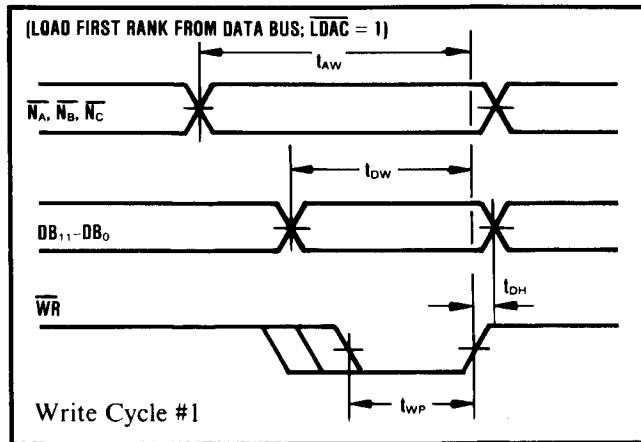
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

MECHANICAL



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TIMING DIAGRAMS



Digital Interface Timing Over Temperature Range:

t_{WP} , $\overline{\text{WR}}$ pulse width, min 50ns
 $\overline{\text{taw1}}, \overline{\text{Nx}}$ and $\overline{\text{LDAC}}$ valid to end of $\overline{\text{WR}}$, min 50ns

t_{DW} , data valid to end of $\overline{\text{WR}}$, min 80ns
 t_{DH} , data valid hold time, min 0ns

PIN NOMENCLATURE

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	V_{DD}	Logic Supply, +5V	14	D_4	DATA, Bit 5
2	$\overline{\text{WR}}$	WRITE, command signal to load latches. Logic low loads latches.	15	DCOM	DIGITAL COMMON, V_{DD} supply return
3	$\overline{\text{LDAC}}$	LOAD D/A CONVERTER, enables $\overline{\text{WR}}$ to load the D/A latch. Logic low enables.	16	D_0	DATA, Bit 1, LSB
4	$\overline{\text{N}}_A$	NYBBLE A, enables $\overline{\text{WR}}$ to load input latch A (the most significant nybble). Logic low enables.	17	D_1	DATA, Bit 2
5	$\overline{\text{N}}_B$	NYBBLE B, enables $\overline{\text{WR}}$ to load input latch B. Logic low enables.	18	D_2	DATA, Bit 3
6	$\overline{\text{N}}_C$	NYBBLE C, enables $\overline{\text{WR}}$ to load input latch C (the least significant nybble). Logic low enables.	19	D_3	DATA, Bit 4
7	D_{11}	DATA, Bit 12, MSB, positive true.	20	$+\text{V}_{\text{CC}}$	Analog Supply Input, +15V or +12V
8	D_{10}	DATA, Bit 11	21	$-\text{V}_{\text{CC}}$	Analog Supply Input, -15V or -12V
9	D_9	DATA, Bit 10	22	GAIN ADJ	To externally adjust gain
10	D_8	DATA, Bit 9	23	ACOM	ANALOG COMMON, $\pm \text{V}_{\text{CC}}$ supply return
11	D_7	DATA, Bit 8	24	V_{out}	D/A converter voltage output
12	D_6	DATA, Bit 7	25	10V RANGE	Connect to pin 24 for 10V Range
13	D_5	DATA, Bit 6	26	SJ	SUMMING JUNCTION of output amplifier
			27	BPO	BIPOLAR OFFSET. Connect to pin 26 for Bipolar Operation
			28	REF OUT	6.3V reference output

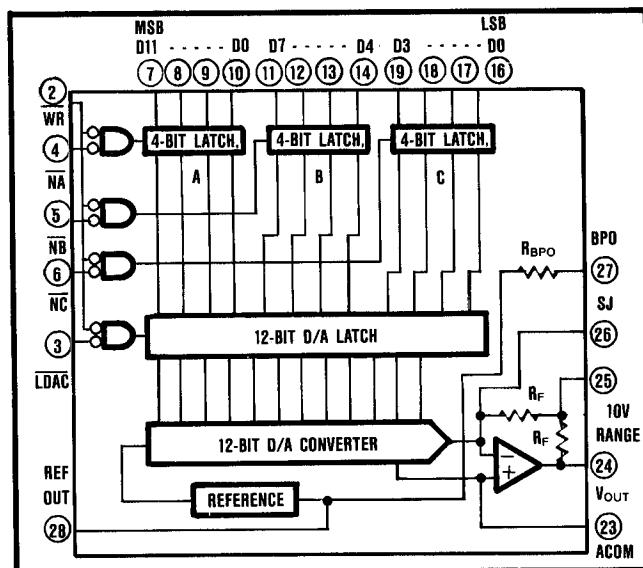


FIGURE 1. DAC1201 Block Diagram.

OPERATION

INTERFACE LOGIC

Input latches A, B, and C hold data temporarily while a complete 12-bit word is assembled before loading into the D/A register. This double-buffered organization prevents the generation of spurious analog output values. Each register is independently addressable.

These input latches are controlled by $\overline{\text{N}}_A$, $\overline{\text{N}}_B$, $\overline{\text{N}}_C$ and $\overline{\text{WR}}$. $\overline{\text{N}}_A$, $\overline{\text{N}}_B$, and $\overline{\text{N}}_C$ are internally NORed with $\overline{\text{WR}}$ so that the input latches transmit data when both $\overline{\text{N}}_A$ (or $\overline{\text{N}}_B$, $\overline{\text{N}}_C$) and $\overline{\text{WR}}$ are at logic "0". When either $\overline{\text{N}}_A$ (or $\overline{\text{N}}_B$, $\overline{\text{N}}_C$) or $\overline{\text{WR}}$ go to logic "1", the input data is latched into the input registers and held until both $\overline{\text{N}}_A$ (or $\overline{\text{N}}_B$, $\overline{\text{N}}_C$) and $\overline{\text{WR}}$ go to logic "0".

The D/A latch is controlled by $\overline{\text{LDAC}}$ and $\overline{\text{WR}}$. $\overline{\text{LDAC}}$ and $\overline{\text{WR}}$ are internally NORed so that the latches

transmit data to the D/A switches when both LDAC and WR are at logic "0". When either LDAC or WR are at logic "1", the data is latched in the D/A latch and held until LDAC and WR go to logic "0".

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for all latches is given in Table I.

TABLE I. DAC1201 Interface Logic Truth Table.

WR	N _A	N _B	N _C	LDAC	Operation
1	X	X	X	X	No Operation
0	0	1	1	1	Enables Input Latch 4MSBs
0	1	0	1	1	Enables Input Latch 4 Middle Bits
0	1	1	0	1	Enables Input Latch 4LSBs
0	1	1	1	0	Loads D/A Latch From Input Latches
0	0	0	0	0	All Latches Transparent

"X" = Don't Care.

GAIN AND OFFSET ADJUSTMENTS

Figures 2 and 3 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

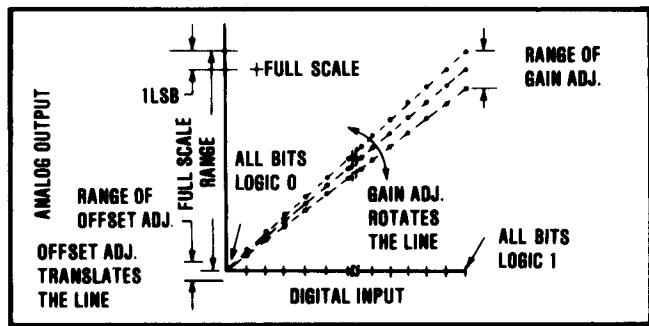


FIGURE 2. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

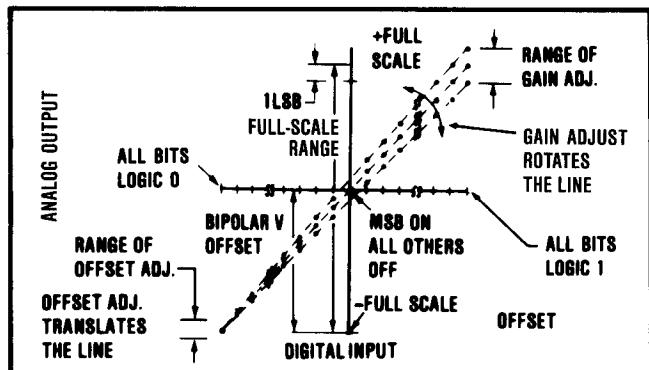


FIGURE 3. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the Offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full-scale voltage. Example: If the full-scale range

is connected for 20V, the maximum negative output voltage is -10V. See Table II for corresponding codes.

TABLE II. Digital Input/Analog Output, $\pm V_{CC} = \pm 15V$.

Digital Input	Analog Output		
12-Bit Resolution	0 to + 10V	$\pm 5V$	$\pm 10V$
MSB LSB	↓ ↓		
111111111111	+9.9976V	+4.9976V	+9.9951V
100000000000	+5.0000V	0.0000V	0.0000V
011111111111	+4.9976V	-0.0024V	-0.0049V
000000000000	0.0000V	-5.0000V	-10.0000V
1LSB	2.44mV	2.44mV	4.88mV

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages.

$\pm 12V$ OPERATION

The DAC1201 is fully specified for operation on $\pm 12V$ power supplies. However, in order for the output to swing to $\pm 10V$, the power supplies must be $\pm 13.5V$ or greater. When operating with $\pm 12V$ supplies, the output swing should be restricted to $\pm 8V$ in order to meet specifications.

INSTALLATION POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram, Figure 4.

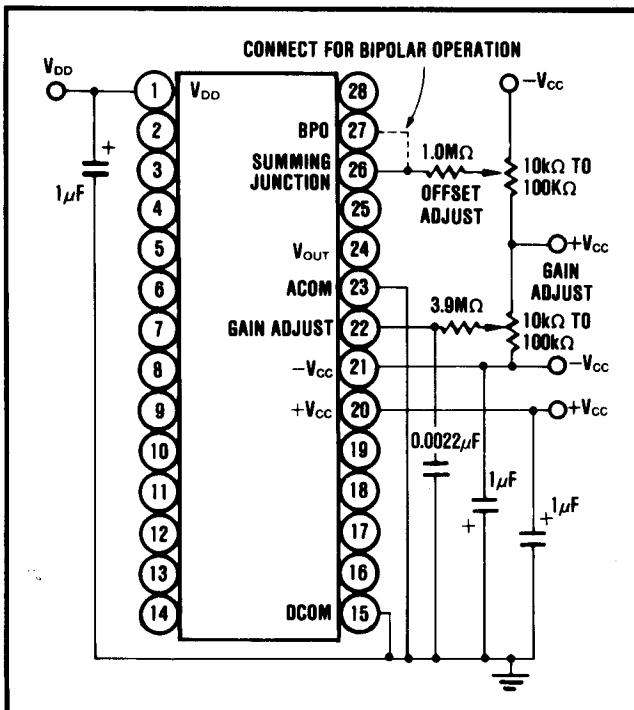


FIGURE 4. Power Supply, Gain, and Offset Potentiometer Connections.

These capacitors (1 μ F to 10 μ F tantalum recommended) should be located close to the DAC1201.

The DAC1201 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. The Analog Common (pin 23) and Digital Common (pin 15) should be connected together at one point. Separate returns minimize current flow in low-level signal paths if properly connected. Logic return currents are not added into the analog signal return path. A $\pm 0.5V$ difference between ACOM and DCOM is permitted for specified operation. High frequency noise on DCOM with respect to ACOM may permit noise to be coupled through to the analog output; therefore, some caution is required in applying these common connections.

The Analog Common is the high quality return for the D/A converter and should be connected directly to the analog reference point of the system. The load driven by the output amplifier should be returned to the Analog Common.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 4. TCR of the potentiometers should be 100ppm/ $^{\circ}$ C or less. The 1.0M Ω and 3.9M Ω resistors (20% carbon or better) should be located close to the DAC1201 to prevent noise pick-up. If it is not convenient to use these high value resistors, and equivalent "T" network, as shown in Figure 5, may be substituted in each case. The Gain Adjust (pin 22) is a high impedance point and a 0.001 μ F to 0.01 μ F ceramic capacitor should be connected from this pin to Analog Common to reduce noise pick-up in all applications, including those not employing external gain adjustment.

OUTPUT RANGE CONNECTIONS

Internal-scaling resistors provided in the DAC1201 may be connected to produce bipolar output voltage ranges of $\pm 10V$ and $\pm 5V$ or unipolar output voltage range of 0

to +10V. The 20V range ($\pm 10V$ bipolar range) is internally connected. Refer to Figure 6. Connections for the output ranges are listed in Table III.

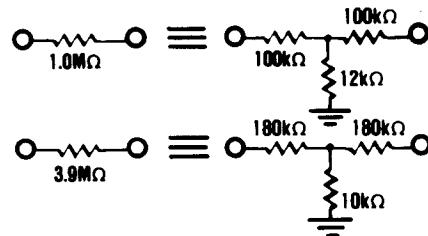


FIGURE 5. Equivalent Resistances.

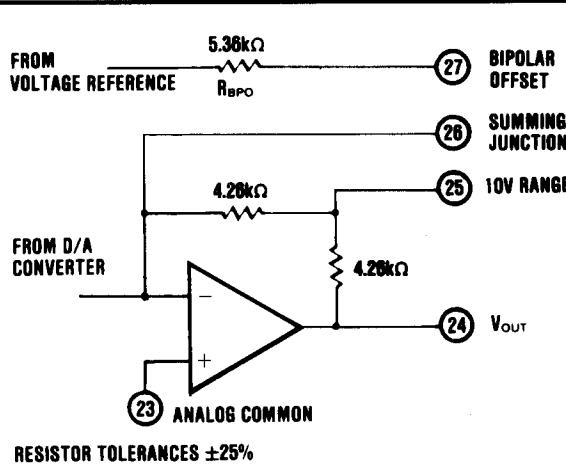


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

TABLE III. Output Range Connections.

Output Range	Digital Input Codes	Connect Pin 25 To	Connect Pin 27 To
0 to +10V	USB	24	23
±5V	BOB or BTC	24	26
±10V	BOB or BTC	NC	26

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