

# 74LV74

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 3 — 9 September 2013

Product data sheet

## 1. General description

The 74LV74 is a dual positive edge triggered, D-type flip-flop. It has individual data ( $nD$ ) inputs, clock ( $nCP$ ) inputs, set ( $nSD$ ) and ( $nRD$ ) inputs, and complementary  $nQ$  and  $n\bar{Q}$  outputs.

The set and reset are asynchronous active LOW inputs that operate independently of the clock input. Information on the data input is transferred to the  $nQ$  output on the LOW-to-HIGH transition of the clock pulse. The  $nD$  inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

## 2. Features and benefits

- Wide supply voltage range from 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Direct interface with TTL levels (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114-A exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV74N	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74LV74D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV74DB	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV74PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1



### 4. Functional diagram

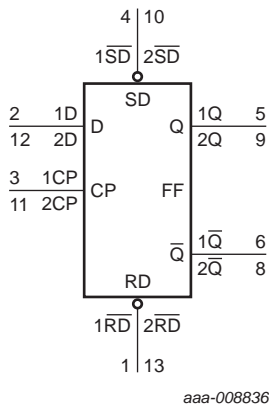


Fig 1. Logic symbol

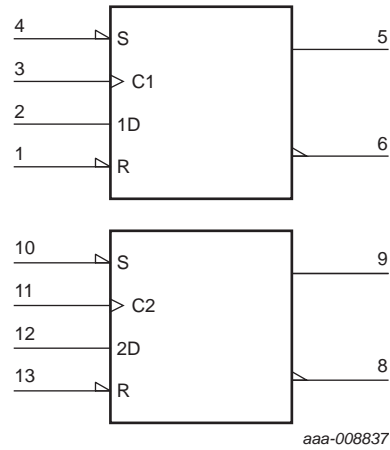


Fig 2. IEC logic symbol

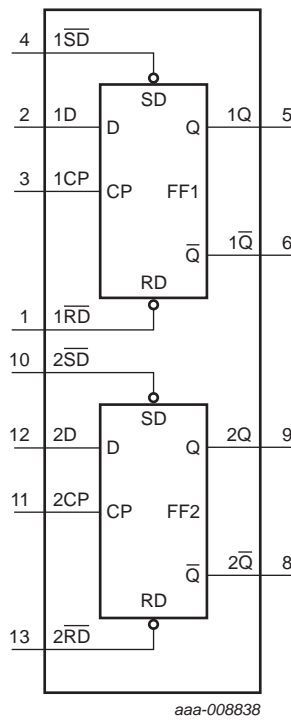


Fig 3. Functional diagram

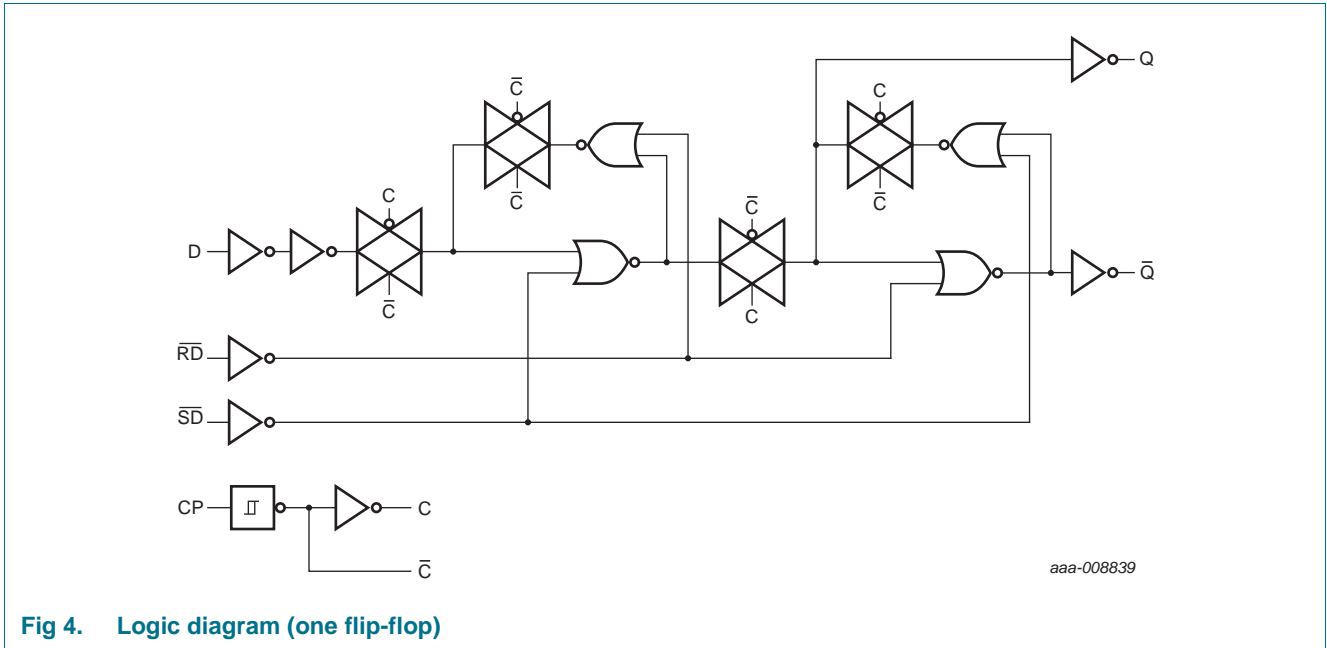


Fig 4. Logic diagram (one flip-flop)

## 5. Pinning information

### 5.1 Pinning

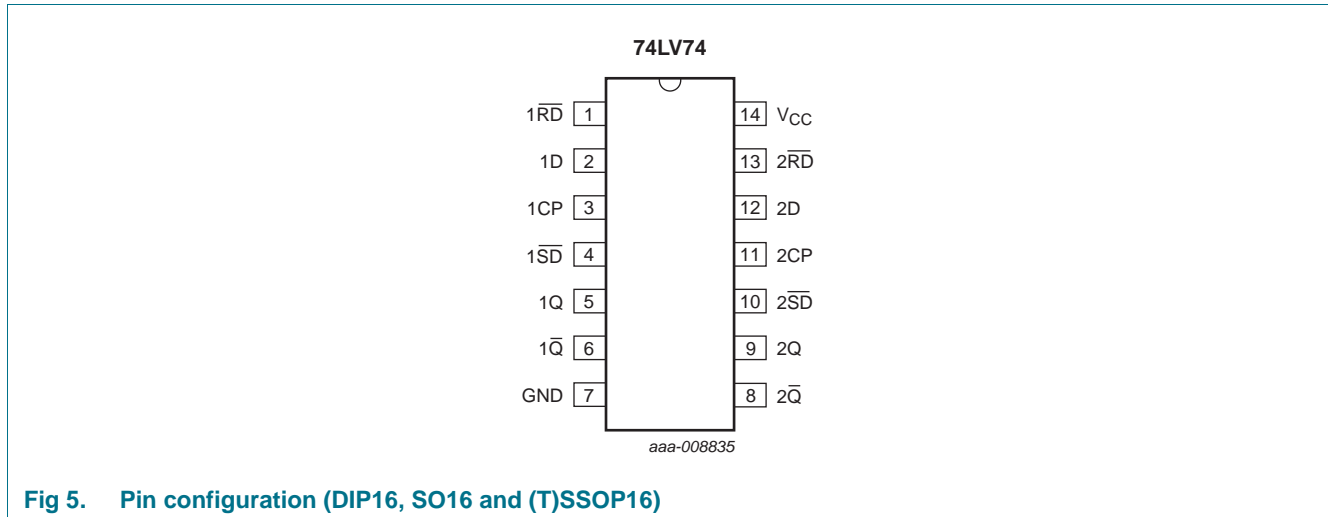


Fig 5. Pin configuration (DIP16, SO16 and (T)SSOP16)

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{1RD}$	1	asynchronous reset-direct input (active-LOW)
1D	2	data inputs
1CP	3	clock input (LOW-to-HIGH), edge-triggered)
$\overline{1SD}$	4	asynchronous set-direct input (active-LOW)
1Q	5	true flip-flop outputs
$\overline{1Q}$	6	complement flip-flop outputs
GND	7	ground (0 V)
$\overline{2Q}$	8	complement flip-flop outputs
2Q	9	true flip-flop outputs
$\overline{2SD}$	10	asynchronous set-direct input (active-LOW)
2CP	11	clock input (LOW-to-HIGH), edge-triggered)
2D	12	data inputs
$\overline{2RD}$	13	asynchronous reset-direct input (active-LOW)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Input				Output			
nSD	nRD	nCP	nD	nQ	nQ̄	Q <sub>n+1</sub>	nQ̄ <sub>n+1</sub>
L	H	X	X	H	L	-	-
H	L	X	X	L	H	-	-
L	L	X	X	H	H	-	-
H	H	↑	L	-	-	L	H
H	H	↑	H	-	-	H	L

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 ↑ = LOW-to-HIGH clock transition;  
 Q<sub>n+1</sub> = state after the next LOW-to-HIGH CP transition

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		[1] -0.5	+7	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	-	20	mA
V <sub>I</sub>	input voltage		[1] -0.5	+7	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	-	±50	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	±50	mA
I <sub>GND</sub>	ground current		-	±50	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C			
		DIP16 package	[2] -	750	mW
		SO16 package	[3] -	500	mW
		(T)SSOP16 package	[4] -	400	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2] P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.  
 [3] P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.  
 [4] P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage <sup>[1]</sup>		1.0	3.3	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V to }2.0\text{ V}$	0	-	500	ns/V
		$V_{CC} = 2.0\text{ V to }2.7\text{ V}$	0	-	200	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0	-	100	ns/V
		$V_{CC} = 3.6\text{ V to }5.5\text{ V}$	0	-	50	ns/V

[1] LV is guaranteed to function down to  $V_{CC} = 1.0\text{ V}$  (input levels GND or  $V_{CC}$ ); DC characteristics are guaranteed from  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 5.5\text{ V}$ .

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit	
			Min	Typ <sup>[1]</sup>	Max	Min	Max		
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	0.9	-	-	0.9	-	V	
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.4	-	-	1.4	-	V	
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>	-	-	0.7 × V <sub>CC</sub>	-	V	
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.3	-	0.3	V	
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.6	-	0.6	V	
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V	
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3 × V <sub>CC</sub>	-	0.3 × V <sub>CC</sub>		
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100 μA							
		V <sub>CC</sub> = 1.2 V	-	1.2	-	-	-		
		V <sub>CC</sub> = 2.0 V	1.8	2.0	-	1.8	-	V	
		V <sub>CC</sub> = 2.7 V	2.5	2.7	-	2.5	-	V	
		V <sub>CC</sub> = 3.0 V	2.8	3.0	-	2.8	-	V	
		V <sub>CC</sub> = 4.5 V	4.3	4.5	-	4.3	-	V	
		standard outputs: V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>							
		V <sub>CC</sub> = 3.0 V; I <sub>O</sub> = -6 mA	2.40	2.82	-	2.20	-	V	
V <sub>CC</sub> = 4.5 V; I <sub>O</sub> = -12 mA	3.60	4.20	-	3.50	-	V			
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100 μA							
		V <sub>CC</sub> = 1.2 V	-	0	-	-	-		
		V <sub>CC</sub> = 2.0 V	-	0	0.2	-	0.2	V	
		V <sub>CC</sub> = 2.7 V	-	0	0.2	-	0.2	V	
		V <sub>CC</sub> = 3.0 V	-	0	0.2	-	0.2	V	
		V <sub>CC</sub> = 4.5 V	-	0	0.2	-	0.2	V	
		standard outputs: V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>							
		V <sub>CC</sub> = 3.0 V; I <sub>O</sub> = 6 mA	-	0.25	0.40	-	0.50	V	
V <sub>CC</sub> = 4.5 V; I <sub>O</sub> = 12 mA	-	0.35	0.55	-	0.65	V			
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±1	-	±1	μA	
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	20	-	80	μA	
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	500	-	850	μA	
C <sub>I</sub>	input capacitance		-	3.5	-			pF	

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

GND (ground = 0 V): for test circuit, see [Figure 8](#)

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nCP to nQ, n $\bar{Q}$ ; see <a href="#">Figure 6</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	70	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	24	44	-	56	ns
		V <sub>CC</sub> = 2.7 V	-	18	28	-	41	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	13	26	-	33	ns
		V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 15 pF	-	11	-	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[4]</sup>	-	9.5	17	-	23	ns
		n $\bar{S}$ D to nQ, n $\bar{Q}$ ; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.2 V	-	90	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	31	46	-	58	ns
		V <sub>CC</sub> = 2.7 V	-	23	34	-	43	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	17	27	-	34	ns
		V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 15 pF	-	14	-	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[4]</sup>	-	12	19	-	24	ns
		n $\bar{R}$ D to nQ, n $\bar{Q}$ ; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.2 V	-	90	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	31	46	-	58	ns
		V <sub>CC</sub> = 2.7 V	-	23	34	-	43	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	17	27	-	34	ns
		V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 15 pF	-	14	-	-	-	ns
V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[4]</sup>	-	12	19	-	24	ns		
t <sub>w</sub>	pulse width	nCP input HIGH to LOW; see <a href="#">Figure 6</a>						
		V <sub>CC</sub> = 2.0 V	34	10	-	41	-	ns
		V <sub>CC</sub> = 2.7 V	25	8	-	30	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	20	7	-	24	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[4]</sup>	15	6	-	18	-	ns
		n $\bar{S}$ D or n $\bar{R}$ D pulse width LOW; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 2.0 V	34	10	-	41	-	ns
		V <sub>CC</sub> = 2.7 V	25	8	-	30	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	20	7	-	24	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[4]</sup>	15	6	-	18	-	ns



**Table 7. Dynamic characteristics ...continued**  
 GND (ground = 0 V): for test circuit, see [Figure 8](#)

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>rec</sub>	recovery time	nRD; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.2 V	-	5	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	14	2	-	15	-	ns
		V <sub>CC</sub> = 2.7 V	10	1	-	11	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	8	1	-	9	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[4]</sup>	6	1	-	7	-	ns
t <sub>su</sub>	set-up time	nD to nCP; see <a href="#">Figure 6</a>						
		V <sub>CC</sub> = 1.2 V	-	10	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	22	4	-	26	-	ns
		V <sub>CC</sub> = 2.7 V	12	3	-	15	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	8	2	-	10	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[4]</sup>	6	1	-	8	-	ns
t <sub>h</sub>	hold time	nD to nCP; see <a href="#">Figure 6</a>						
		V <sub>CC</sub> = 1.2 V	-	-10	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	3	-2	-	3	-	ns
		V <sub>CC</sub> = 2.7 V	3	-2	-	3	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	3	-2	-	3	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	3	-2	-	3	-	ns
f <sub>max</sub>	maximum frequency	nCP; see <a href="#">Figure 6</a>						
		V <sub>CC</sub> = 2.0 V	14	40	-	12	-	MHz
		V <sub>CC</sub> = 2.7 V	50	90	-	40	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	60	100	-	48	-	MHz
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[4]</sup>	70	110	-	56	-	MHz
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[5]</sup>	-	24	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

[2] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.

[3] Typical value measured at V<sub>CC</sub> = 3.3 V.

[4] Typical values are measured at V<sub>CC</sub> = 5.0 V.

[5] C<sub>PD</sub> is used to determine the dynamic power dissipation P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> + Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) (P<sub>D</sub> in μW), where:

f<sub>i</sub> = input frequency in MHz;

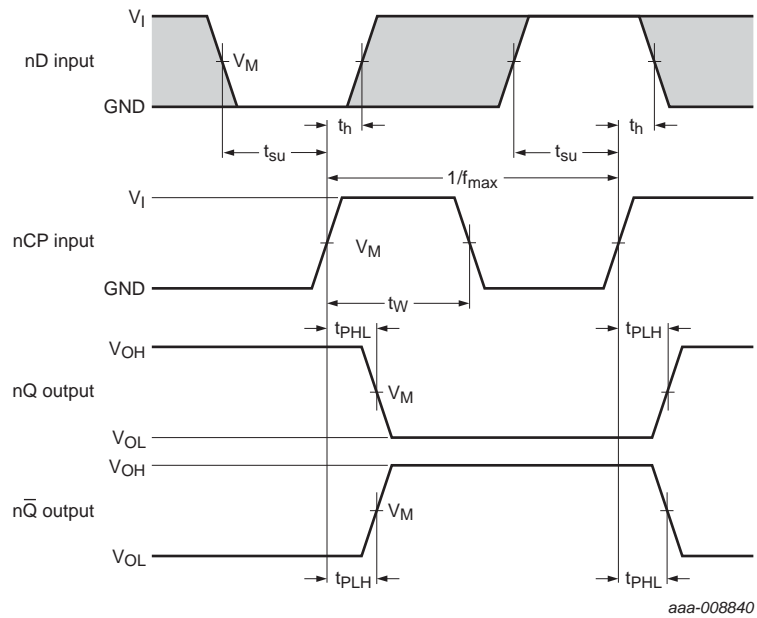
f<sub>o</sub> = output frequency in MHz;

Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V.

11. Waveforms

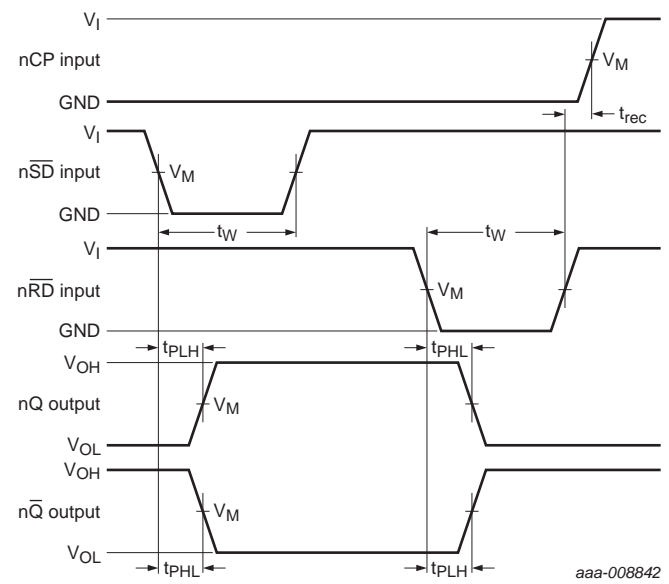


aaa-008840

Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 6. Clock pulse (nCP) to output (nQ, nQ-bar) propagation delays, nCP pulse width and maximum frequency**



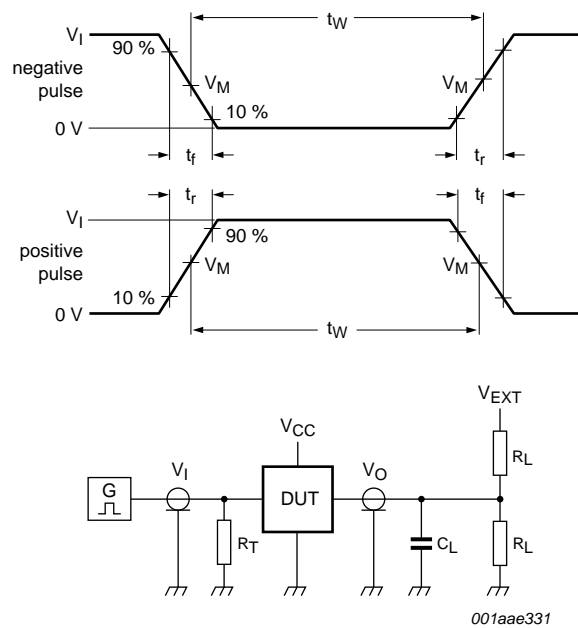
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Measurement points are given in [Table 8](#).

**Fig 7. The set (nSD) and reset (nRD) input to output (nQ, nQ-bar) propagation delays, the set and reset pulse widths and the nRD to nCP recovery time**

Table 8. Measurement points

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
$\geq 4.5$ V	$0.5V_{CC}$	$0.5V_{CC}$



001aae331

Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		$V_{EXT}$
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$
< 2.7 V	$V_{CC}$	2.5 ns	50 pF	1 k $\Omega$	open
2.7 V to 3.6 V	2.7 V	2.5 ns	50 pF, 15 pF	1 k $\Omega$	open
$\geq 4.5$ V	$V_{CC}$	2.5 ns	50 pF	1 k $\Omega$	open

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

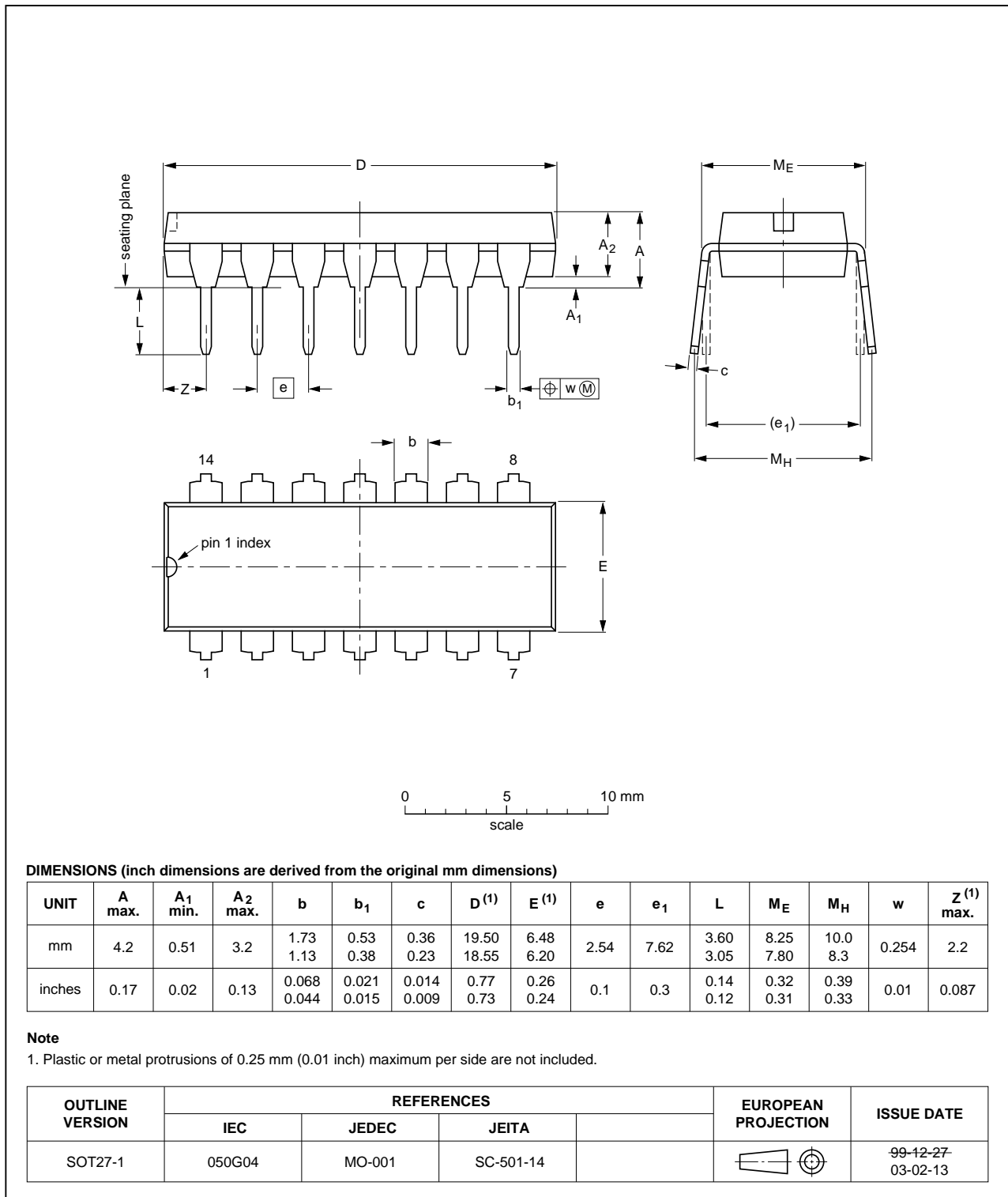


Fig 9. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

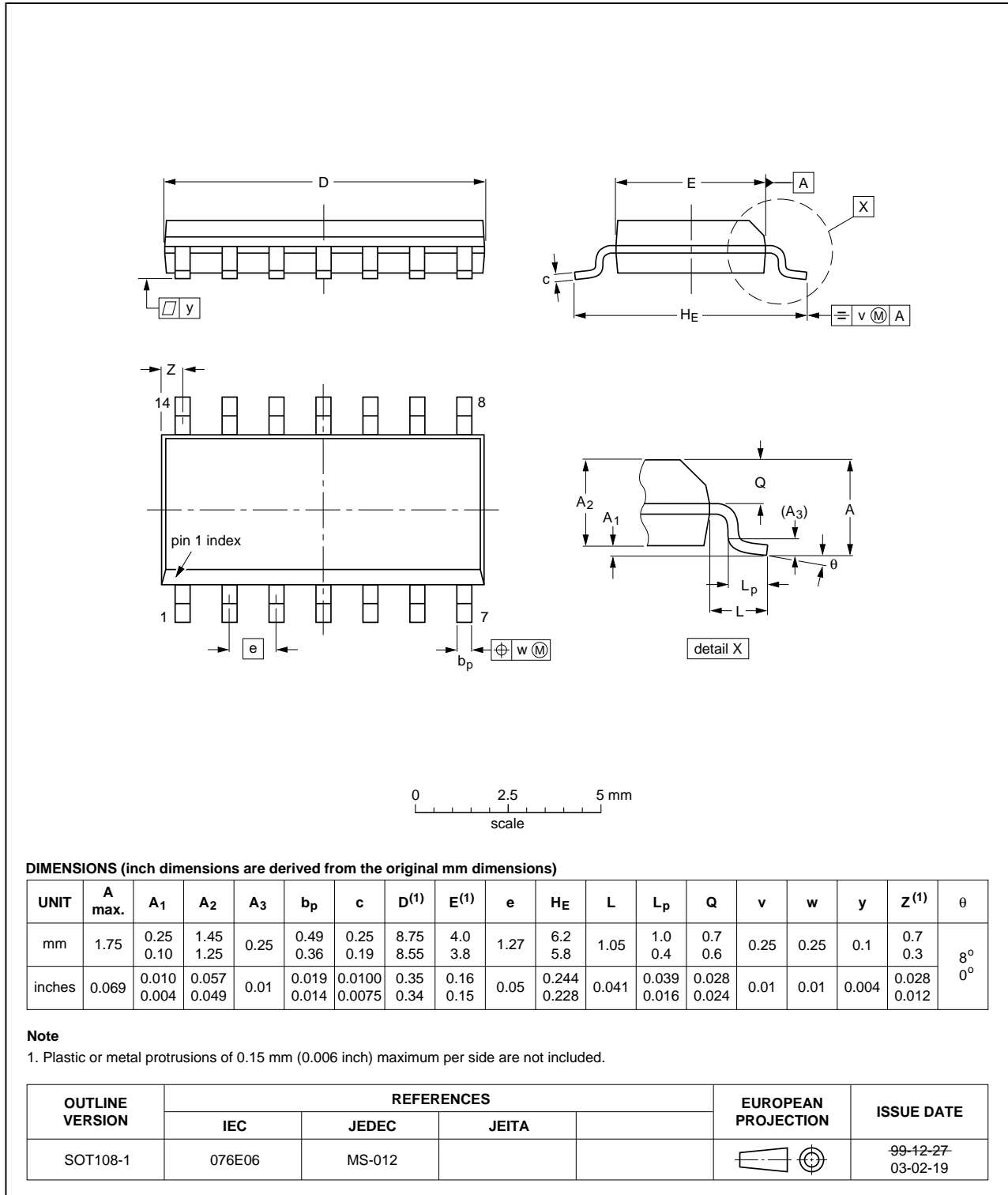


Fig 10. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

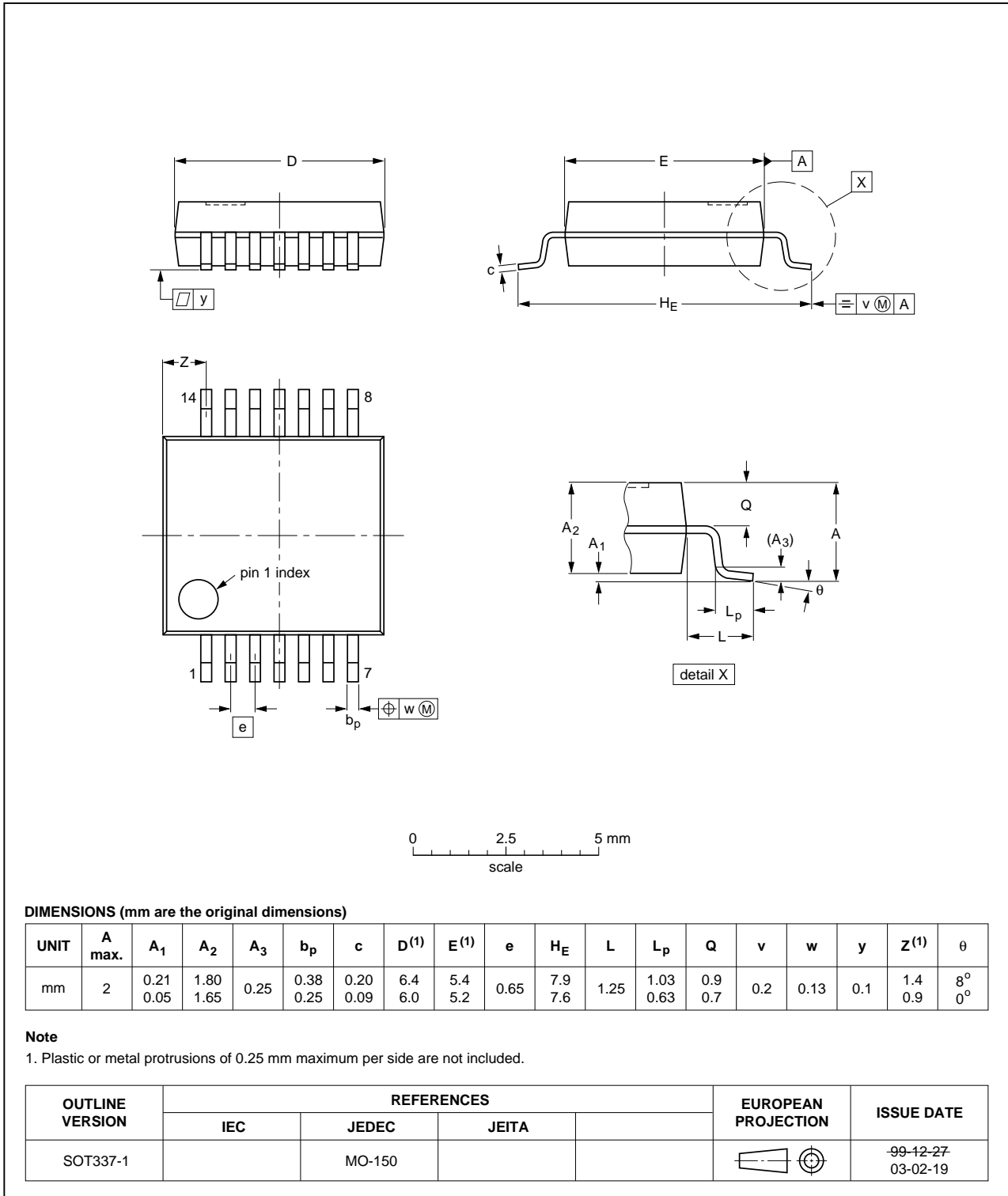


Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

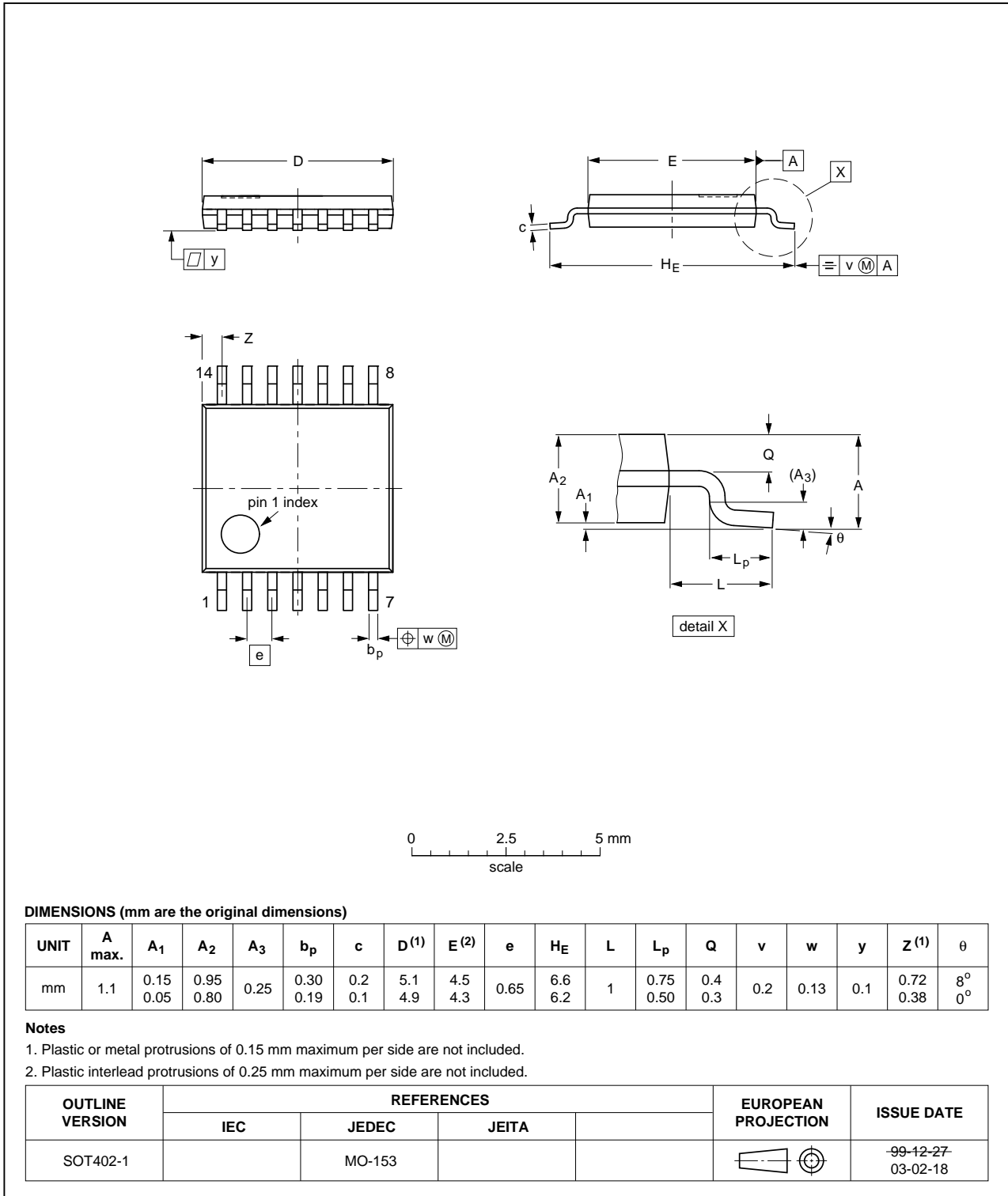


Fig 12. Package outline SOT402-1 (TSSOP14)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV74 v.3	20130909	Product data sheet	-	74LV74_CNV v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Family data added, see <a href="#">Section 9 "Static characteristics"</a></li> </ul>			
74LV74_CNV v.2	April 1998	Product specification	-	-



## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

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## Dual D-type flip-flop with set and reset; positive-edge trigger

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