

74F573

Octal D-Type Latch with 3-STATE Outputs

General Description

The 74F573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (\overline{OE}) inputs.

This device is functionally identical to the 74F373 but has different pinouts.

Features

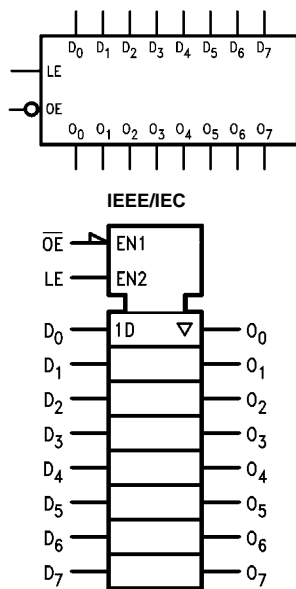
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 74F373
- 3-STATE outputs for bus interfacing
- Guaranteed 4000V minimum ESD protection

Ordering Code:

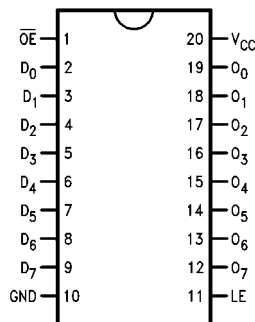
Order Number	Package Number	Package Description
74F573SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F573SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F573PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0-D_7	Data Inputs	1.0/1.0	20 μ A/-0.6 mA
LE	Latch Enable Input (Active HIGH)	1.0/1.0	20 μ A/-0.6 mA
\overline{OE}	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μ A/-0.6 mA
O_0-O_7	3-STATE Latch Outputs	150/40(33.3)	-3 mA/24 mA (20 mA)

Functional Description

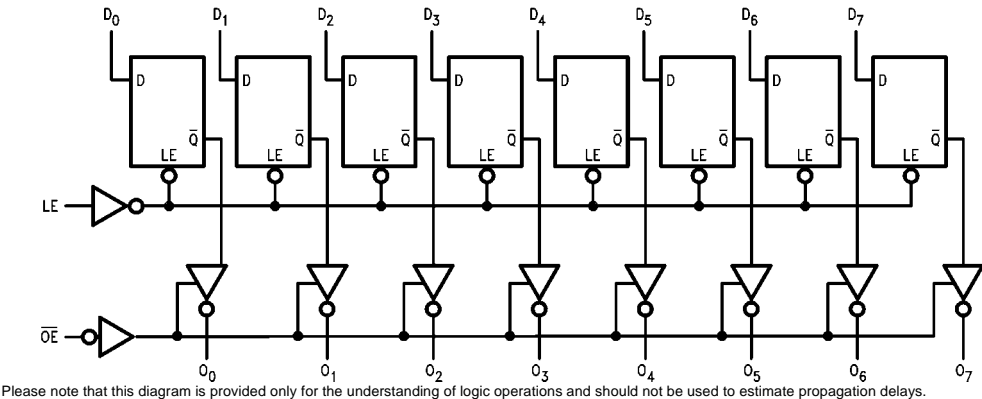
The 74F573 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

Inputs			Outputs
\overline{OE}	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 O_0 = Value stored from previous clock cycle

Logic Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

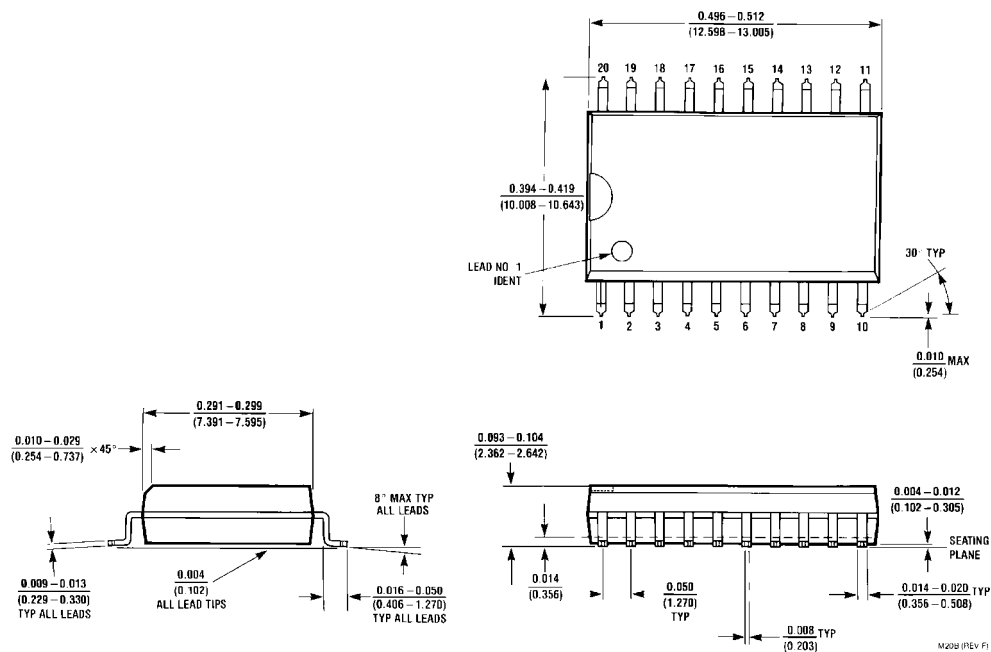
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 10% V _{CC} 5% V _{CC} 5% V _{CC}	2.5 2.4 2.7 2.7		V	Min	I _{OH} = −1 mA I _{OH} = −3 mA I _{OH} = −1 mA I _{OH} = −3 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 24 mA
I _{IH}	Input HIGH Current			20.0 5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−0.6	mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			−50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current	−60		−150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CCL}	Power Supply Current		35	55	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		35	55	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = +5.0V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.0	5.3	7.0	3.0	9.0	3.0	8.0	ns
t _{PHL}	D _n to O _n	2.0	3.7	6.0	2.0	7.0	2.0	6.5	
t _{PLH}	Propagation Delay	5.0	9.0	11.0	5.0	13.5	5.0	12.0	ns
t _{PHL}	LE to O _n	3.0	5.2	7.0	3.0	7.5	3.0	7.0	
t _{PZH}	Output Enable Time	2.0	5.0	8.0	2.0	10.0	2.0	9.0	ns
t _{PZL}		2.0	5.6	8.5	2.0	10.0	2.0	9.5	
t _{PHZ}	Output Disable Time	1.5	4.5	5.5	1.5	7.0	1.5	6.5	
t _{PLZ}		1.5	3.8	5.5	1.5	5.5	1.5	5.5	

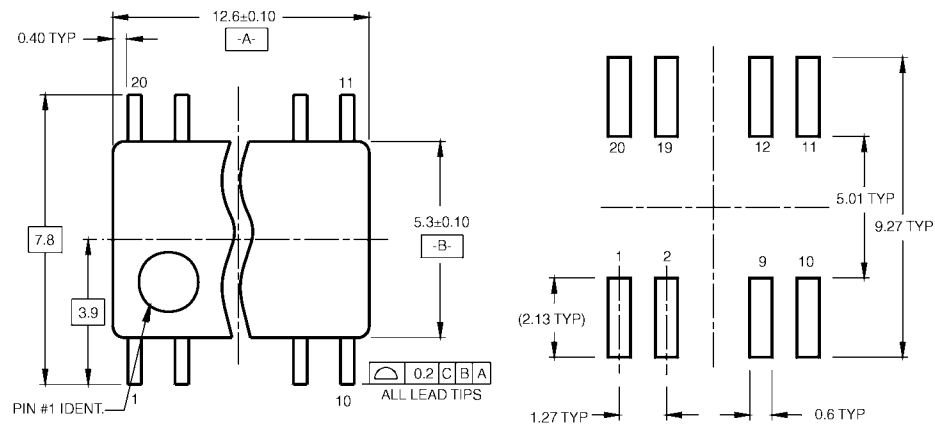
AC Operating Requirements

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = -55°C to +125°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = +5.0V		Units
		Min	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	2.0		2.0		2.0		ns
t _S (L)	D _n to LE	2.0		2.0		2.0		
t _H (H)	Hold Time, HIGH or LOW	3.0		3.0		3.0		
t _H (L)	D _n to LE	3.5		4.0		3.5		
t _W (H)	LE Pulse Width, HIGH	4.0		4.0		4.0		ns

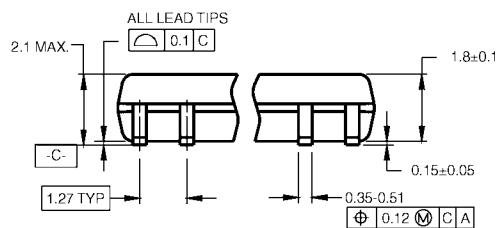
Physical Dimensions inches (millimeters) unless otherwise noted


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B**

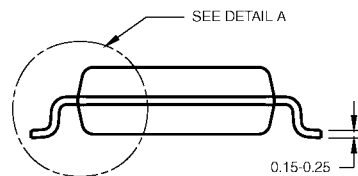
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



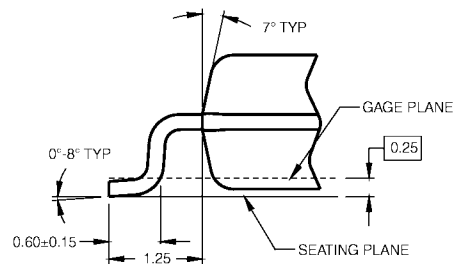
DIMENSIONS ARE IN MILLIMETERS



NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

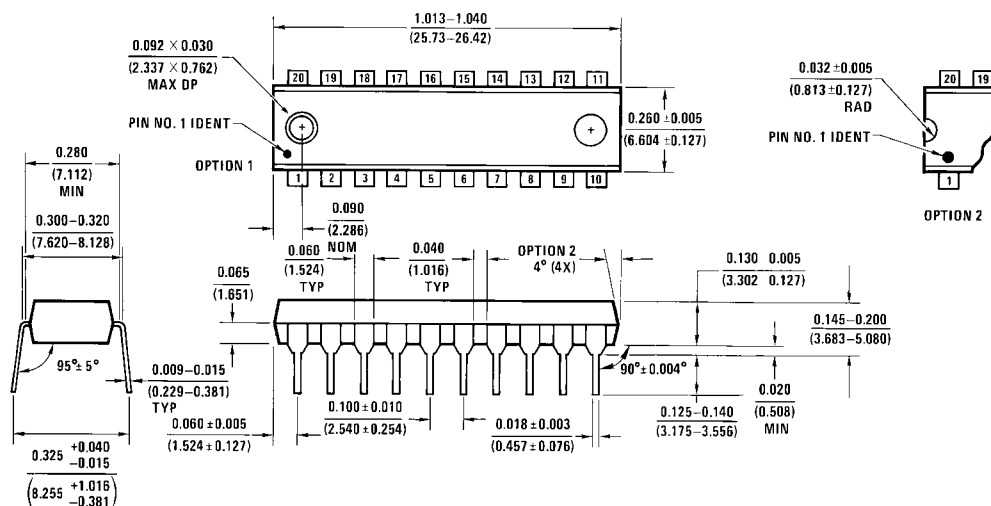
M20DRevB1



DETAIL A

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

N20A (REV G)

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