OptiMOS™3 Power MOS Transistor Chip

IPC302N20NFD

Type	$V_{(BR)DSS}$	$R_{DS(on)}$	Die size	Si-thickness
IPC302N20NFD	200 V	12 mΩ[1)]	6.7 x 4.5mm^2	250 µm

Description

- N-channel enhancement mode
- For dynamic characterization refer to the datasheet of IPP120N20NFD
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
- Die bond: soldered or glued
- Backside metallization: NiV system
- Frontside metallization: AlSiCu system
- Passivation: nitride and polymide (only on edge structure)

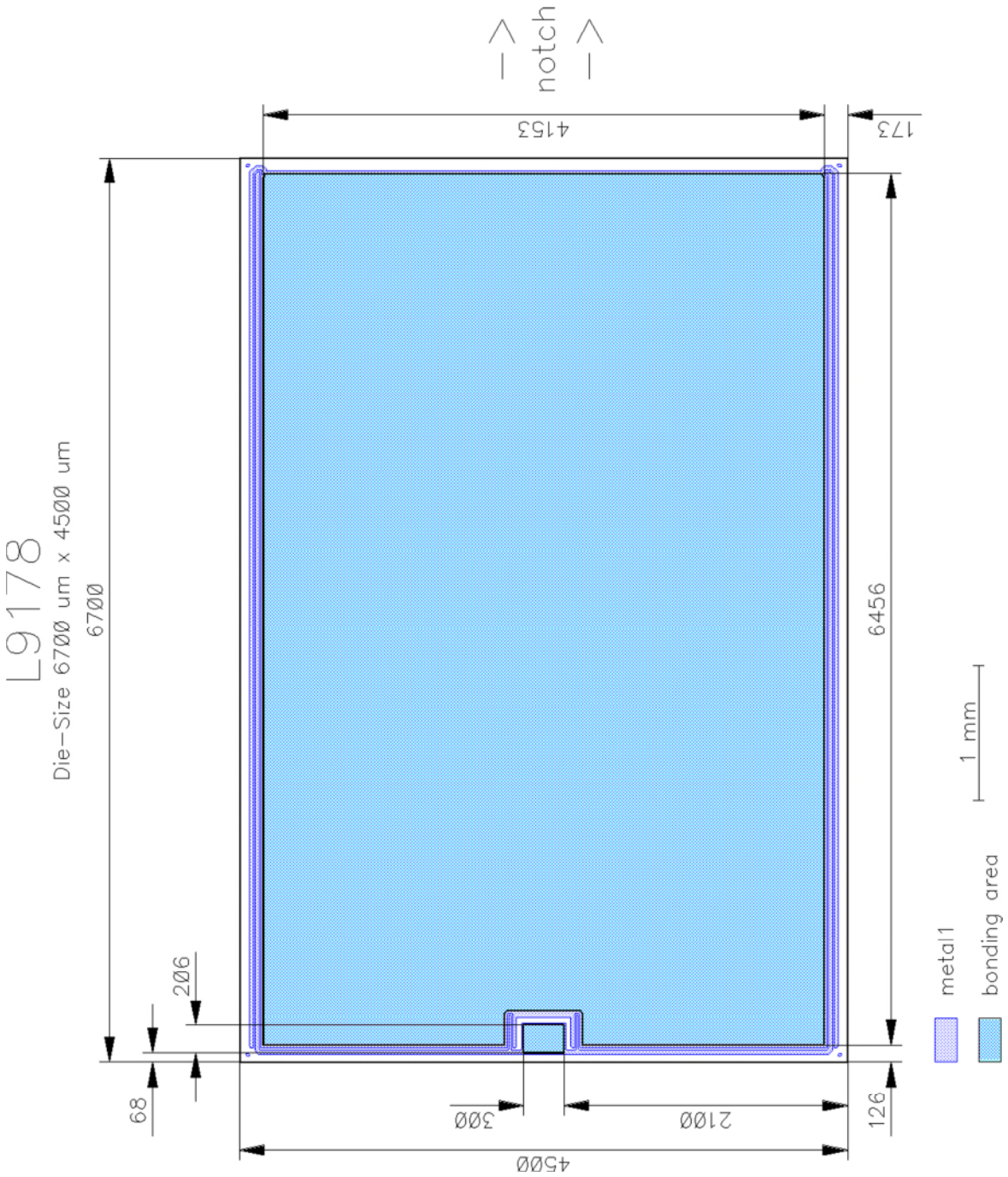
1 Electrical Characteristics on Wafer Level

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Value			Unit	Conditions
		min.	typ.	max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	200	-	-	V	V_{GS} = 0V I_D = 1 mA
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	V_{DS} = V_{GS} I_D = 270 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{GS} = 0V V_{DS} = 160 V
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS} = 20 V V_{DS} = 0 V
Drain-source on-resistance	$R_{DS(on)}$	-	9.4[2)]	100 [3)]	mΩ	V_{GS}= 10 V I_D= 2.0 A
Reverse diode forward on-voltage	V_{SD}	-	0.65	1.2	V	V_{GS}=0 V I_F= 1 A
Avalanche energy, single pulse	E_{AS}	-	45 [4)]	-	mJ	I_D= 30 A, R_{GS}=25Ω

[1)] packaged in a PG-TO220-3 (see ref. product)
[2)] typical bare die $R_{DS(on)}$; V_{GS}=10V
[3)] limited by wafer test-equipment
[4)] Wafer tested. For general avalanche capability refer to the datasheet of IPP120N20NFD

2 Chip Layout



Revision History

Major changes since the last revision

Page or Reference	Description of change
Rev. 2.0	Release of final version

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