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April 2015

FAN25800 — 500 mA, Low- I_Q , Low-Noise, LDO Regulator

FAN25800

500 mA, Low- I_Q , Low-Noise, LDO Regulator

Features

- V_{IN} : 2.3 V to 5.5 V
- V_{OUT} = 2.7 V, 3.3 V (I_{OUT} Max. = 500 mA)
- V_{OUT} = 2.8 V (I_{OUT} Max. = 250 mA)
- Output Noise Density at 250 mA and 10 kHz = 19 nV/ $\sqrt{\text{Hz}}$ (Integrated 8 μV_{rms})
- Low I_Q of 17 μA in Regulation and Low- I_Q Dropout Mode with Optimized Dropout Transitions
- <70 mV Dropout Voltage at 250 mA Load
- Controlled Soft-Start to Reduce Inrush Current
- Thermal Shutdown Protection (TSD)
- Input Under-Voltage Lockout (UVLO)
- Short-Circuit Protection (SCP)
- Stable with Two 1.5 μF , 0201 Ceramic Capacitors at V_{OUT}
- 4-Ball WLCSP, 0.65 mm x 0.65 mm, 0.35 mm Pitch, Plated Solder, 330 μm Maximum Thickness

Description

The FAN25800 is a linear low-dropout regulator with a high PSRR (85 dB at 100 Hz) and low output noise (typically 8 μV_{RMS} over a 10 Hz to 100 kHz bandwidth). The LDO can provide up to 500 mA of output current.

The enable control pin can be used to shut down the device and disconnect the output load from the input. During shutdown, the supply current drops below 1 μA .

The FAN25800 is designed to be stable with space-saving ceramic capacitors as small as 0201 case size. The FAN25800 is available in a 4-bump, 0.35 mm pitch, WLCSP package.

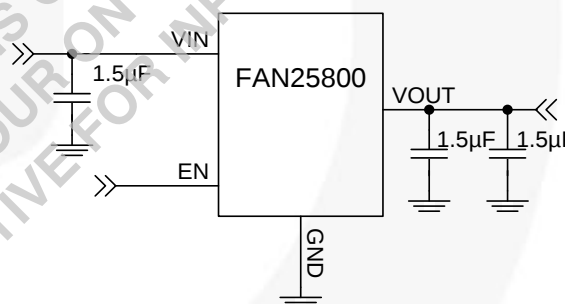


Figure 1. Typical Application

Applications

- WiFi Modules
- PDA Handsets
- Smart Phones, Tablets, Portable Devices

Ordering Information

Part Number ⁽¹⁾	V_{OUT}	I_{OUT_MAX}	Operating Temperature	Package	Packing Method
FAN25800AUC33X	3.3 V	500 mA	-40°C to 85°C	4-Bump, WLCSP, 0.65 x 0.65 mm, 0.35 mm Pitch	Tape & Reel
FAN25800AUC28X	2.8 V	250 mA			
FAN25800AUCF27X	2.7 V	500 mA			

Note:

1. For other trim options, please contact a Fairchild representative.

Block Diagram

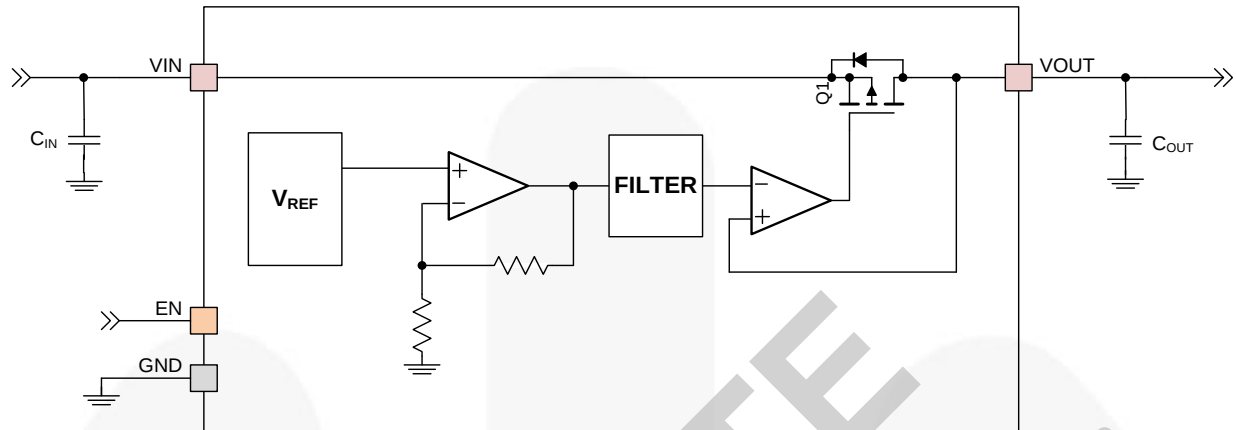


Figure 2. IC and System Block Diagram

Table 1. Recommended External Components

Component	Description	Vendor	Parameter	Typ.	Unit
C_{IN}	1.5 μ F, 6.3 V, X5R, 0201	Murata GRM033R60J155M	C	1.5 ⁽²⁾	μ F
C_{OUT}	2x1.5 μ F, 6.3 V, X5R, 0201	Murata GRM033R60J155M		1.5 ⁽²⁾	μ F
$C_{Alternative}^{(3)}$	1.0 μ F, 6.3 V, X5R, 0201	Murata GRM033R60J105M		1.0 ⁽²⁾	μ F

Notes:

- Capacitance value does not reflect effects of bias, tolerance, and temperature. See *Recommended Operating Conditions* and *Operation Description* sections for more information.
- $C_{Alternative}$ can be used for both C_{IN} and C_{OUT} . FAN25800 is stable with one 1 μ F at C_{IN} and one 1 μ F at C_{OUT} .

Pin Configuration

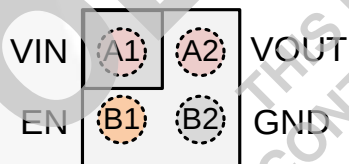


Figure 3. Top-Through View

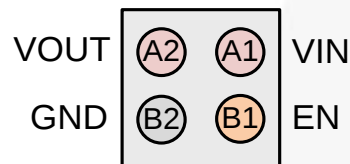


Figure 4. Bottom View

Pin Definitions

Pin #	Name	Description
A1	VIN	Input Voltage. Connect to input power source and C_{IN} .
A2	VOUT	Output Voltage. Connect to C_{OUT} and load.
B1	EN	Enable. The device is in Shutdown Mode when this pin is LOW. No internal pull-down. Do not leave this pin floating. Recommended to not tie EN pin directly to VIN. ⁽⁴⁾
B2	GND	Ground. Power and IC ground. All signals are referenced to this pin.

Note:

- Recommended to use logic voltage of 1.8 V to drive the EN pin.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V _{IN}	Input Voltage with Respect to GND		-0.3	6.0	V
V _{CC}	Voltage on Any Other Pin (with Respect to GND)		-0.3	V _{IN} +0.3 ⁽⁵⁾	V
T _J	Junction Temperature		-40	+150	°C
T _{STG}	Storage Temperature		-65	+150	°C
T _L	Lead Soldering Temperature, 10 Seconds			+260	°C
ESD	Electrostatic Discharge Protection Level	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	4000		V
		Charged Device Model per JESD22-C101	1500		
LU	Latch Up		JESD 78D		

Note:

5. Lesser of 6.0 V or V_{IN} + 0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{IN}	Supply Voltage	2.3		5.5 ⁽⁶⁾	V
I _{OUT_MAX} ⁽⁷⁾	Output Current (V _{OUT} = 2.7 V, 3.3 V)			500	mA
I _{OUT_Recommend}	Output Current (V _{OUT} = 3.3 V)			500	mA
	Output Current (V _{OUT} = 2.7 V, 2.8 V)			250	mA
C _{IN}	Input Capacitor (Effective Capacitance) ⁽⁸⁾	0.4	0.8		μF
C _{OUT}	Output Capacitor (Effective Capacitance) ⁽⁸⁾	0.4	0.8	15.0	μF
T _A	Ambient Temperature	-40		+85	°C
T _J	Junction Temperature	-40		+125	°C

Note:

6. For V_{IN} ≥ 3.4 V, thermal properties of the device must be taken into account at maximum load of 500 mA; refer to θ_{JA} thermal properties.
7. I_{OUT_MAX} is for V_{IN} = V_{OUT} + 0.3 V.
8. Effective capacitance, including the effects of bias, tolerance, and temperature. See the Operation Description section for more information.

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature, T_{J(max)}, at a given ambient temperature, T_A.

Symbol	Parameter	Typ.	Unit
θ _{JA}	Junction-to-Ambient Thermal Resistance	180	°C/W

Electrical Specifications

Minimum and maximum values are at $V_{IN} = V_{OUT} + 0.3\text{ V}$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; and test circuit shown in Figure 1. Typical values are at $V_{IN} = V_{OUT} + 0.3\text{ V}$, $T_A = 25^\circ\text{C}$, $I_{LOAD} = 10\text{ mA}$, and $V_{EN} = 1.8\text{ V}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
LDO						
I _{IN}	V _{IN} Supply Current	V _{IN} = V _{OUT} + 0.3 V to 4.2 V, I _{LOAD} = 0 mA		17.0	25.0	μA
		Dropout ⁽¹⁰⁾ , I _{LOAD} = 0 mA		18.5	30.0	
PSRR	Power Supply Rejection Ratio ⁽⁹⁾	I _{OUT} = 10 mA, V _{IN} = 3.6 V, V _{OUT} = 3.3 V	f = 50 Hz	84		dB
			f = 100 Hz	85		
			f = 1 kHz	84		
			f = 10 kHz	79		
		I _{OUT} = 250 mA, V _{IN} = 3.6 V, V _{OUT} = 3.3 V	f = 50 Hz	68		
			f = 100 Hz	73		
			f = 1 kHz	75		
			f = 10 kHz	76		
e _n	Output Noise Voltage Density ⁽⁹⁾	f = 10 kHz, V _{OUT} = 3.3 V	I _{OUT} = 10 mA	20	40	nV/√Hz
			I _{OUT} = 250 mA	19	39	
e _{n_bw}	Output Noise Voltage (Integrated) ⁽⁹⁾	f = 10 Hz – 100 kHz, V _{OUT} = 3.3 V	I _{OUT} = 10 mA	8	25	μV _{RMS}
			I _{OUT} = 250 mA	8	25	
V _{DO}	V _{OUT} Dropout Voltage ⁽¹⁰⁾	V _{OUT} = V _{OUT_TARGET} – 100 mV, I _{OUT} = 250 mA		70	130	mV
ΔV _{OUT}	V _{OUT} Voltage Accuracy	5 mA ≤ I _{OUT} ≤ I _{OUT_Recommend} , V _{IN} = V _{OUT} + 0.3 V to 4.2 V	-1.9		+1.9	%
ΔV _{OUT_LOAD}	Load Regulation	I _{OUT} = 5 mA to I _{OUT_MAX}		12	35	μV/mA
I _{LIM}	V _{OUT} Current Limit	I _{OUT} = 0 mA → Current Limit, V _{OUT} = 3.3 V, 2.7V, V _{OUT} Drops by 2%	550	650	800	mA
		I _{OUT} = 0 mA → Current Limit, V _{OUT} = 2.8 V, V _{OUT} Drops by 2%	275	323	400	
I _{SD}	Shutdown Supply Current	V _{EN} = 0 V, V _{IN} = V _{OUT} + 0.3 V to 4.2 V		0.125	1.000	μA
V _{UVLO}	Under-Voltage Lockout Threshold	Rising V _{IN}		2.1	2.3	V
V _{UVHYS}	Under-Voltage Lockout Hysteresis			150		mV
t _{START}	Startup Time	Rising EN to 95% V _{OUT} , I _{OUT} = 10 mA		250	500	μs
TSD	Thermal Shutdown	Rising Temperature		150		°C
		Hysteresis		20		
Logic Levels: EN						
V _{I_H}	Enable High-Level Input Voltage		1.05			V
V _{I_L}	Enable Low-Level Input Voltage				0.4	V
I _{EN}	Input Bias Current	V _{EN} = 1.8 V		0.04	1.00	μA

Notes:

9. Guaranteed by design; not tested in production.

10. Dropout voltage = $V_{IN} - V_{OUTX}$ when V_{OUT} drops more than 100 mV below the nominal regulated V_{OUT} level.

Typical Characteristics

Unless otherwise specified; $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $T_A = +25^\circ\text{C}$, and test circuit per Figure 1.

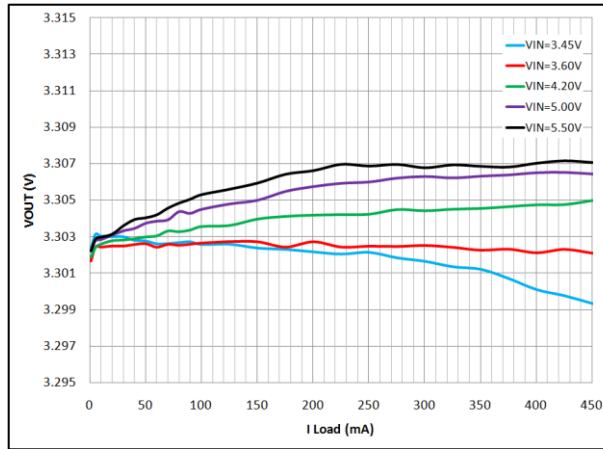


Figure 5. Output Regulation vs. Load Current and Input Voltage

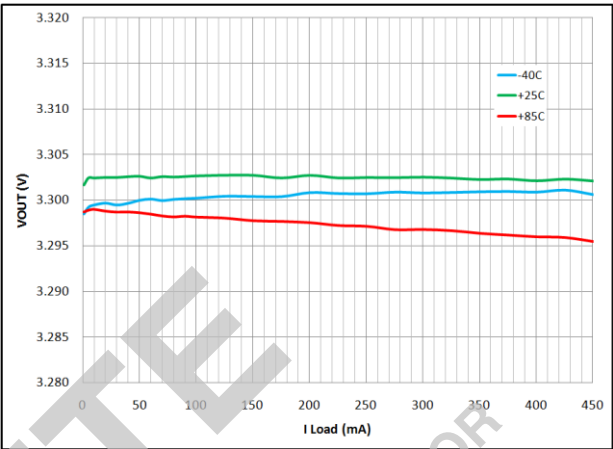


Figure 6. Output Regulation vs. Load Current and Temperature

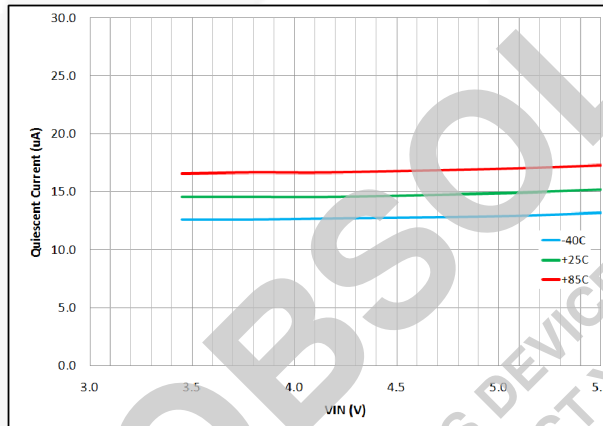


Figure 7. Quiescent Current vs. Input Voltage and Temperature

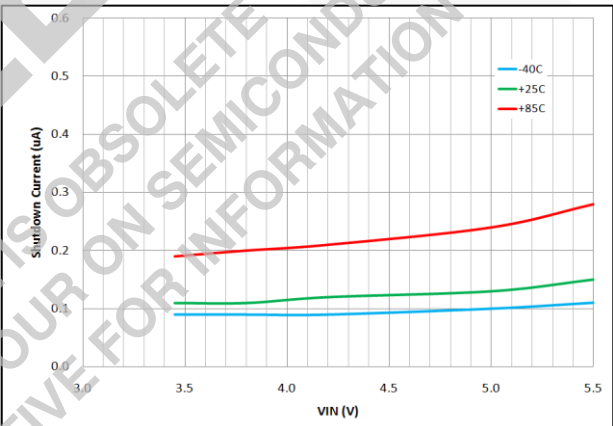


Figure 8. Shutdown Current vs. Input Voltage and Temperature

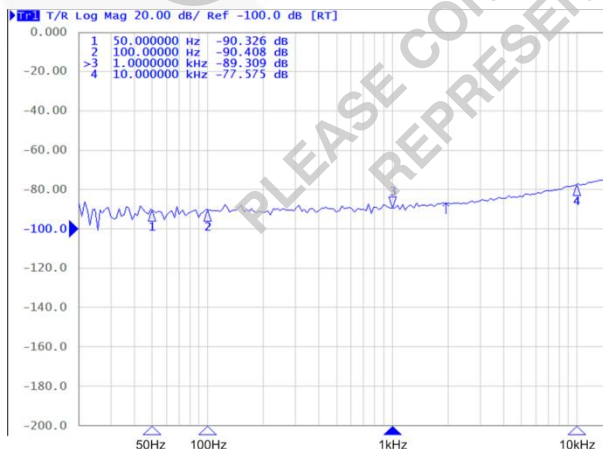


Figure 9. PSRR vs. Frequency, 10 mA Load

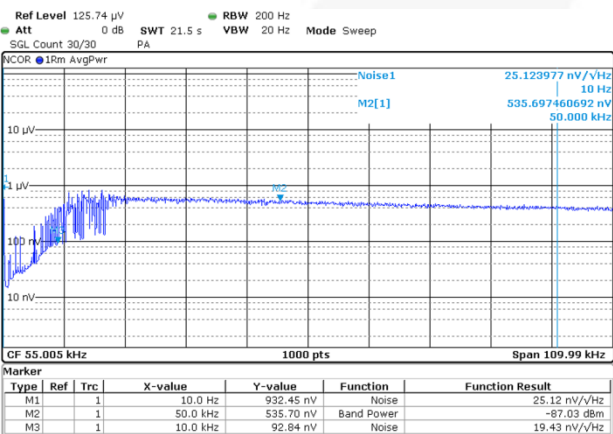


Figure 10. Output Noise Voltage vs. Frequency, 10 mA Load

Typical Characteristics

Unless otherwise specified; $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $T_A = +25^\circ\text{C}$, and test circuit per Figure 1.

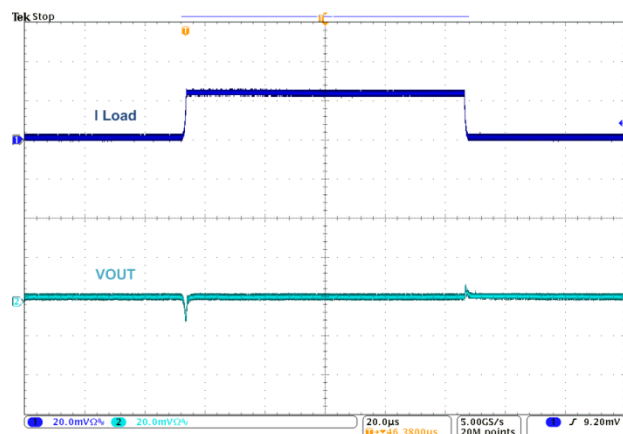


Figure 11. Load Transient, $I_{OUT} = 10 \rightarrow 250 \rightarrow 10\text{ mA}$, $V_{IN}=3.6\text{ V}$, 400 ns Edge

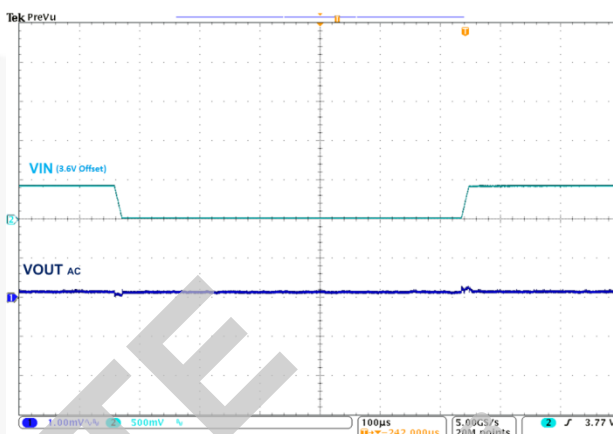


Figure 12. Line Transient, $V_{IN} = 4.0 \rightarrow 3.6 \rightarrow 4.0\text{ V}$, 10 μs Transitions, 10 mA Load



Figure 13. Line Transient, $V_{IN} = 4.0 \rightarrow 3.6 \rightarrow 4.0\text{ V}$, 10 μs Transitions, 250 mA Load

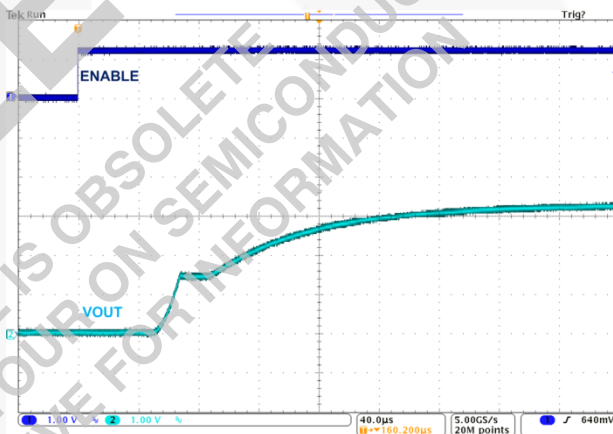


Figure 14. Startup, 10 mA Load

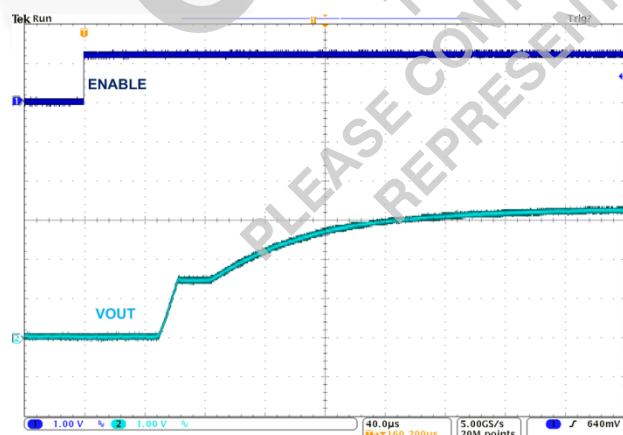


Figure 15. Startup, 250 mA Load

Circuit Description

The FAN25800 is a linear low-dropout (LDO) regulator that has high PSRR and low output noise. The enable control pin can be used to shut down the device and disconnect the output load from the input. During shutdown, the supply current drops below 1 μ A. The LDO is designed to be stable with space-saving ceramic capacitors as small as 0201 case size.

Enable and Soft-Start

When EN is LOW, all circuits are off and the IC draws <550 nA of current. The EN pin does not have an internal pull-down resistor and must not be left floating. When EN is HIGH and V_{IN} is above the UVLO threshold, the regulator begins a soft-start cycle for the output. The soft-start cycle controls inrush current, limiting it to the I_{LIM} peak current limit.

Short-Circuit and Thermal Protection

The output current is short-circuit protected. When an output fault occurs, the output current is automatically limited to I_{LIM} and V_{OUT} drops. The resultant V_{OUT} is equal to I_{LIM} multiplied by the fault impedance.

Short-circuit fault or output overload may cause the die temperature to increase and exceed the maximum rating due to power dissipation. In such cases (depending upon the ambient temperature; the V_{IN} , load current, and thermal resistance (θ_{JA}) of the mounted die), the device may enter thermal shutdown.

If the die temperature exceeds the thermal shutdown temperature threshold, the onboard thermal protection disables the output until the temperature drops below its hysteresis value. At that point, the output is re-enabled and a new soft-start sequence occurs.

Thermal Considerations

For best performance, the die temperature and the power dissipated should be kept at moderate values. The maximum power dissipated can be evaluated based on the following relationship:

$$P_{D(max)} = \left\{ \frac{T_{J(max)} - T_A}{\theta_{JA}} \right\} \quad (1)$$

where $T_{J(max)}$ is the maximum allowable junction temperature of the die; T_A is the ambient operating temperature; and θ_{JA} is dependent on the surrounding PCB layout and can be improved by providing a heat sink or surrounding copper ground.

The addition of backside copper with through-holes, stiffeners, and other enhancements can help reduce θ_{JA} . The heat contributed by the dissipation of devices nearby must be included in design considerations.

Capacitor Selection

An output capacitor with an effective capacitance between 400 nF and 15 μ F is required for loop stability. The ESR value should be within 3 to 100 m Ω . DC bias

characteristics of the capacitors must be considered when selecting the voltage rating and the case size of the capacitor. Figure 16 is a typical derating curve for a 0201 case size, 1.5 μ F, 6.3 V, X5R capacitor.

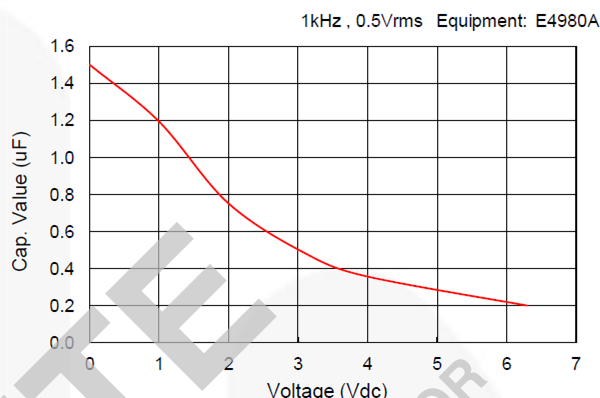


Figure 16. Capacitor DC Bias Characteristics

Typical Application for Post Regulation

Due to its high PSRR and low output noise, the FAN25800 can be used as a post-DC-DC regulator to reduce output ripple and output noise at high efficiency for noise-sensitive applications. Figure 17 shows a post-DC-DC regulation of the LDO with a buck converter. The capacitor on the output of the buck converter can be shared by the LDO as its input capacitor.

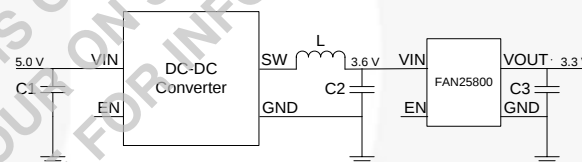


Figure 17. LDO as Post DC-DC Regulator

PCB Layout Recommendations

Capacitors should be placed as close to the IC as possible. All power and ground pins should be routed to their capacitors using top copper. The copper area connecting to the IC should be maximized to improve thermal performance.

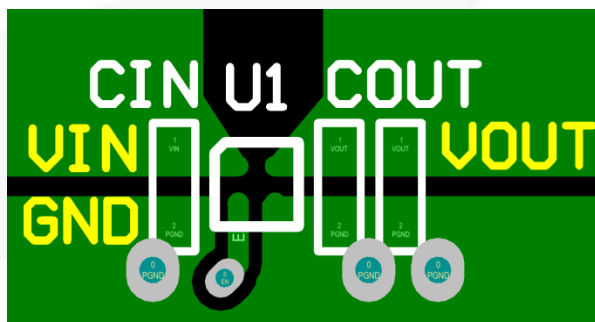


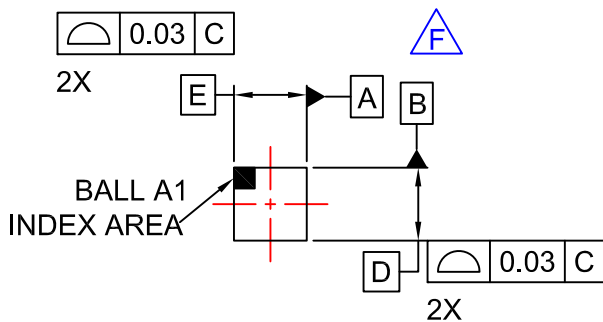
Figure 18. Recommended Layout

Product-Specific Dimensions

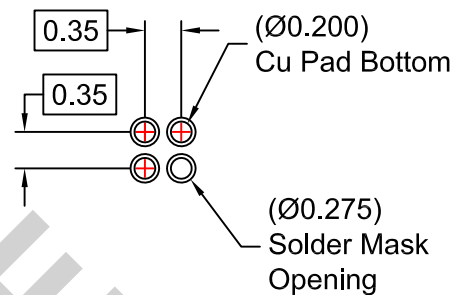
D	E	X	Y
0.65 ±0.025 mm	0.65 ±0.025 mm	0.15 mm	0.15 mm

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THIS DEVICE IS OBSOLETE
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REPRESENTATIVE FOR INFORMATION

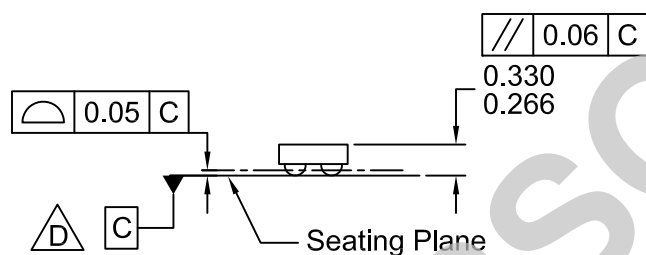




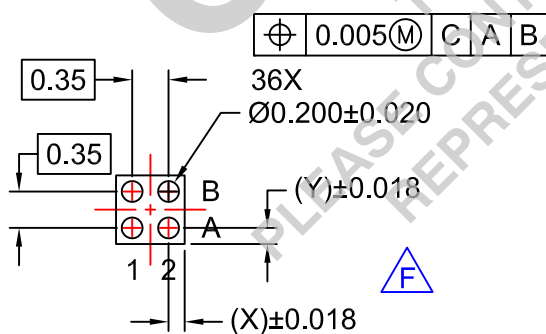
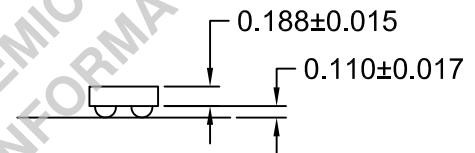
TOP VIEW



RECOMMENDED LAND PATTERN
(NSMD TYPE)



SIDE VIEWS



BOTTOM VIEW

NOTES

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 2009.

 D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 298 ± 32 MICRONS (266-330 MICRONS).

 F. FOR DIMENSIONS D,E,X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC004AK REV1

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