

January 1998 - Revised October 2003

High-Speed CMOS Logic 4x4 Register File

Features

- Simultaneous and Independent Read and Write Operations
- Expandable to 512 Words of n-Bits
- Three-State Outputs
- Organized as 4 Words x 4 Bits Wide
- Buffered Inputs
- Typical Read Time = 16ns for 'HC670 $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^\circ C$
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . $-55^\circ C$ to $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

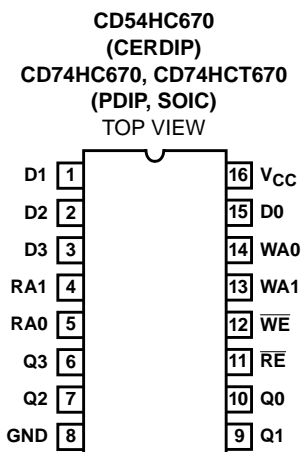
The 'HC670 and CD74HCT670 are 16-bit register files organized as 4 words x 4 bits each. Read and write address and enable inputs allow simultaneous writing into one location while reading another. Four data inputs are provided to store the 4-bit word. The write address inputs (WA0 and WA1) determine the location of the stored word in the register. When write enable (\overline{WE}) is low the word is entered into the address location and it remains transparent to the data. The outputs will reflect the true form of the input data. When (\overline{WE}) is high data and address inputs are inhibited. Data acquisition from the four registers is made possible by the read address inputs (RA1 and RA0). The addressed word appears at the output when the read enable (\overline{RE}) is low. The output is in the high impedance state when the (\overline{RE}) is high. Outputs can be tied together to increase the word capacity to 512 x 4 bits.

Ordering Information

| PART NUMBER | TEMP. RANGE ($^\circ C$) | PACKAGE |
|---------------|-------------------------------|--------------|
| CD54HC670F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC670E | -55 to 125 | 16 Ld PDIP |
| CD74HC670M | -55 to 125 | 16 Ld SOIC |
| CD74HC670MT | -55 to 125 | 16 Ld SOIC |
| CD74HC670M96 | -55 to 125 | 16 Ld SOIC |
| CD74HCT670E | -55 to 125 | 16 Ld PDIP |
| CD74HCT670M | -55 to 125 | 16 Ld SOIC |
| CD74HCT670MT | -55 to 125 | 16 Ld SOIC |
| CD74HCT670M96 | -55 to 125 | 16 Ld SOIC |

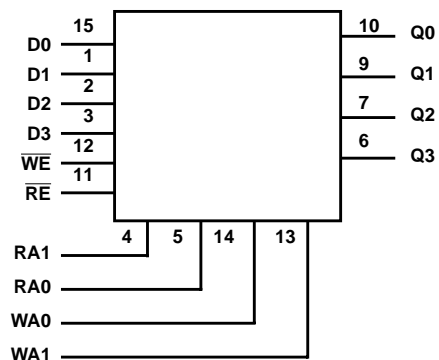
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout



CD54HC670, CD74HC670, CD74HCT670

Functional Diagram



WRITE MODE SELECT TABLE

| OPERATING MODE | INPUTS | | INTERNAL LATCHES (NOTE 1) |
|----------------|-----------------|-------|---------------------------|
| | \overline{WE} | D_N | |
| Write Data | L | L | L |
| | L | H | H |
| Data Latched | H | X | No Change |

NOTE:

1. The Write Address (WA0 and WA1) to the "internal latches" must be stable while \overline{WE} is LOW for conventional operation.

READ MODE SELECT TABLE

| OPERATING MODE | INPUTS | | OUTPUT Q_N |
|----------------|-----------------|---------------------------|--------------|
| | \overline{RE} | INTERNAL LATCHES (NOTE 2) | |
| Read | L | L | L |
| | L | H | H |
| Disabled | H | X | (Z) |

NOTE:

2. The selection of the "internal latches" by Read Address (RA0 and RA1) are not constrained by \overline{WE} or \overline{RE} operation.
H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance "Off" State

CD54HC670, CD74HC670, CD74HCT670

Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 7V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Drain Current, per Output, I_O | |
| For $-0.5V < V_O < V_{CC} + 0.5V$ | $\pm 35mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC V_{CC} or Ground Current, I_{CC} | $\pm 50mA$ |

Thermal Information

| | |
|--|--|
| Thermal Resistance (Typical, Note 3) | θ_{JA} ($^{\circ}C/W$) |
| E (PDIP) Package | 67 |
| M (SOIC) Package | 73 |
| Maximum Junction Temperature | 150 $^{\circ}C$ |
| Maximum Storage Temperature Range | -65 $^{\circ}C$ to 150 $^{\circ}C$ |
| Maximum Lead Temperature (Soldering 10s) | 300 $^{\circ}C$ (SOIC - Lead Tips Only) |

Operating Conditions

| | |
|---|------------------------------------|
| Temperature Range, T_A | -55 $^{\circ}C$ to 125 $^{\circ}C$ |
| Supply Voltage Range, V_{CC} | |
| HC Types | .2V to 6V |
| HCT Types | .4.5V to 5.5V |
| DC Input or Output Voltage, V_I , V_O | 0V to V_{CC} |
| Input Rise and Fall Time | |
| 2V | 1000ns (Max) |
| 4.5V | 500ns (Max) |
| 6V | 400ns (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS | | |
|---|-----------------|------------------------------------|---------------------|------------------------|------|-----|------|---------------|------|----------------|------|-------|----|----|
| | | V _I (V) | I _O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | | | |
| HC TYPES | | | | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V | | |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V | | |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V | | |
| Low Level Input Voltage | V _{IL} | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V | | |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V | | |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V | | |
| High Level Output Voltage CMOS Loads | V _{OH} | V _{IH} or V _{IL} | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V | | |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V | | |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V | | |
| - | | | - | - | - | - | - | - | - | - | V | | | |
| -6 | | | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V | | | |
| -7.8 | | | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V | | | |
| High Level Output Voltage TTL Loads | V _{OL} | V _{IH} or V _{IL} | - | - | - | - | - | - | - | - | - | V | | |
| | | | -6 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V | | |
| | | | -7.8 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V | | |
| 0.02 | | | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V | | | |
| 0.02 | | | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V | | | |
| 0.02 | | | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V | | | |
| Low Level Output Voltage CMOS Loads | V _{OL} | V _{IH} or V _{IL} | - | - | - | - | - | - | - | - | - | V | | |
| | | | 6 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V | | |
| | | | 7.8 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V | | |
| Input Leakage Current | | | I _I | V _{CC} or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | μA |

CD54HC670, CD74HC670, CD74HCT670

DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|------------------------------|------------------------------------|---|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
| | | V _I (V) | I _O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | μA |
| Three- State Leakage Current | | V _{IL} or V _{IH} | V _O = V _{CC} or GND | 6 | - | - | ±0.5 | - | ±5.0 | - | ±10 | μA |
| HCT TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | V _{OH} | V _{IH} or V _{IL} | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -6 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | V _{OL} | V _{IH} or V _{IL} | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 6 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I _I | V _{CC} and GND | 0 | 5.5 | - | | ±0.1 | - | ±1 | - | ±1 | μA |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | μA |
| Three- State Leakage Current | | V _{IL} or V _{IH} | V _O = V _{CC} or GND | 5.5 | - | - | ±0.5 | - | ±5.0 | - | ±10 | μA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI _{CC} (Note 4) | V _{CC} -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | μA |

NOTE:

- For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

| INPUT | UNIT LOADS |
|-----------------|------------|
| \overline{WE} | 0.3 |
| WA0 | 0.2 |
| WA1 | 0.4 |
| \overline{RE} | 1.5 |
| DATA | 0.15 |
| RA0 | 0.4 |
| RA1 | 0.7 |

NOTE: Unit Load is ΔI_{CC} limit specific in DC Electrical Specifications Table, e.g., 360μA max. at 25°C.

CD54HC670, CD74HC670, CD74HCT670

Prerequisite for Switching Specifications

| PARAMETER | SYMBOL | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | | -55°C TO 125°C | | | UNITS |
|---|---------------|---------------------|------|-----|-----|---------------|-----|-----|----------------|-----|-----|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| HC TYPES | | | | | | | | | | | | |
| Setup Time Data to \overline{WE} Write to \overline{WE} | t_{SU}, t_h | 2 | 60 | - | - | 75 | - | - | 90 | - | - | ns |
| | | 4.5 | 12 | - | - | 15 | - | - | 18 | - | - | ns |
| | | 6 | 10 | - | - | 13 | - | - | 15 | - | - | ns |
| Hold Time Data to \overline{WE} Write to \overline{WE} | t_H, t_W | 2 | 5 | - | - | 5 | - | - | 5 | - | - | ns |
| | | 4.5 | 5 | - | - | 5 | - | - | 5 | - | - | ns |
| | | 6 | 5 | - | - | 5 | - | - | 5 | - | - | ns |
| Pulse Width \overline{WE} | t_W | 2 | 80 | - | - | 100 | - | - | 120 | - | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | - | 24 | - | - | ns |
| | | 6 | 14 | - | - | 17 | - | - | 20 | - | - | ns |
| Latch Time \overline{WE} to RA0, RA1 | t_{LATCH} | 2 | 100 | - | - | 125 | - | - | 150 | - | - | ns |
| | | 4.5 | 20 | - | - | 25 | - | - | 30 | - | - | ns |
| | | 6 | 17 | - | - | 21 | - | - | 26 | - | - | ns |
| HCT TYPES | | | | | | | | | | | | |
| Setup Time Data to \overline{WE} | t_{SU}, t_h | 4.5 | 12 | - | - | 15 | - | - | 18 | - | - | ns |
| Hold Time Data to \overline{WE} Write to \overline{WE} | t_H, t_W | 4.5 | 5 | - | - | 5 | - | - | 5 | - | - | ns |
| Setup Time Write to \overline{WE} | t_{SU} | 4.5 | 18 | - | - | 23 | - | - | 27 | - | - | ns |
| Pulse Width \overline{WE} | t_W | 4.5 | 20 | - | - | 25 | - | - | 30 | - | - | ns |
| Latch Time \overline{WE} to RA0, RA1 | t_{LATCH} | 4.5 | 25 | - | - | 31 | - | - | 38 | - | - | ns |

Switching Specifications $C_L = 50\text{pF}$, Input $t_r, t_f = 6\text{ns}$

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---------------------------------------|-------------------------------------|-----------------------|---------------------|------|-----|-----|------------------|-----|-------------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | |
| Propagation Delay Reading Any Word | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 195 | - | 245 | - | 295 | ns |
| | | | 4.5 | - | - | 39 | - | 49 | - | 59 | ns |
| | | C _L = 15pF | 5 | - | 16 | - | - | - | - | - | ns |
| | | C _L = 50pF | 6 | - | - | 33 | - | 42 | - | 50 | ns |
| Write Enable to Output | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 250 | - | 315 | - | 375 | ns |
| | | | 4.5 | - | - | 50 | - | 63 | - | 75 | ns |
| | | C _L = 15pF | 5 | - | 21 | - | - | - | - | - | ns |
| | | C _L = 50pF | 6 | - | - | 43 | - | 54 | - | 64 | ns |

CD54HC670, CD74HC670, CD74HCT670

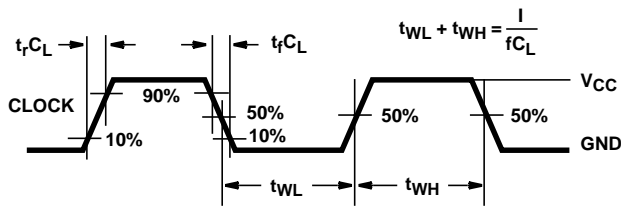
Switching Specifications $C_L = 50\text{pF}$, Input t_r , $t_f = 6\text{ns}$ (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | V_{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|-----------------------|---------------------|--------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Data to Output | t_{PLH} , t_{PHL} | $C_L = 50\text{pF}$ | 2 | - | - | 256 | - | 315 | - | 375 | ns |
| | | | 4.5 | - | - | 50 | - | 63 | - | 75 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 21 | - | - | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | - | 43 | - | 54 | - | 64 | ns |
| Output Disable Time | t_{PLZ} , t_{PHZ} | $C_L = 50\text{pF}$ | 2 | - | - | 150 | - | 190 | - | 225 | ns |
| | | | 4.5 | - | - | 30 | - | 38 | - | 45 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 12 | - | - | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | - | 26 | - | 33 | - | 38 | ns |
| Output Enable Time | t_{PZL} , t_{PZH} | $C_L = 50\text{pF}$ | 2 | - | - | 150 | - | 190 | - | 225 | ns |
| | | | 4.5 | - | - | 30 | - | 38 | - | 45 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 12 | - | - | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | - | 26 | - | 33 | - | 38 | ns |
| Output Transition Time | t_{THL} , t_{TLH} | $C_L = 50\text{pF}$ | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 10 | - | 19 | ns |
| Input Capacitance | C_I | $C_L = 50\text{pF}$ | - | 10 | - | 10 | - | 10 | - | 10 | pF |
| Three-State Output Capacitance | C_O | - | - | 20 | - | 20 | - | 20 | - | 20 | pF |
| Power Dissipation Capacitance (Notes 5, 6) | C_{PD} | $C_L = 15\text{pF}$ | 5 | - | 59 | - | - | - | - | - | pF |
| HCT TYPES | | | | | | | | | | | |
| Propagation Delay Reading Any Word | t_{PHL} , t_{PLH} | $C_L = 50\text{pF}$ | 4.5 | - | - | 40 | - | 50 | - | 53 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 17 | - | - | - | - | - | ns |
| Write Enable to Output | t_{PHL} , t_{PLH} | $C_L = 50\text{pF}$ | 4.5 | - | - | 50 | - | 63 | - | 75 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 21 | - | - | - | - | - | ns |
| Data to Output | t_{PHL} , t_{PLH} | $C_L = 50\text{pF}$ | 4.5 | - | - | 50 | - | 63 | - | 75 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 21 | - | - | - | - | - | ns |
| Output Disable Time | t_{PLZ} , t_{PHZ} | $C_L = 50\text{pF}$ | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 14 | - | - | - | - | - | ns |
| Output Enable Time | t_{PZL} , t_{PZH} | $C_L = 50\text{pF}$ | 4.5 | - | - | 38 | - | 48 | - | 57 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 16 | - | - | - | - | - | ns |
| Output Transition Time | t_{THL} , t_{TLH} | $C_L = 50\text{pF}$ | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| Input Capacitance | C_I | $C_L = 50\text{pF}$ | - | 10 | - | 10 | - | 10 | - | 10 | pF |
| Three-State Output Capacitance | C_O | - | - | 20 | - | 20 | - | 20 | - | 20 | pF |
| Power Dissipation Capacitance (Notes 5, 6) | C_{PD} | $C_L = 15\text{pF}$ | 5 | - | 66 | - | - | - | - | - | pF |

NOTES:

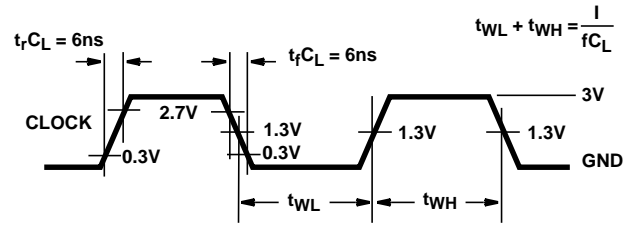
- C_{PD} is used to determine the dynamic power consumption, per output.
- $P_D = C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_O$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

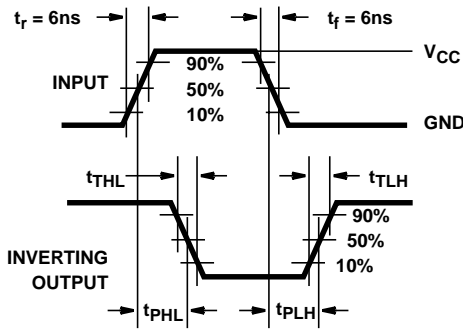


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

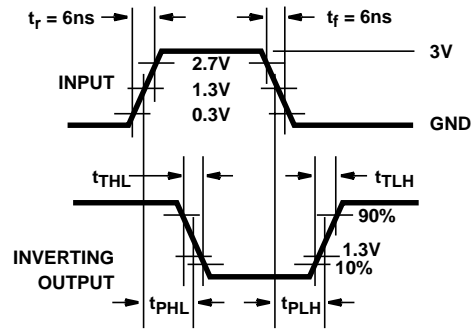


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

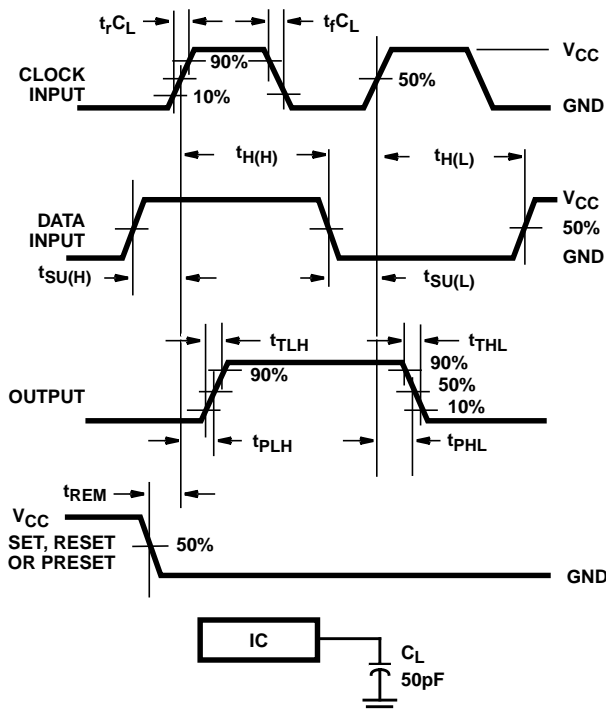


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

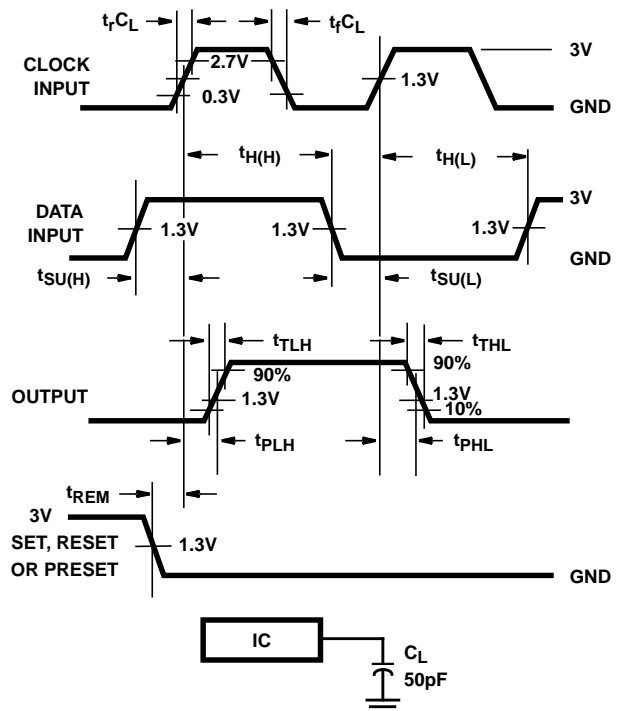


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Test Circuits and Waveforms (Continued)

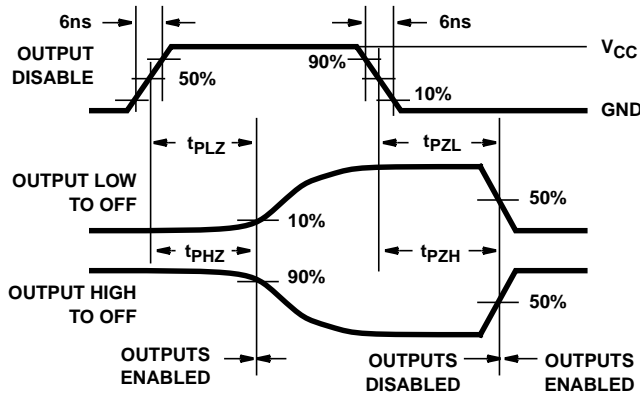


FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

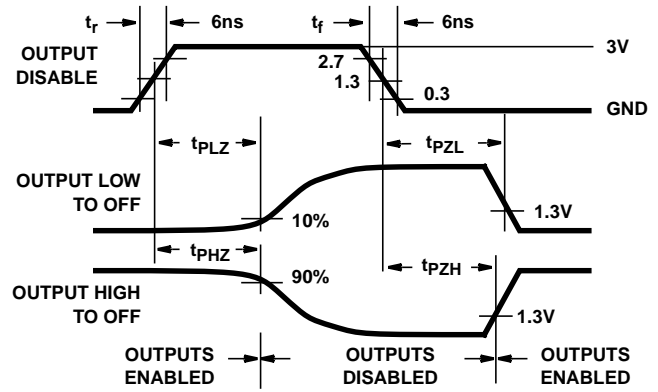
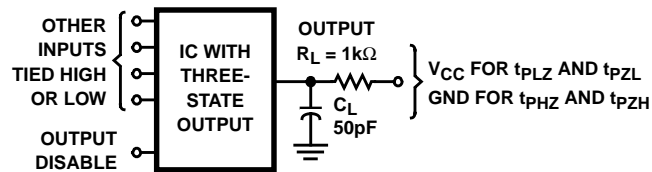


FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CD74HC670E | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC670E |
| CD74HC670E.A | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC670E |
| CD74HC670M | Obsolete | Production | SOIC (D) 16 | - | - | Call TI | Call TI | -55 to 125 | HC670M |
| CD74HC670M96 | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC670M |
| CD74HC670M96.A | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC670M |
| CD74HCT670E | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT670E |
| CD74HCT670E.A | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT670E |
| CD74HCT670M | Active | Production | SOIC (D) 16 | 40 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT670M |
| CD74HCT670M.A | Active | Production | SOIC (D) 16 | 40 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT670M |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC670M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC670M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74HC670E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC670E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC670E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC670E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT670E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT670E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT670E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT670E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT670M | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| CD74HCT670M.A | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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