

FOD0708 Single Channel CMOS Optocoupler

FOD0738 Dual Channel CMOS Optocoupler

Features

- +5 V CMOS compatibility
- 15 ns typical pulse width distortion
- 30 ns max. pulse width distortion
- 40 ns max. propagation delay skew
- High speed: 15 MBd
- 60 ns max. propagation delay
- 10 kV/μs minimum common mode rejection
- -40°C to 100°C temperature range
- UL approved (file #E90700)

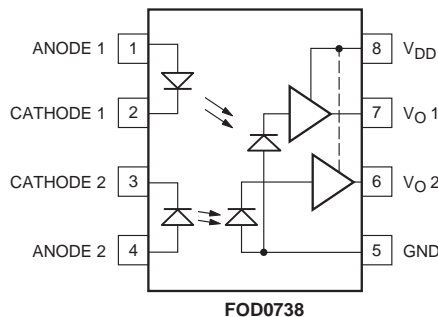
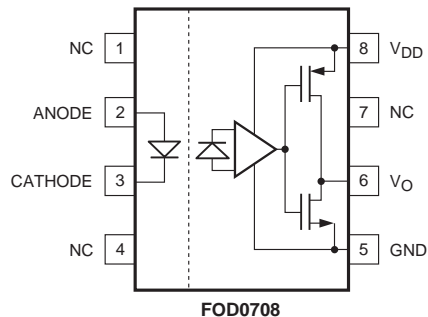
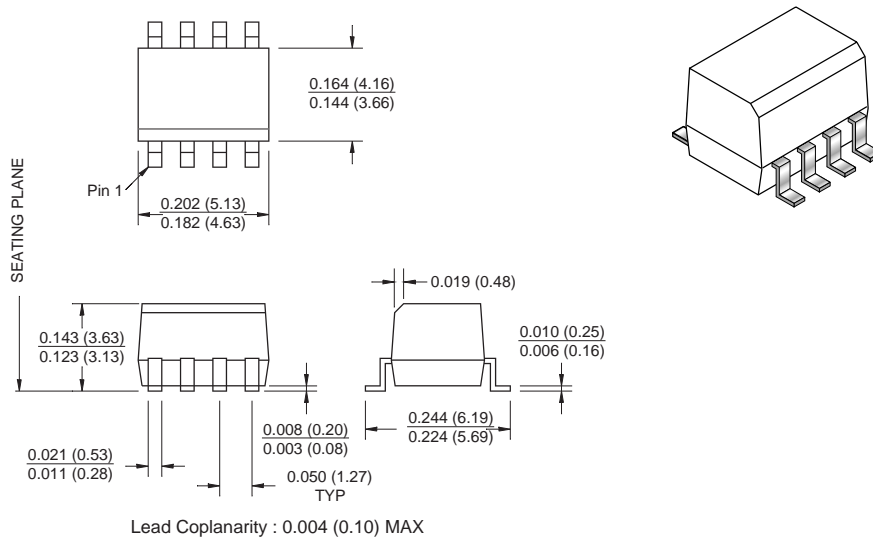
Applications

- Line receivers
- Pulse transformer replacement
- Output interface to CMOS-LSTTL-TTL
- Wide bandwidth analog coupling

General Description

The FOD0708 and FOD0738 optocouplers consist of an AlGaAs LED optically coupled to a high speed transimpedance amplifier and voltage comparator. These optocouplers utilize the latest CMOS IC technology to achieve outstanding performance with very low power consumption. The devices are housed in a compact 8-pin SOIC package for optimum mounting density.

Package Dimensions



TRUTH TABLE

LED	V _O OUTPUT
OFF	H
ON	L

Note: A 0.1μF bypass capacitor must be connected between pins 5 and 8.

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Min.	Max.	Units
T_S	Storage Temperature	-40	+125	$^\circ\text{C}$
T_A	Ambient Operating Temperature	-40	+100	$^\circ\text{C}$
V_{DD}	Supply Voltages	0	6	Volts
V_O	Output Voltage	-0.5	$V_{DD} + 0.5$	Volts
I_O	Average Output Current		2	mA
I_F	Average Forward Input Current		20	mA
	Lead Solder Temperature	260 $^\circ\text{C}$ for 10 sec., 1.6 mm below seating plane		
	Solder Reflow Temperature Profile	See Solder Reflow Temperature Profile Section		
	LED Power Dissipation Single Channel Dual Channel	40 mW (derate above 95 $^\circ\text{C}$, 1.4 mW/ $^\circ\text{C}$) 40 mW per channel (derate above 90 $^\circ\text{C}$, 1.2 mW/ $^\circ\text{C}$)		
	Detector Power Dissipation Single Channel Dual Channel	85 mW (derate above 75 $^\circ\text{C}$, 1.8 mW/ $^\circ\text{C}$) 65 mW per channel (derate above 90 $^\circ\text{C}$, 2.0 mW/ $^\circ\text{C}$)		

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
T_A	Ambient Operating Temperature	-40	+100	$^\circ\text{C}$
V_{DD}	Supply Voltages	4.5	5.5	Volts
I_F	Input Current (ON)	10	16	mA

Electrical Characteristics ($T_A = -40^\circ\text{C}$ to $+100^\circ\text{C}$) and $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
V_F	Input Forward Voltage	$I_F = 12\text{ mA}$	1.3	1.45	1.8	V	9
BV_R	Input Reverse Breakdown Voltage	$I_R = 10\ \mu\text{A}$	5			V	
V_{OH}	Logic High Output Voltage	$I_F = 0, I_O = -20\ \mu\text{A}$	4.0	5.0		V	
V_{OL}	Logic Low Output Voltage	$I_F = 12\text{ mA}, I_O = 20\ \mu\text{A}$		0.01	0.1	V	
I_{TH}	Input Threshold Current (FOD0708) (FOD0738)	$I_{OL} = 20\ \mu\text{A}$		4.0 4.4	8.2 8.2	mA	1,5
I_{DDL}	Logic Low Output Supply Current (FOD0708) (FOD0738)	$I_F = 12\text{ mA}$		3.4 6.9	14.0 18.0	mA	3,7
I_{DDH}	Logic High Output Supply Current (FOD0708) (FOD0738)	$I_F = 0$		3.7 7.5	11.0 15.0	mA	4,8

*All typicals at $T_A = 25^\circ\text{C}$ and $V_{DD} = 5\text{V}$ unless otherwise noted.

Switching Characteristics Over recommended temperature ($T_A = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$) and $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$. All typical specifications are at $T_A = 25^{\circ}\text{C}$, $V_{DD} = +5\text{ V}$.

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Units
t_{PHL}	Propagation Delay Time to Logic Low Output	$I_F = 12\text{ mA}$, $C_L = 15\text{ pF}$ CMOS Signal Levels, note 1, fig. 10	20		60	ns
t_{PLH}	Propagation Delay Time to Logic High Output	$I_F = 12\text{ mA}$, $C_L = 15\text{ pF}$ CMOS Signal Levels, note 1, fig. 10	FOD0708	13	60	ns
			FOD0738	11	60	
PW	Pulse Width		100			ns
PWD	Pulse Width Distortion	$I_F = 12\text{ mA}$, $C_L = 15\text{ pF}$ CMOS Signal Levels, note 2	0		30	ns
t_{PSK}	Propagation Delay Skew	$I_F = 12\text{ mA}$, $C_L = 15\text{ pF}$ CMOS Signal Levels, note 3			40	ns
t_R	Output Rise Time (10%–90%)	$I_F = 12\text{ mA}$, $C_L = 15\text{ pF}$ CMOS Signal Levels		12		ns
t_F	Output Fall Time (90%–10%)	$I_F = 12\text{ mA}$, $C_L = 15\text{ pF}$ CMOS Signal Levels		8		ns
CM_H	Common Mode Transient Immunity at Logic High Output	$V_{CM} = 1000\text{ V}$, $T_A = 25^{\circ}\text{C}$, $I_F = 0\text{ mA}$, note 4, fig. 11	25	50		kV/ μs
CM_L	Common Mode Transient Immunity at Logic Low Output	$V_{CM} = 1000\text{ V}$, $T_A = 25^{\circ}\text{C}$, $I_F = 12\text{ mA}$, note 5, fig. 11	25	50		kV/ μs

*All typicals at $T_A = 25^{\circ}\text{C}$ and $V_{DD} = 5\text{V}$ unless otherwise noted.

Isolation Characteristics ($T_A = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ Unless otherwise specified.)

Characteristics	Test Conditions	Symbol	Min	Typ.**	Max	Unit
Input-Output Insulation Leakage Current	(Relative humidity = 45%) ($T_A = 25^{\circ}\text{C}$, $t = 5\text{ s}$) ($V_{I-O} = 3000\text{ VDC}$) (Note 6)	I_{I-O}			1.0	μA
Withstand Insulation Test Voltage	($I_{I-O} \leq 10\text{ }\mu\text{A}$, $R_H < 50\%$, $T_A = 25^{\circ}\text{C}$) ($t = 1\text{ min.}$) (Note 6)	V_{ISO}	2500			V_{RMS}
Resistance (Input to Output)	($V_{I-O} = 500\text{ V}$) (Note 6)	R_{I-O}		10^{12}		Ω
Capacitance (Input to Output)	($f = 1\text{ MHz}$) (Note 6)	C_{I-O}		0.6		pF

** All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$

Notes:

- Propagation delay time, high to low (t_{PHL}), is measured from the 50% level on the rising edge of the input pulse to the 2.5V level of the falling edge of the output voltage signal. Propagation delay time, low to high (t_{PLH}), is measured from the 50% level on the falling edge of the input pulse to the 2.5V level of the rising edge of the output voltage signal.
- Pulse width distortion is defined as the absolute difference between the high to low and low to high propagation delay times, $|t_{PHL} - t_{PLH}|$.
- Propagation delay skew, t_{PSK} , is defined as the worst case difference in t_{PHL} or t_{PLH} between units within the recommended operating range of the device.
- CM_H – The maximum tolerated rate of rise of the common mode voltage to ensure the output will remain in the high state, (i.e., $V_{OUT} > 2.0\text{V}$) Measured in kilovolts per microsecond (kV/ μs).
- CM_L – The maximum tolerated rate of fall of the common mode voltage to ensure the output will remain in the low state, (i.e., $V_{OUT} < 0.8\text{V}$). Measured in kilovolts per microsecond (kV/ μs).
- Isolation voltage, V_{ISO} , is an internal device dielectric breakdown rating. For this test, pins 1,2,3,4 are common, and pins 5,6,7,8 are common.

Typical Characteristics

Figure 1. FOD0708
Typical Input Threshold Current vs Ambient Temperature

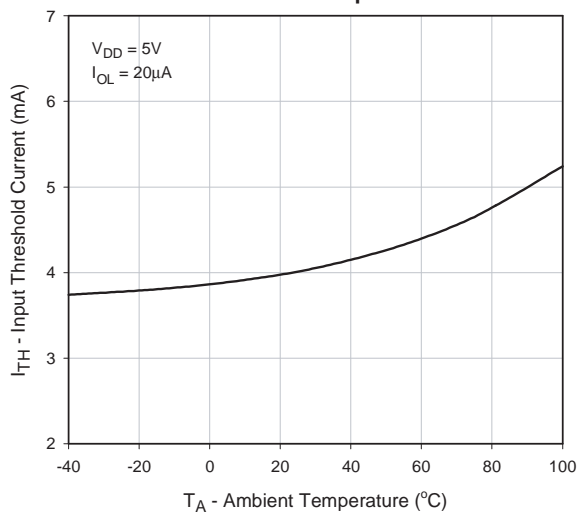


Figure 2. FOD0708
Typical Switching Speed vs Pulse Input Current

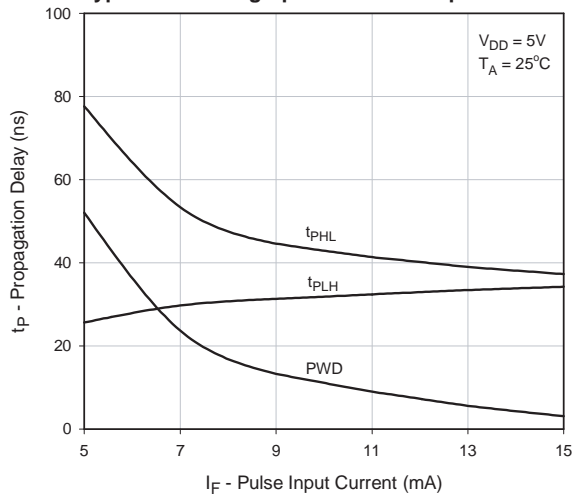


Figure 3. FOD0708
Typical Logic Low Output Supply Current vs Ambient Temperature

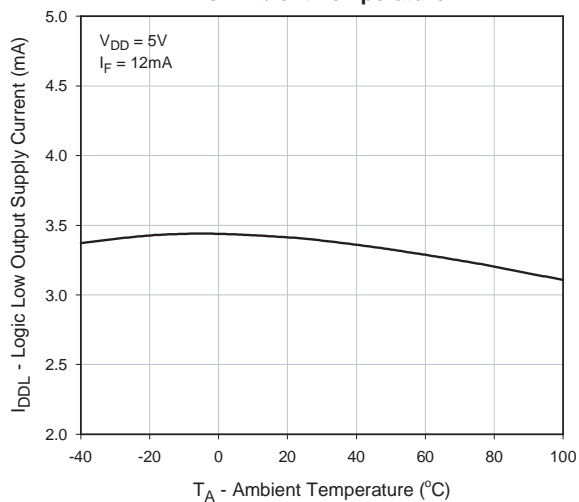
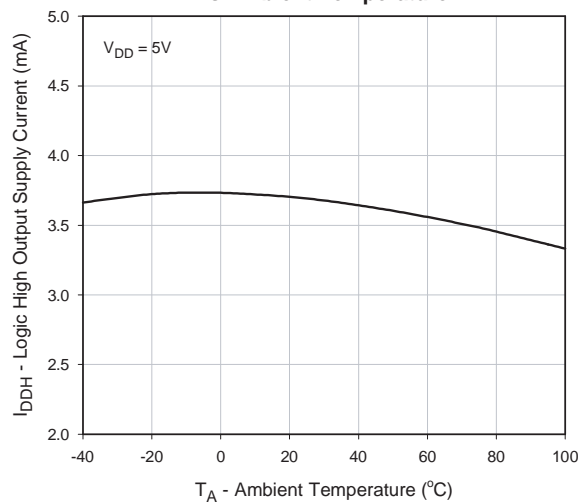
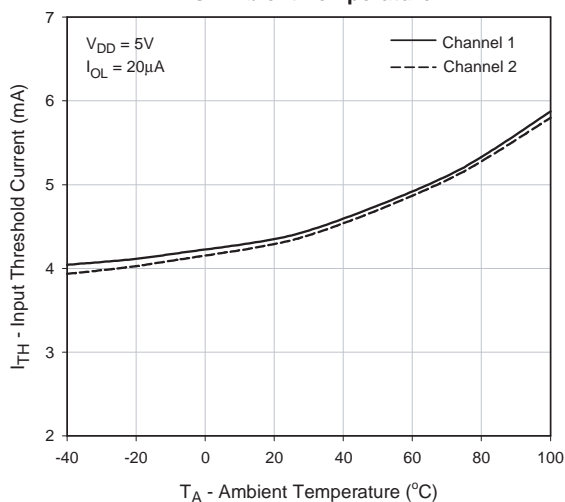


Figure 4. FOD0708
Typical Logic High Output Supply Current vs Ambient Temperature

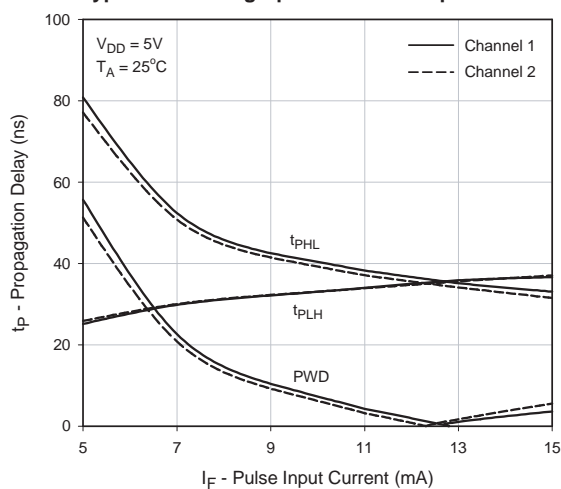


Typical Characteristics (Continued)

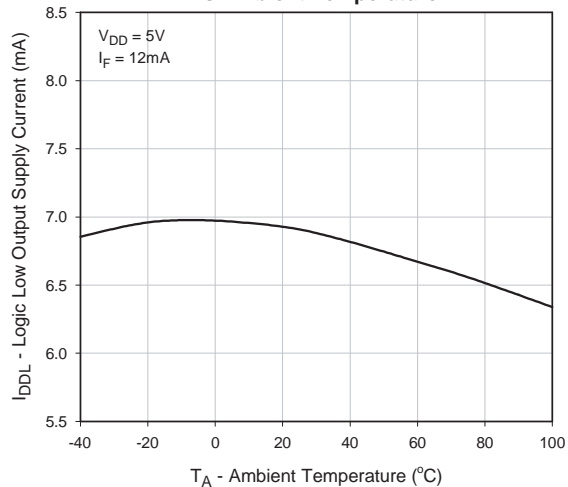
**Figure 5. FOD0738
Typical Input Threshold Current vs Ambient Temperature**



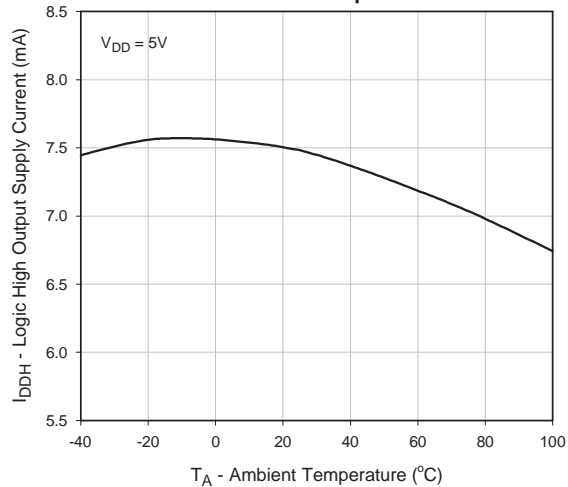
**Figure 6. FOD0738
Typical Switching Speed vs Pulse Input Current**



**Figure 7. FOD0738
Typical Logic Low Output Supply Current vs Ambient Temperature**

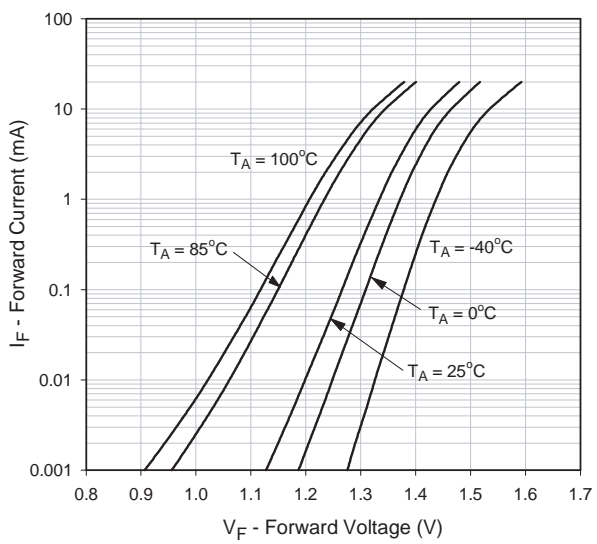


**Figure 8. FOD0738
Typical Logic High Output Supply Current vs Ambient Temperature**



Typical Characteristics (Continued)

Figure 9. Input Forward Current vs. Forward Voltage



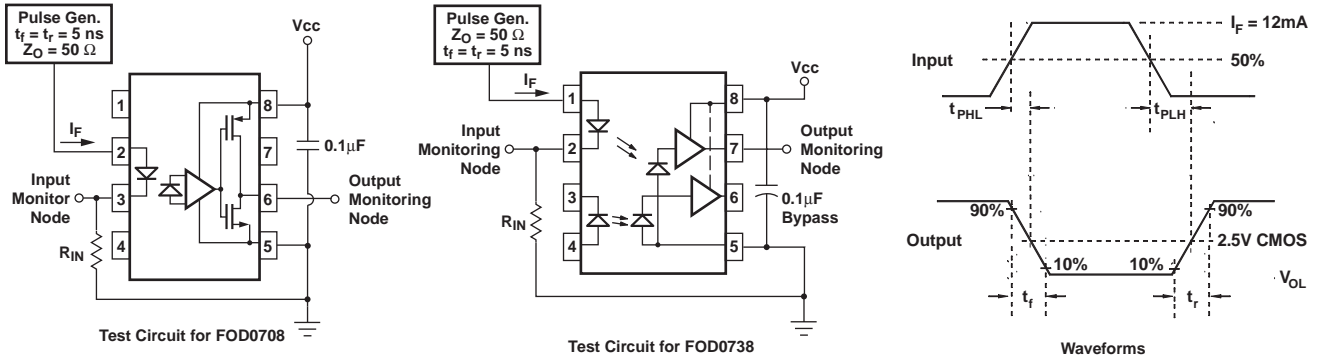


Fig. 10 Test Circuit and Waveforms for t_{PLH} , t_{PHL} , t_r and t_f .

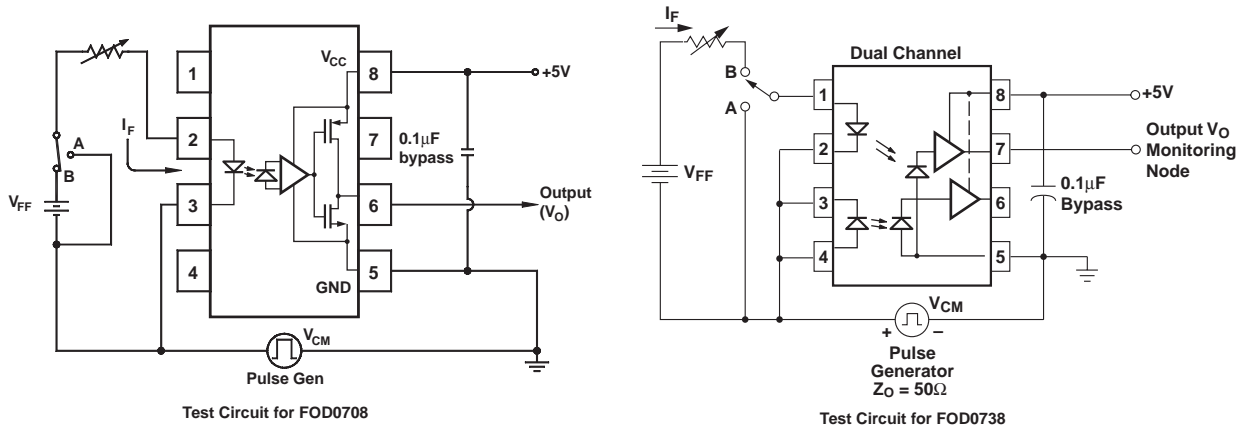
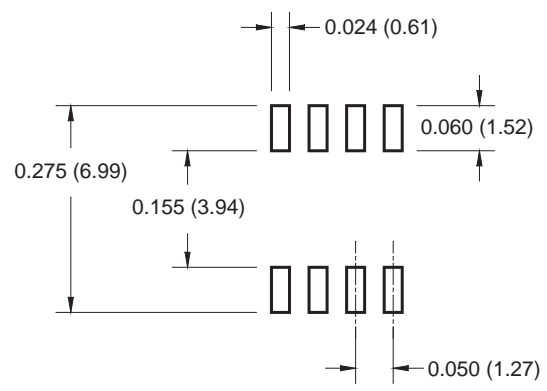


Fig. 11 Test Circuit Common Mode Transient Immunity (FOD0708 and FOD0738)

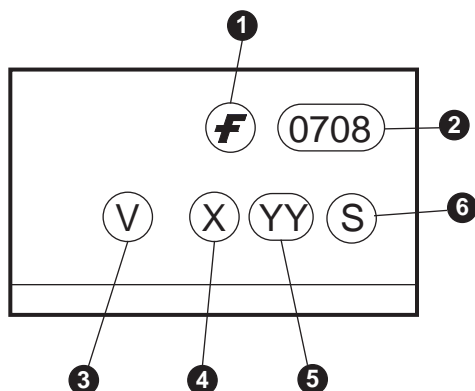
8-Pin Small Outline



Ordering Information

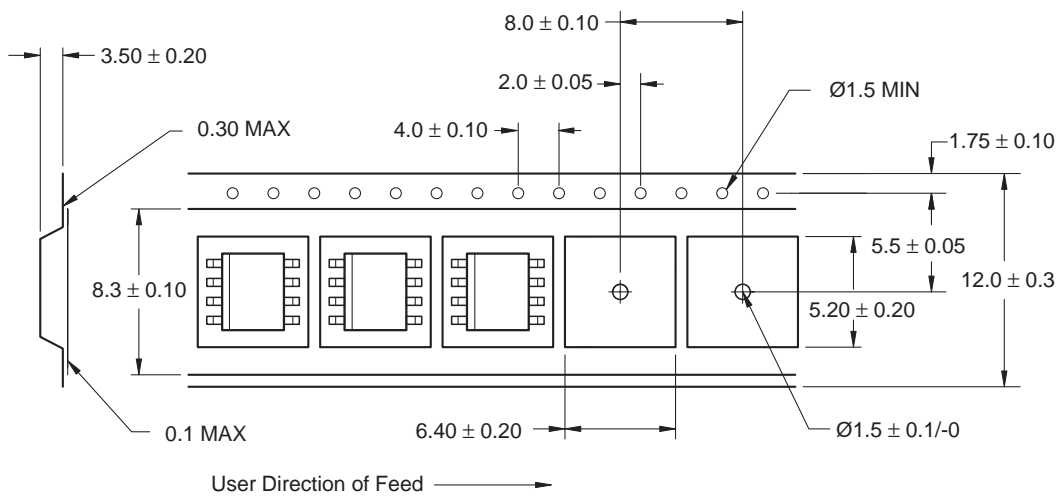
Option	Order Entry Identifier	Description
No Suffix	FOD0708	Shipped in tubes (50 units per tube)
R1	FOD0708R1	Tape and Reel (500 units per reel)
R2	FOD0708R2	Tape and Reel (2500 units per reel)

Marking Information

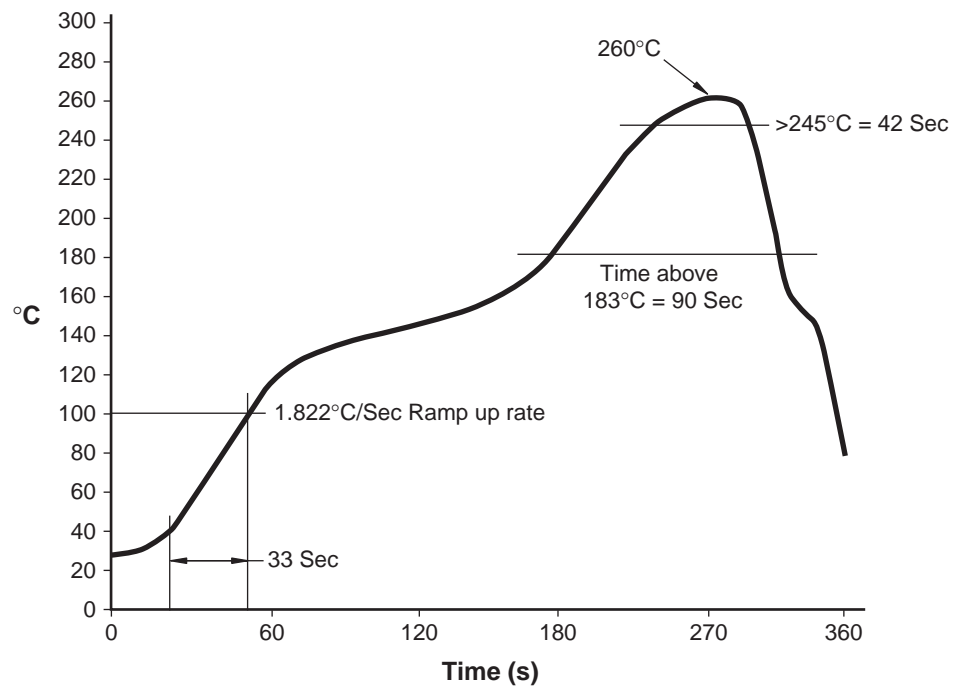


Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., '5'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

Carrier Tape Specification



Reflow Profile



TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE ^x TM	FAST [®]	ISOPLANAR TM	PowerSaver TM	SuperSOT TM -6
ActiveArray TM	FAST ^r TM	LittleFET TM	PowerTrench [®]	SuperSOT TM -8
Bottomless TM	FPS TM	MICROCOUPLER TM	QFET [®]	SyncFET TM
Build it Now TM	FRFET TM	MicroFET TM	QS TM	TCM TM
CoolFET TM	GlobalOptoisolator TM	MicroPak TM	QT Optoelectronics TM	TinyLogic [®]
CROSSVOLT TM	GTO TM	MICROWIRE TM	Quiet Series TM	TINYOPTO TM
DOME TM	HiSeC TM	MSX TM	RapidConfigure TM	TruTranslation TM
EcoSPARK TM	I ² C TM	MSXPro TM	RapidConnect TM	UHC TM
E ² CMOS TM	<i>i-Lo</i> TM	OCX TM	μSerDes TM	UltraFET [®]
EnSigna TM	ImpliedDisconnect TM	OCXPro TM	ScalarPump TM	UniFET TM
FACT TM	IntelliMAX TM	OPTOLOGIC [®]	SILENT SWITCHER [®]	VCX TM
FACT Quiet Series TM		OPTOPLANAR TM	SMART START TM	Wire TM
Across the board. Around the world. TM		PACMAN TM	SPM TM	
The Power Franchise [®]		POP TM	Stealth TM	
Programmable Active Droop TM		Power247 TM	SuperFET TM	
		PowerEdge TM	SuperSOT TM -3	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I18