

### POWER MANAGEMENT

#### Description

The SC2614 is a fully integrated DDR power solution providing power for the VDDQ and the VTT rails. The SC2614 also completely adheres to the ACPI sleep state power requirements. A synchronous buck controller provides the high current of the VDDQ at high efficiency, while a linear sink/source regulator provides the termination voltage with 2 Amp Source/Sink capability. This approach makes the best trade-off between cost and performance. Additional logic and UVLOs complete the functionality of this single chip DDR power solution in compliance with S3 and S5 motherboard signals. A **BF\_CUT output signal** prevents Back Feeding Input Rail during S3 while a **PGOOD output** signals correct voltage Rails.

The SC2614 is capable of sourcing up to 20A at the switcher output, and 2A at the VTT output. The MLP package provides excellent thermal impedance while keeping small footprint. VDDQ current limit as well as 3 independent thermal shutdown circuits assure safe operation under all fault conditions.

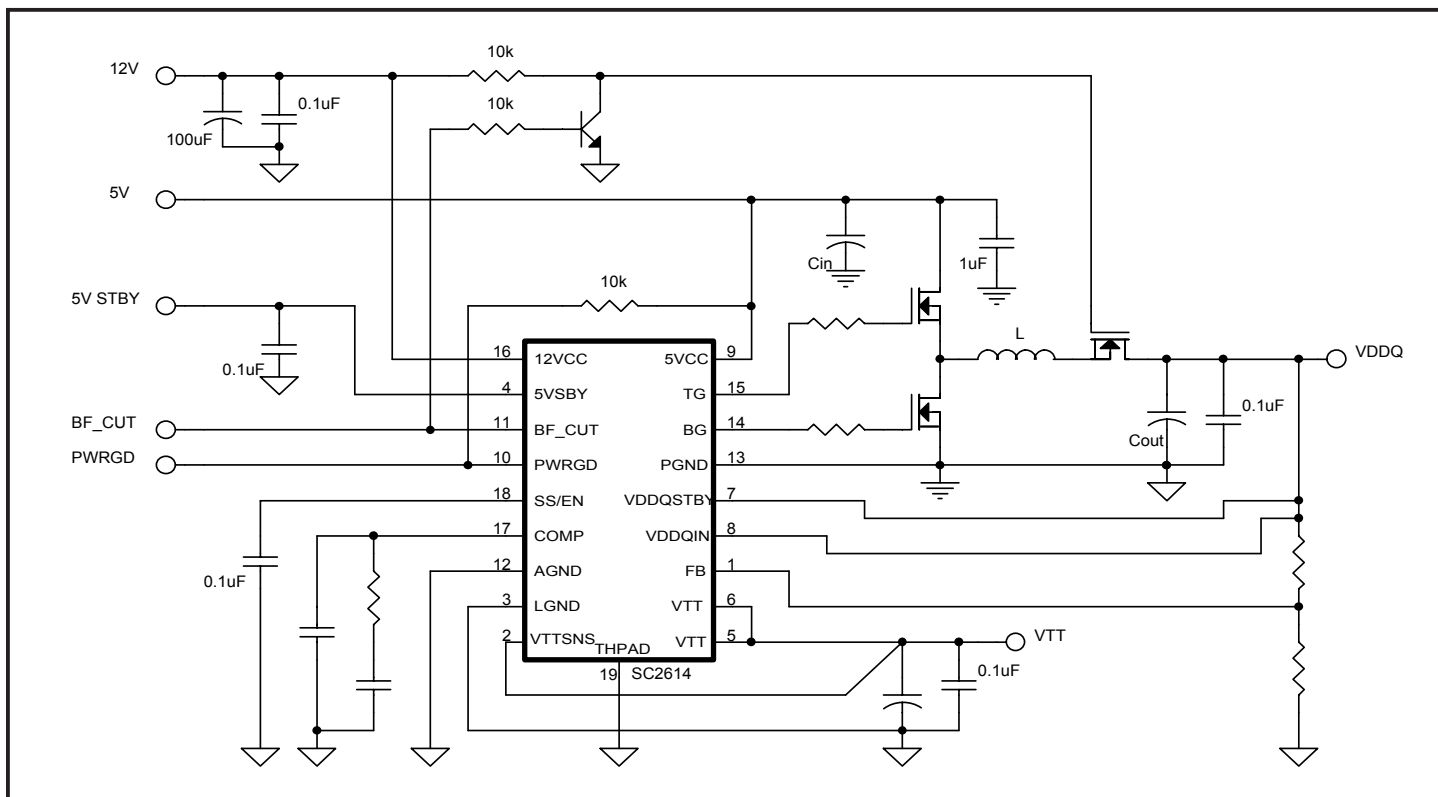
#### Features

- ◆ **Uses Latched BF\_Cut from Glue Chip to sequence the three regulators**
- ◆ High efficiency (90%) switcher for **VDDQ supplies 20 Amps**
- ◆ Single chip solution complies fully with ACPI power sequencing Specifications
- ◆ **2 Amp VTT Source/Sink Capability**
- ◆ High current gate drives
- ◆ **Internal S3 state LDO for VDDQ**
- ◆ UVLO on 5V and 12V
- ◆ Independent Thermal Shutdown for VDDQ and VTT
- ◆ Fast transient response
- ◆ 18 pin MLP package

#### Applications

- ◆ Power Solution for DDR memory per Intel<sup>®</sup> motherboard specification
- ◆ High speed data line termination

#### Typical Application Circuit



## POWER MANAGEMENT

### Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage, 5VCC to AGND	$V_{5VCC}$	7	V
Supply Voltage, 12VCC to AGND	$V_{12VCC}$	15	V
Standby Input Voltage	$V_{5VSBY}$	7	V
Inputs	I/O	5VSTBY +0.3, AGND -0.3	V
AGND to PGND or LGND		0.3	V
VTT Output Current	$I_{O(VTT)}$	+/- 2	A
Operating Ambient Temperature Range	$T_A$	0 to 70	°C
Operating Junction Temperature	$T_J$	125	°C
Thermal Resistance Junction to Ambient *	$\theta_{JA}$	25	°C/W
Thermal Resistance Junction to Case *	$\theta_{JC}$	4	°C/W
Storage Temperature Range	$T_{STG}$	-65 to 150	°C
TG/BG DC Voltage		12Vcc + 0.3, AGND -0.5	V
TG/BG AC Voltage		12Vcc + 1.0, AGND -1.0	V
ESD Rating (Human Body Model)	ESD	2	kV

\* See Mounting Considerations.

### Electrical Characteristics

Unless specified:  $T_A = 25^\circ\text{C}$ , 12VCC = 12V, 5VCC = 5V, 5VSBY = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
5V Supply Voltage	$V_{5VCC}$		4.5	5	5.5	V
12V Supply Voltage	$V_{12VCC}$		10.8	12	13.2	V
5V Standby Voltage	$V_{5VSBY}$		4.5	5	5.5	V
Quiescent Current	$I_{Q(5VSBY)}$	BF_CUT low		1.8	2.5	mA
		BF_CUT High		3.5	5.0	
BF_CUT Threshold				TTL		V
12VCC Under Voltage Lockout	$UVLO_{12VCC}$		7	8.2	10	V
5VCC Under Voltage Lockout	$UVLO_{5VCC}$		3.5	3.7	4	V
Feedback Reference	$V_{REF}$			1.25		V
Feedback Current	$I_{FB}$	$V_{FB} = 1.25V$			2	uA
SS/EN Shutdown Threshold	$V_{EN(TH)}$			0.3		V

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

Unless specified:  $T_A = 25^\circ\text{C}$ , 12VCC = 12V, 5VCC = 5V, 5VSBY = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal Shutdown	$T_{J\text{-SHDN}}$			150		$^\circ\text{C}$
Thermal Shutdown Hysteresis	$T_{J\text{-HYST}}$			10		$^\circ\text{C}$
<b>Switcher</b>						
Load Regulation		$I_{VDDQ} = 0\text{A to } 10\text{A}$		0.2		%
Oscillator Frequency	$f_{\text{OSC}}$		225	250	275	KHz
Soft Start Current	$I_{\text{SS}}$			25		$\mu\text{A}$
Duty Cycle			0		80	%
Overcurrent Trip Voltage	$V_{\text{TRIP}}$	% of VDDQ Setpoint	50	60	70	%
Top Gate Rise Time	$TG_R$	Gate capacitance = 4000pF		25		nS
Top Gate Fall Time	$TG_F$	Gate capacitance = 4000pF		25		nS
Bottom Gate Rise Time	$BG_R$	Gate capacitance = 4000pF		35		nS
Bottom Gate Fall Time	$BG_F$	Gate capacitance = 4000pF		35		nS
Dead Time	$t_d$		20	50		nS
Error Amplifier Transconductance	gm			0.8		mS
Error Amplifier Gain @ DC	$A_{\text{EA}}$	$R_{\text{COMP}} = \text{open}$		38		dB
Error Amplifier Bandwidth	$G_{\text{BW}}$			5		MHz
Error Amplifier Source/Sink Current				+/-60		$\mu\text{A}$
Modulator Gain	$A_M$	$V_{\text{IN}} = 5\text{V}$		19		dB
Power Good Low		$I_{\text{PWRGD}} = 1\text{mA, sink}$		50	400	mV
Power Good High Leakage		$V_{\text{PWRGD}} = 5\text{V}; \text{BF\_CUT} = 0$		0.1	2	$\mu\text{A}$
<b>STBY LDO</b>						
Output Current	$I_{VDDQ\text{STBY}}$		750			mA
Load Regulation	$\Delta V/\Delta I$	$I_{VDDQ} = 0\text{A to } 650\text{mA}$		0.5		%
Current Limit	$I_{\text{LIM}}$	BF_CUT = high, VTT floating		1		A
<b>VTT LDO</b>						
Output Voltage	VTT	$V_{VDDQ} = 2.500\text{V}$	1.235	1.250	1.265	V
Source and Sink Currents	$I_{\text{VTT}}$		+/-1.8			A
Load Regulation	$\Delta V_{\text{TTC}}/\Delta I$	$I_{\text{VTT}} = +1.8\text{A to } -1.8\text{A}$			+/- 1	%
Error Amplifier Gain	$A_{\text{EA\_VTT}}$			75		dB
Current Limit	$V_{\text{TTC\_ILIM}}$	BF_CUT = low		3		A

## POWER MANAGEMENT

### Pin Configuration

#### TOP VIEW

FB	1	18	SS/EN
VTTSENS	2	17	COMP
LGND	3	16	12VCC
5VSBY	4	15	TG
VTT	5	14	BG
VTT	6	13	PGND
VDDQSTBY	7	12	AGND
VDDQIN	8	11	BF_CUT
5VCC	9	10	PWRGD

(18 Pin MLP)

Note: Pin19 is the thermal Pad on the bottom of the device

### Ordering Information

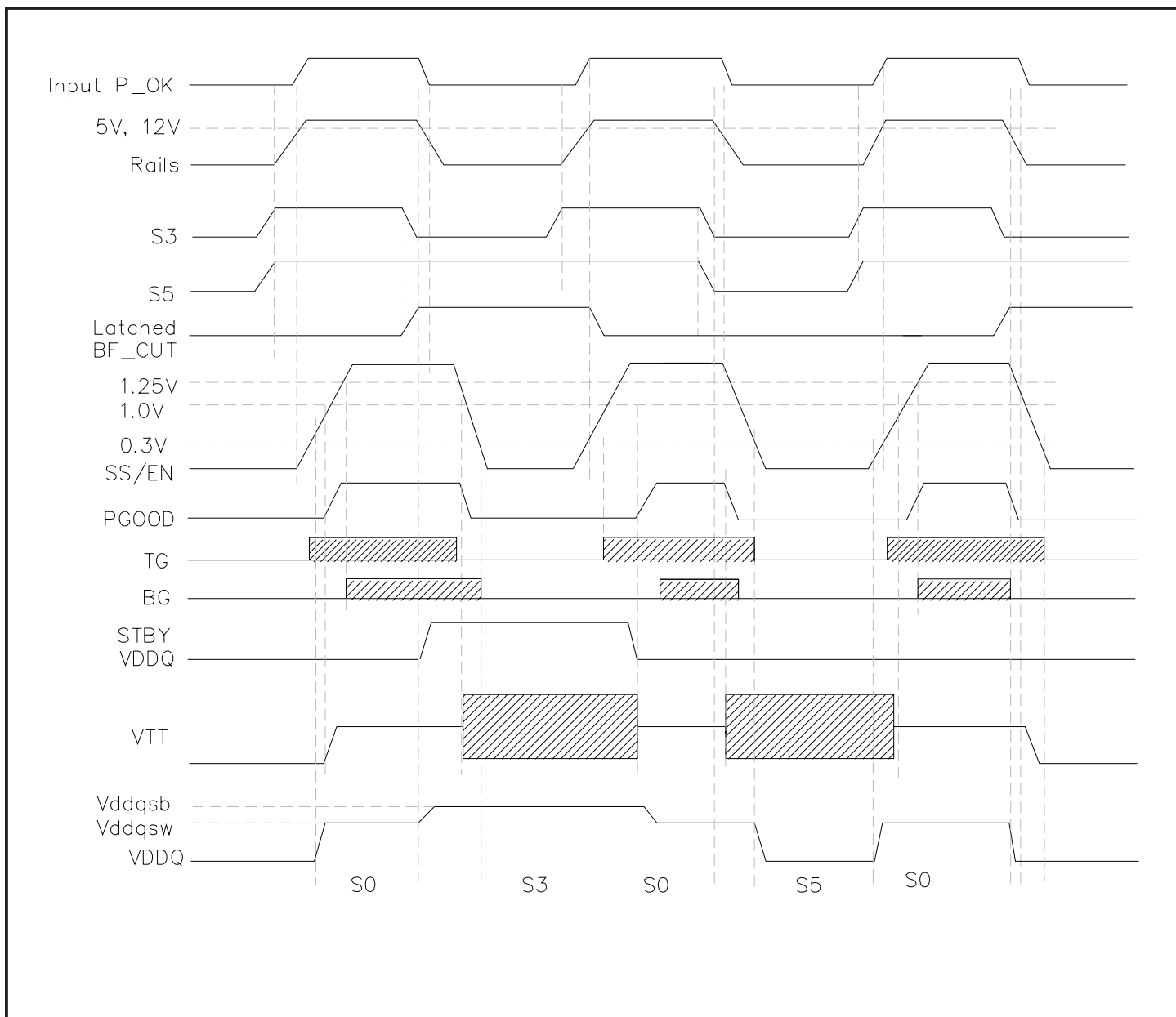
Part Numbers	Package
SC2614MLTR <sup>(1)</sup>	MLP-18

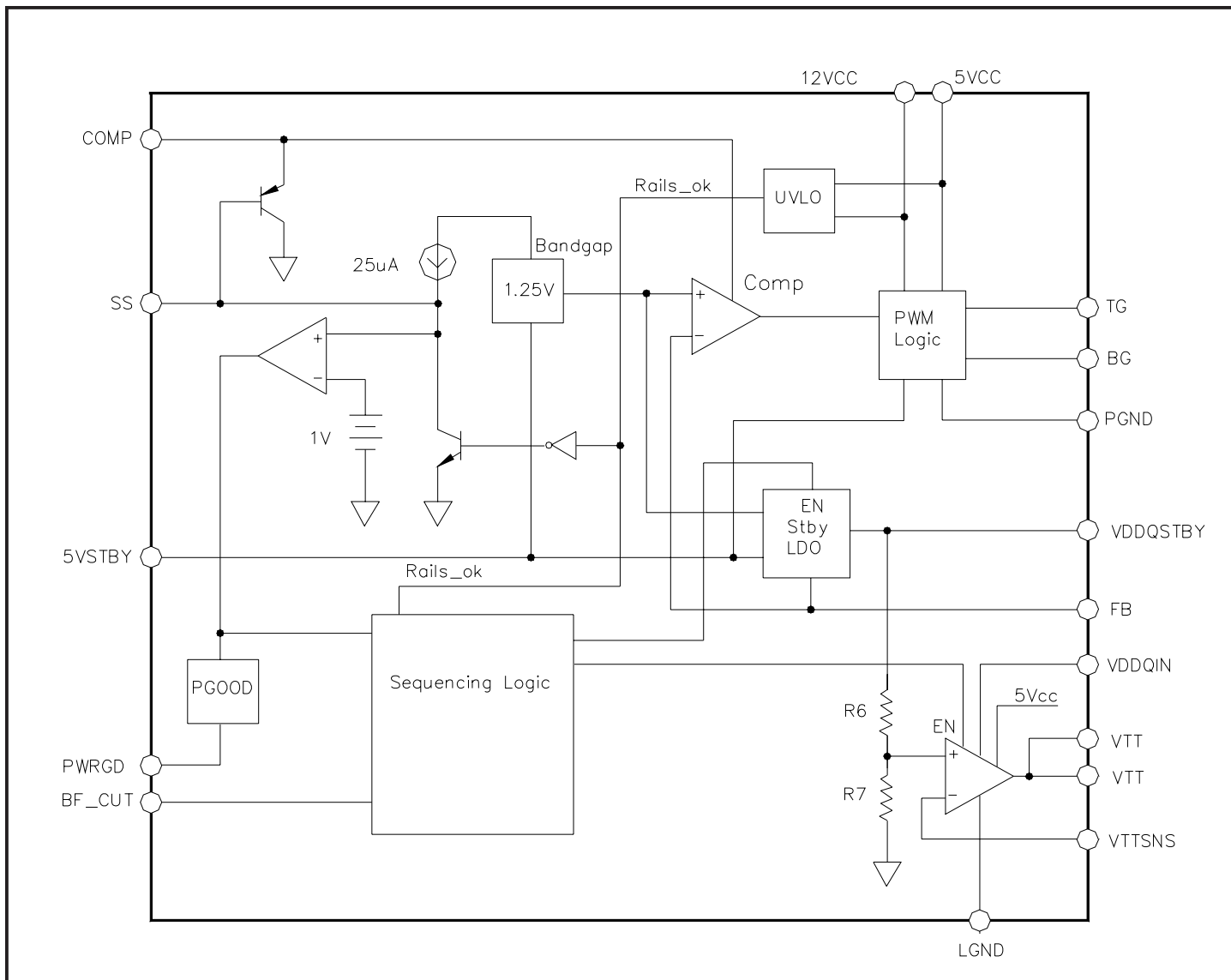
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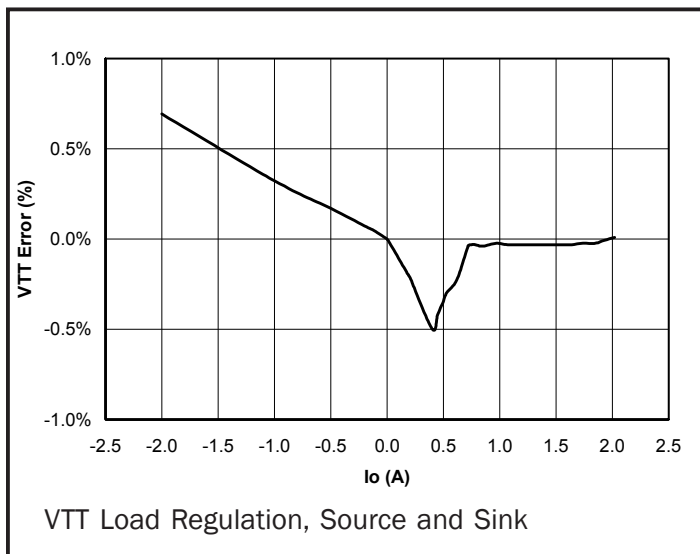
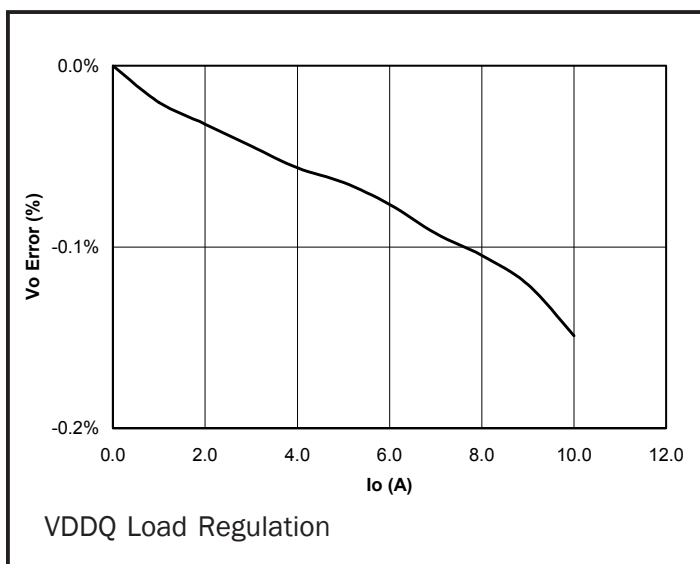
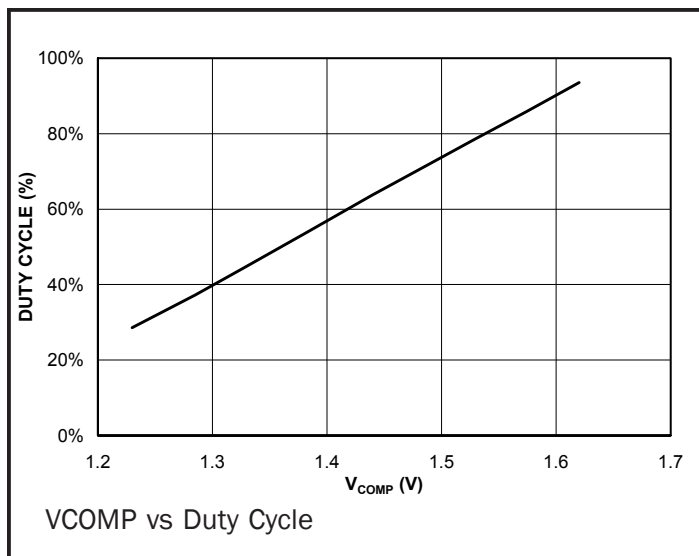
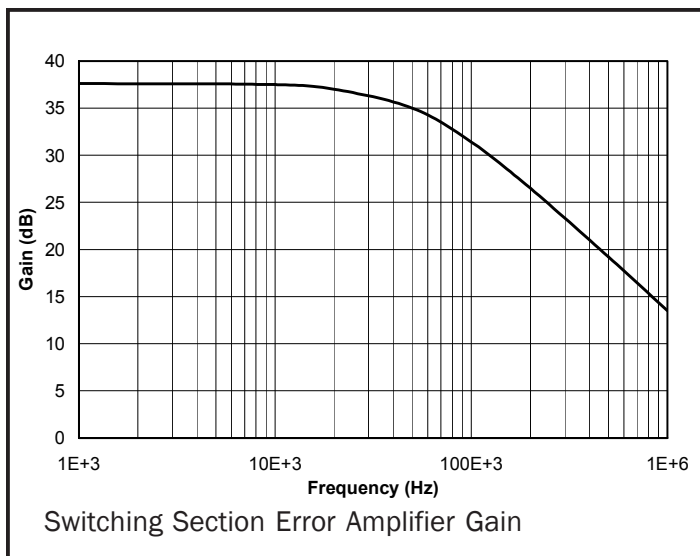
(1) Only available in tape and reel packaging. A reel contains 3000 devices.

### Pin Descriptions

Pin #	Pin Name	Pin Function
1	FB	Feedback for the STBY LDO and the switcher for VDDQ.
2	VTTSENS	VTT LDO feedback and remote sense input.
3	LGND	VTT return. Connect to point of load return. The trace connecting to this pin must be able to carry 2 Amps.
4	5VSBY	Bias supply for the chip. Connect to 5V standby.
5, 6	VTT	Regulator output. Regulates to 1/2 VDDQ. Sources or sinks current. 2 Amp source capability.
7	VDDQSTBY	S3 VDDQ output.
8	VDDQIN	VDDQ power input to VTT LDO. Must carry 2 Amps.
9	5VCC	Supply to the lower gate drive.
10	PWRGD	Switcher powergood and internal enable to VTT LDO.
11	BF_CUT	This pin will enable the STBY LDO in S3.
12	AGND	Analog ground.
13	PGND	Gate drive return. Keep this pin close to bottom FET source.
14	BG	Bottom gate drive.
15	TG	Top gate drive.
16	12VCC	Supply to the upper and lower gate drives.
17	COMP	Compensation pin for the PWM transconductance amplifier.
18	SS/EN	Soft start capacitor to GND. Pull low to disable.
19	TH_PAD	Internally Connected to AGND.

**Timing Diagram**


**POWER MANAGEMENT**
**Block Diagram**


**POWER MANAGEMENT**
**Typical Characteristics**


## POWER MANAGEMENT

## Evaluation Board Schematic

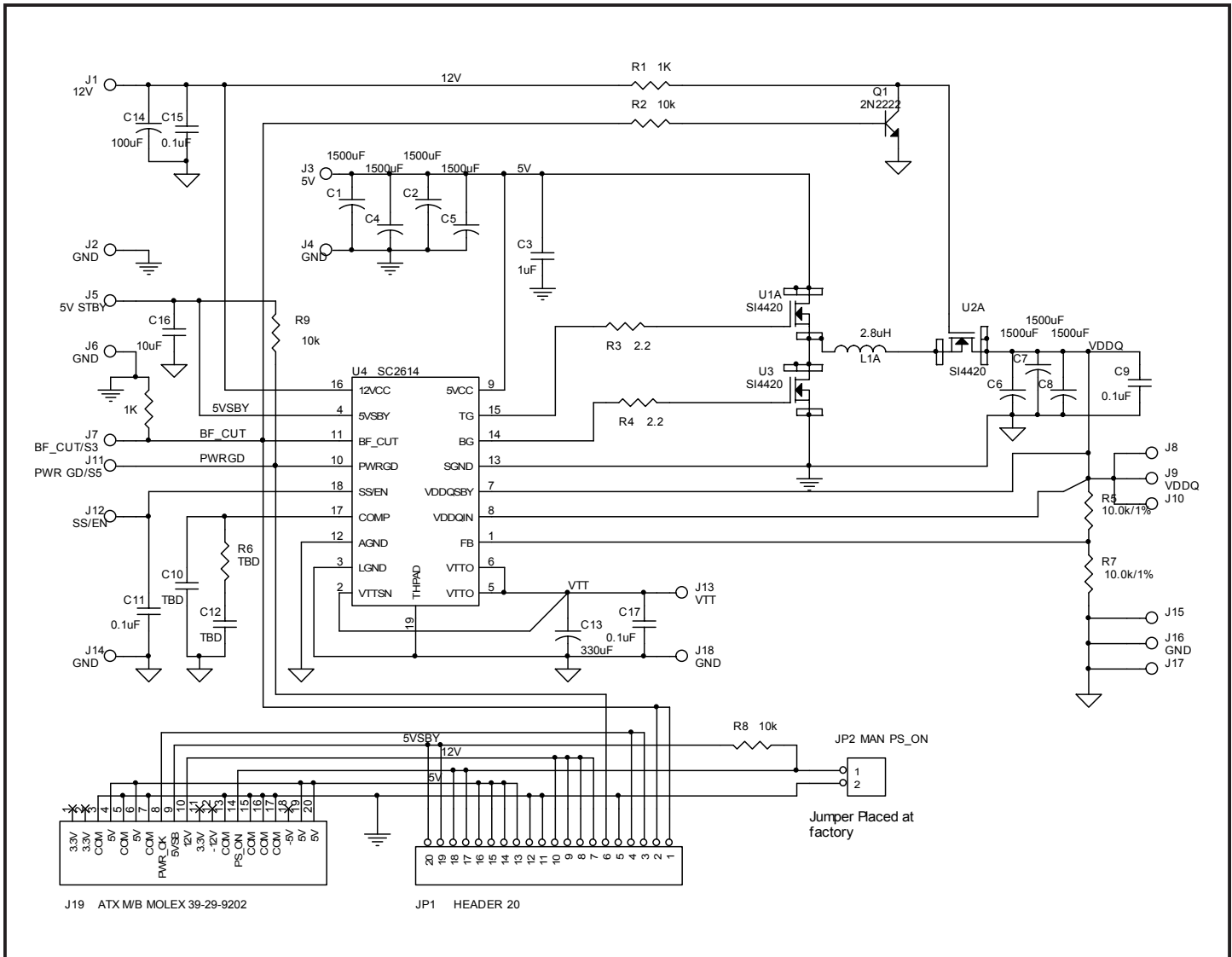


Figure 2: Evaluation Board Schematic



## POWER MANAGEMENT

### Applications Information

#### Description

The Semtech SC2614 DDR power supply controller is the latest and most complete, three in one, switching and linear regulator, providing the necessary functions to comply with S3 and S5 sleep state signals generated by the Desktop Computer Motherboards. The SC2614 uses the **BF\_CUT** input signal which is generated externally on Intel P4 Motherboard glue chip to comply with the power sequencing requirements.

Logically, the BF\_CUT signal can be represented as:

$BF\_CUT = S0 \cdot NAND.P\_OK$

Where S0 is the state of the operation, S0=high for S0 and Low for S3. P\_OK is a signal generated by the Silverbox supply, indicating that all rails are within specification .

The BF\_CUT signal is inverted to drive a **Back\_Feed\_Cut** MOSFET. The **Back\_Feed\_Cut** MOSFET prevents current flow from the VDDq supply back to the 5V supply during S3 state (when BF\_CUT is high). VDDQ supply and the VTT termination voltages are supplied to the Memory bus during S0 (normal operation).

During S0, VDDQ is supplied via the Switching regulator, sourcing high output currents to the VDD bus which in turn sources the termination supply current. The SC2614 is capable of driving a 4000pf capacitor in 25ns (typical, top gate). This drive capability allows 15-20A DC load on the VDDQ supply.

The VTT termination voltage is an internal sink/source linear regulator, which during S0 state receives its power from the VDDQ bus. It is capable of sourcing and sinking 2 Amps (max). The current limit on this pin is set to 3 Amps (typical). The current handling capacity of this pin depends upon the amount of heat the PC board can sink from the SC2614 thermal pad. (See mounting instructions). The PC board layout must take into consideration the high current paths, and ground returns for both the VDDQ and VTT supply pins. VTT, LGND, VDDQ, 5VCC and PGND traces must also be routed using wide traces to minimize power loss and heat in these traces, based on the current handling requirements.

#### S3 and S5 States

During S3 and S5 sleep states, The BF\_CUT signal is pulled high (see the timing diagram). The operation of the VDDQ and VTT supplies is governed by the internal sequencing logic in strict adherence with intel™ specifications with regards to the BF\_CUT signal. The timing diagram demonstrates the state of the controller, and each of the VDDQ and VTT supplies during S3 and S5 transitions. When S3 is low, the VDDQ supplies the “Suspend To RAM” current of 650 mA (max) to maintain the information in memory while in standby mode. The VTT termination voltage is not needed during this state, and is thus tri-stated. Once BF\_CUT goes low, the VDDQ switcher recovers and takes control of the VDDQ supply voltage.

The SS/EN pin must be pulled low and high again to restart the SC2614. This can be achieved by cycling the input supplies, 5V or 12V.

#### Initial Conditions

With the S5 and S3 go high (BF\_CUT goes low) for the first time, the VDDQ is supplied by the Switcher, thus removing the burden of charging the output capacitors via the linear VDDQ regulator.

#### Back-feeding the Input Supply

When in S3 state, VDDQ is supplied by the linear regulator and current can flow back from the VDDQ supply through the body diode of the Top switching MOSFET to the 5V supply in the Silver Box. Since the 5VCC is off during this state, this back flow of current in effect shorts out the VDDQ supply and is not desirable.

The blocking MOSFET is driven from the inverted BF\_CUT signal, as shown in figure 2 (Evaluation Board Schematic). When the gate voltage for this series MOSFET is low, the current can not flow from the VDDQ supply back into the input power source.

#### Current Limit

Current limit is implemented by sensing the VDDQ voltage. If it falls to 60% off its nominal voltage, as sensed by the FB pin, the TG and BG pins are latched off and the switcher and the linear controllers are shutdown. To

## POWER MANAGEMENT

### Applications Information (Cont.)

recover from the current limit condition, either the power rails, 5VCC /12VCC have to be recycled, or the SS/EN pin must be pulled low and released to restart switcher operation.

#### Thermal Shutdown

There are three independent Thermal Shutdown protection circuits in the SC2614: The VDDQ linear regulator, the VTT source regulator, and the VTT sink regulator. If any of the three regulators' temperature rises above the threshold, that regulator will turn off independently, until the temperature falls below the thermal shutdown limit.

#### Compensation Components -

Once the filter components have been determined, the compensation components can be calculated. The goal of compensation is to modify the frequency response characteristics of the error amplifier to ensure that the closed loop feedback system has the highest gain and bandwidth possible while maintaining stability.

A simplified stability criteria states that the open loop gain of the converter should fall through 0dB at 20dB/decade at a frequency no higher than 20-25% of the switching frequency.

This objective is most simply met by generating asymptotic bode plots of the small signal response of the various sections of the converter.

It is convenient to split the converter into two sections, the Error amp and compensation components being one section and the Modulator, output filter and divider being the other.

First calculate the DC Filter + Modulator + Divider gain. The DC filter gain is always 0dB, the Modulator gain is 19dB at 5V in and is proportional to  $V_{in}$ , so modulator gain at any input voltage is.

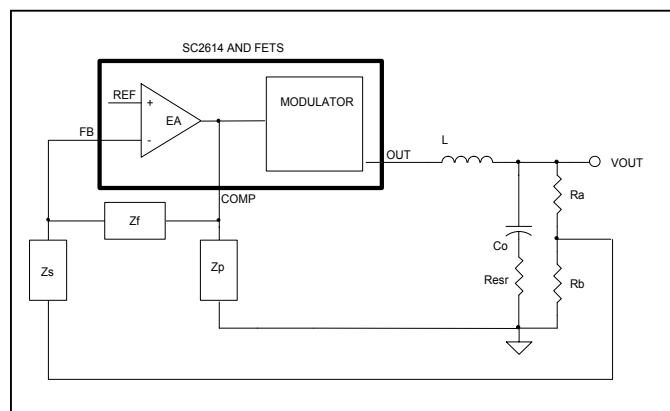
$$G_{MOD} = 19 + 20 \cdot \log\left(\frac{V_{IN}}{5}\right)$$

the divider gain is given by

$$G_{DIV} = 20 \cdot \log\left(\frac{R_8}{R_5 + R_8}\right)$$

So the total Filter + Modulator + Divider DC Gain is

$$G_{FMD} = 19 + 20 \cdot \log\left(\frac{V_{IN}}{5}\right) + 20 \cdot \log\left(\frac{R_8}{R_5 + R_8}\right)$$



Calculate the filter double pole frequency ( $F_p(lc)$ )

$$F_p(lc) = \frac{1}{2\pi\sqrt{LC_o}}$$

and calculate ESR Zero frequency ( $F_z(esr)$ )

$$F_z(esr) = \frac{1}{2\pi \cdot C_o \cdot Resr}$$

Choose an open loop crossover frequency ( $F_{co}$ ) no higher than 20% of the switching frequency ( $F_s$ ).

The proximity of  $F_z(esr)$  to the crossover frequency  $F_{co}$  determines the type of compensation required, if  $F_z(esr) > F_{co}/4$ , use type 3 compensation, otherwise use type 2. Type 1 compensation is not appropriate and is not discussed here.

#### Type 2 Example

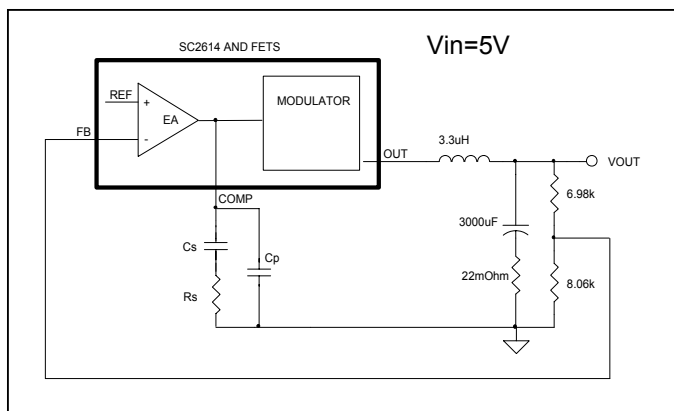
As an example of type 2 compensation, we will use the Evaluation board schematic.

The total Filter+Modulator+Divider DC Gain is:

$$G_{FMD} = 19 + 20 \cdot \log\left(\frac{5}{5}\right) + 20 \cdot \log\left(\frac{8.06}{6.98 + 8.06}\right) = 13.6\text{dB}$$

This is drawn as the line A-B in Fig. 2

$$F_p(lc) = \frac{1}{2\pi\sqrt{LC_o}} = \frac{1}{2\pi\sqrt{3.3 \cdot 10^{-6} \cdot 3000 \cdot 10^{-6}}} \approx 1.6 \text{ kHz}$$



This is point B in figure 2.

$$F_z(\text{esr}) = \frac{1}{2\pi \cdot 3000 \cdot 10^{-6} \cdot 22 \cdot 10^{-3}} = 2.4 \text{ kHz}$$

This is point C in Fig. 2., the line joining B-C slopes at -40dB/decade, the line joining C-D slopes at -20dB/decade.

For 600kHz switching frequency, crossover is designed for 100kHz.

Since  $F_z(\text{esr}) \ll F_{co}/4$  Type 2 compensation is appropriate. Having plotted the line ABCD, and confirmed the type of compensation necessary, compensation component values can be determined.

At  $F_{co}$ , the line ABCD shows a gain of -27.5dB and a slope of -20dB/decade. In order for the total open loop gain to be 0dB with a -20dB/decade slope at this frequency, the compensated error amp gain at  $F_{co}$  must be +27.5dB with a 0dB slope. This is the line FG on the plot below.

Since open loop DC gain should be as high as possible to minimize errors, a zero is placed at F and to minimize high frequency gain and switching interference a pole is placed at G.

The zero at F should be no higher than  $F_{co}/4$  and the pole at G no lower than  $4 \cdot F_{co}$ . The equations to set the gain and the pole and zero locations are:

$$R_s = \frac{10^{\frac{A}{20}}}{g_m} \text{ where } A = \text{gain at } F_{co} \text{ (in dB)}$$

$$C_s = \frac{1}{2\pi \cdot |F_z| \cdot R_s}$$

$$C_p = \frac{1}{2\pi \cdot F_{p1} \cdot R_s}$$

For this example, this results in the following values.

$$R_s = \frac{10^{\frac{27.5}{20}}}{0.8} = 29.6\text{k}\Omega \approx 30\text{k}\Omega$$

$$C_s \approx \frac{1}{6 \cdot 25 \cdot 10^3 \cdot 30 \cdot 10^3} = 0.22 \text{ nF}$$

$$C_p \approx \frac{1}{6 \cdot 400 \cdot 10^3 \cdot 30 \cdot 10^3} = 14 \text{pF (unnecessary due to EA rolloff)}$$

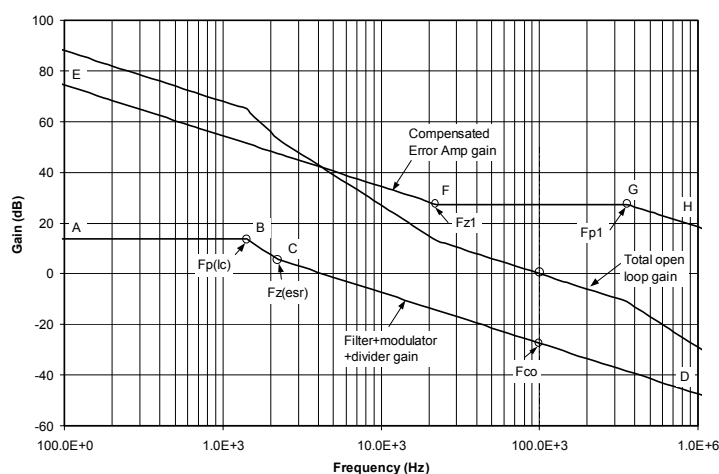


Fig. 3: Type 2 Error Amplifier Compensation

**Power Good**

An open collector output provides indication that the VDDq switcher is in regulation. This is accomplished by monitoring the SS/EN pin. When the voltage on this pin has risen above 1.0V, PGOOD goes high (open). When BF\_CUT goes high (standby), the 5V and 12V rails go low, and the SS/EN also goes low. Subsequently, PWRGD will also go low, and stays low until the 5V and 12V rails are recycled and rise above their respective UVLO thresholds.

**POWER MANAGEMENT****Mounting Considerations****Description**

The MLP18 is a leadless package whose electrical connections are made by lands on the bottom surface of the component. These lands are soldered directly to the PC board. The MLP has an exposed die attach pad, which enhances the thermal and electrical characteristics enabling high power applications. Power handling capability of the MLP package is typically >2x the power of other common SMT packages, such as the TSSOP and SOIC packages. In order to take full advantage of this feature the exposed pad must be physically connected to the PCB substrate with solder.

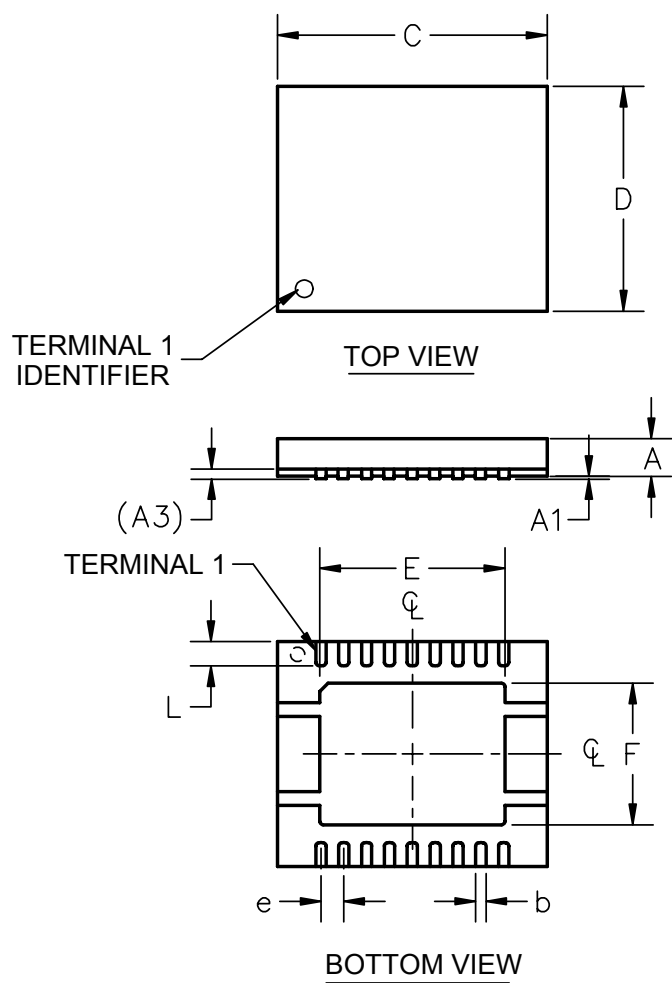
**Thermal Pad Via Design**

Thermal data for the MLP18 is based on a 4 layer PCB incorporating vias which act as the thermal path to other layers. (Ref: Jedec Specification JESD 51-5). Based on thermal performance, four-layer PCB's with vias are recommended to effectively remove heat from the device. Vias should be 0.3mm diameter on a 1.2mm pitch, and should be plugged to prevent voids being formed between the exposed pad and PCB thermal pad due to solder escaping by capillary action. Plugging can be accomplished by "tenting" the via during the solder mask process. The via solder mask diameter should be 100µm larger than the via diameter.

Two layer boards have less copper and thus typically require an increase in the PC board area for effective heatsinking. The copper area immediately surrounding the thermal pad connection must not be interrupted by routing traces.

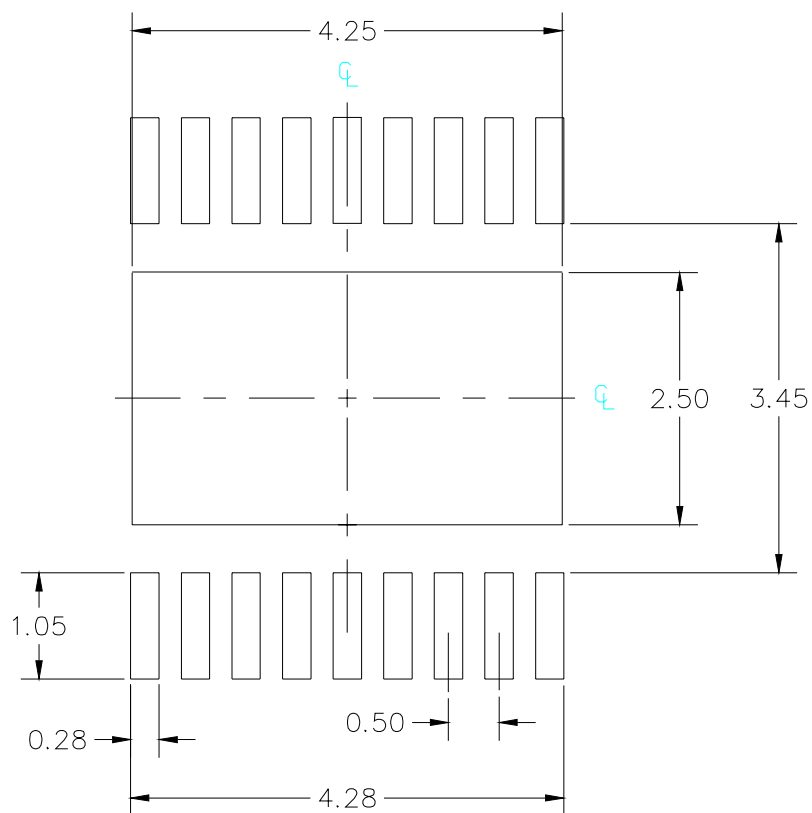
**Exposed Pad Stencil Design**

It is good practice to minimize the presence of voids within the exposed pad inter-connection. Total elimination is difficult but the design of the exposed pad stencil is important, a single slotted rectangular pattern is recommended. (If large exposed pads are screened with excessive solder, the device may "float", thus causing a gap between the MLP terminal and the PCB land metalization.) The proposed stencil designs enables out-gassing of the solder paste during reflow as well as controlling the finished solder thickness.



DIMENSIONS					
DIM <sup>N</sup>	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.032	.039	0.80	1.00	—
A1	0	.002	0	0.05	—
A3	—	.008	—	0.20	REF
b	.007	.012	0.18	0.30	—
C	.236		6.00		NOM
D	.197		5.00		NOM
E	.157	.167	4.00	4.25	—
F	.118	.128	3.00	3.25	—
e	.020	BSC	0.50	BSC	—
L	.017	.026	0.45	0.65	—

1 CONTROLLING DIMENSIONS: MILLIMETERS

**POWER MANAGEMENT**
**Land Pattern - MLP-18**


1 CONTROLLING DIMENSIONS: MILLIMETERS.

**Contact Information**

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