

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Ideal for Use in PC133 Register DIMM
- Typical Output Skew . . . <250 ps
- $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  . . . Normal Range
- $V_{CC} = 2.7\text{ V}$  to  $3.6\text{ V}$  . . . Extended Range
- $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$
- Rail-to-Rail Output Swing for Increased Noise Margin
- Balanced Output Drivers . . .  $\pm 18\text{ mA}$
- Low Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

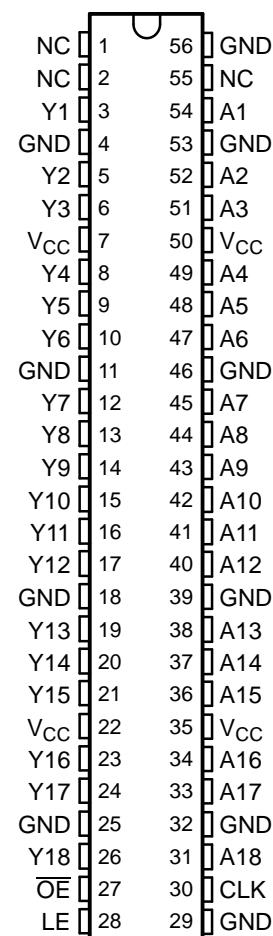
## DESCRIPTION/ORDERING INFORMATION

This 18-bit universal bus driver is designed for 2.3-V to 3.6-V  $V_{CC}$  operation.

Data flow from A to Y is controlled by the output-enable ( $\overline{OE}$ ) input. The device operates in the transparent mode when the latch-enable (LE) input is high. When LE is low, the A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The SN74ALVCF162835 has series damping resistors in the device output structure that reduce switching noise in 128-MB and 256-MB SDRAM modules. Designed with a drive capability of  $\pm 18\text{ mA}$ , this device is a midway drive between the SN74ALVC162835 ( $\pm 12\text{ mA}$ ) and SN74ALVC16835 ( $\pm 24\text{ mA}$ ).

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DL	Tube	SN74ALVCF162835DL	ALVCF162835
		Tape and reel	SN74ALVCF162835DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCF162835GR	ALVCF162835
	TVSOP - DGV	Tape and reel	SN74ALVCF162835VR	VF2835

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

**SN74ALVCF162835  
3.3-V CMOS 18-BIT UNIVERSAL BUS DRIVER  
WITH 3-STATE OUTPUTS**

SCES397A—JULY 2002—REVISED AUGUST 2004

 **TEXAS  
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**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

The SN74ALVCF162835 is a faster version of the SN74ALVC162835. It is suitable for PC133 applications and, particularly, SDRAM modules clocked at 133 MHz.

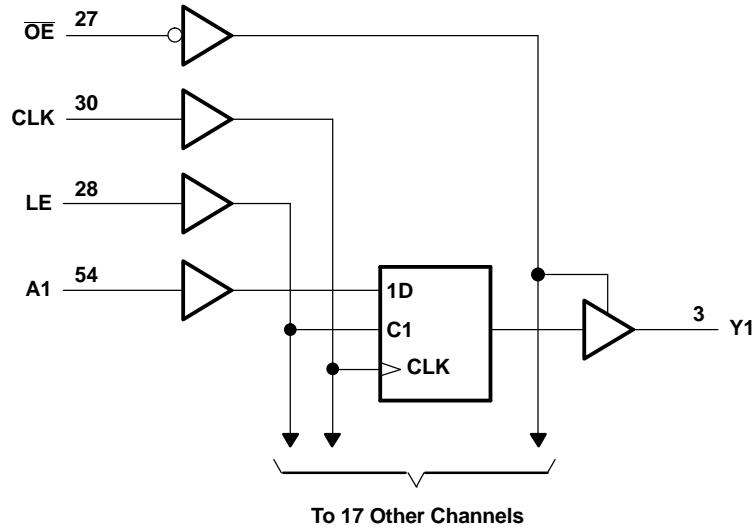
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**FUNCTION TABLE**

INPUTS				OUTPUT Y
$\overline{OE}$	LE	CLK	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L or H	X	$Y_0^{(1)}$

(1) Output level before the indicated steady-state input conditions were established

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
$V_O$	Output voltage range <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$ or $V_I < V_{CC}$		-50 mA
$I_{OK}$	Output clamp current	$V_O < 0$		-50 mA
$I_o$	Continuous output current			$\pm 50$ mA
Continuous current through each $V_{CC}$ or GND			$\pm 100$ mA	
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package		64 °C/W
		DGV package		48
		DL package		56
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.3	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.3$ V to 2.7 V		1.7
		$V_{CC} = 2.7$ V to 3.6 V		2
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.3$ V to 2.7 V		0.7
		$V_{CC} = 2.7$ V to 3.6 V		0.8
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.3$ V		-6
				-8
		$V_{CC} = 2.7$ V		-6
				-12
		$V_{CC} = 3$ V		-8
$I_{OL}$	Low-level output current			-18
		$V_{CC} = 2.3$ V		6
				8
		$V_{CC} = 2.7$ V		6
				12
		$V_{CC} = 3$ V		8
				18
$\Delta t/\Delta V$	Input transition rise or fall rate			10 ns/V
$T_A$	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN74ALVCF162835**  
**3.3-V CMOS 18-BIT UNIVERSAL BUS DRIVER**  
**WITH 3-STATE OUTPUTS**

SCES397A—JULY 2002—REVISED AUGUST 2004

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**ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>OH</sub>	I <sub>OH</sub> = -0.1 mA	2.3 V to 3.6 V	V <sub>CC</sub> - 0.2	1.9	2.2	V	
	I <sub>OH</sub> = -6 mA						
	I <sub>OH</sub> = -8 mA						
	I <sub>OH</sub> = -6 mA						
	I <sub>OH</sub> = -12 mA						
	I <sub>OH</sub> = -8 mA						
	I <sub>OH</sub> = -18 mA						
V <sub>OL</sub>	I <sub>OL</sub> = 0.1 mA	2.3 V to 3.6 V	V <sub>CC</sub> - 0.2	0.2	0.4	V	
	I <sub>OL</sub> = 6 mA						
	I <sub>OL</sub> = 8 mA						
	I <sub>OL</sub> = 6 mA						
	I <sub>OL</sub> = 12 mA						
	I <sub>OL</sub> = 8 mA						
	I <sub>OL</sub> = 18 mA						
V <sub>IK</sub>	V <sub>CC</sub> = 2.3 V, I <sub>I</sub> = -18 mA	3.6 V			-1.2	V	
V <sub>hys</sub>	V <sub>CC</sub> = 3.6 V	3.6 V			100	mV	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±5	µA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	µA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			0.1	40	µA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	µA	
C <sub>i</sub>	Inputs V <sub>I</sub> = 0 V	3.3 V			3.5	pF	
C <sub>o</sub>	Outputs V <sub>O</sub> = 0 V	3.3 V			4.5	pF	

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

**TIMING REQUIREMENTS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 and Figure 2)

			V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency				150			150	MHz
t <sub>w</sub>	Pulse duration	LE high	3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		
t <sub>su</sub>	Setup time	Data before CLK↑		1.8	1.5	1			ns
		Data before LE↓	CLK high	1.9	1.6	1.5			
			CLK low	1.3	1.1	1			
t <sub>h</sub>	Hold time	Data after CLK↑		0.6	0.6	0.6			ns
		Data after LE↓	CLK high or low	1.4	1.7	1.4			

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			150		150		150		MHz
$t_{pd}$	A	Y	1	4	4.6	1	3.5		ns
	LE		1.3	5.5	5.4	1.3	4.6		
	CLK		1.4	5.9	5.6	1.4	3.5		
$t_{en}$	$\overline{OE}$	Y	1.4	5.9	6	1.1	5		ns
$t_{dis}$	$\overline{OE}$	Y	1	4.7	4.6	1.3	4.2		ns
$t_{sk(0)}$							500	ps	

## SWITCHING CHARACTERISTICS

from 0°C to 65°C,  $C_L = 50\text{ pF}$

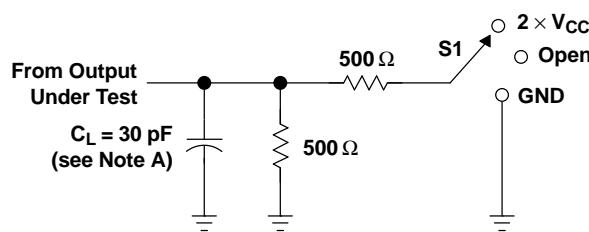
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		UNIT
			MIN	MAX	
$t_{pd}$	CLK	Y	1.8	3.5	ns

## OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

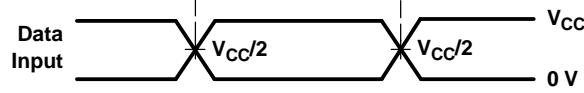
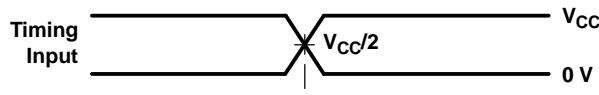
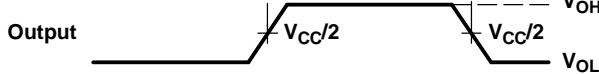
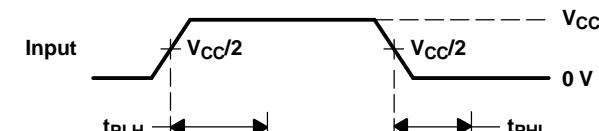
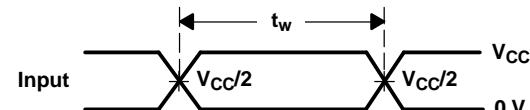
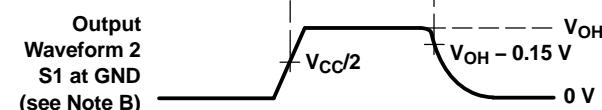
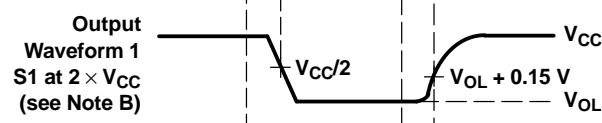
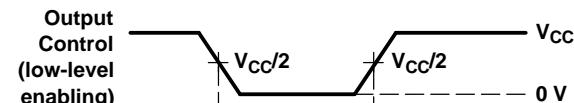
C <sub>pd</sub>	PARAMETER	TEST CONDITIONS	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	
Power dissipation capacitance	Outputs enabled	$C_L = 0\text{ pF}, f = 10\text{ MHz}$	27	33	pF
	Outputs disabled		16	21	

## PARAMETER MEASUREMENT INFORMATION

 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ 

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

## LOAD CIRCUIT

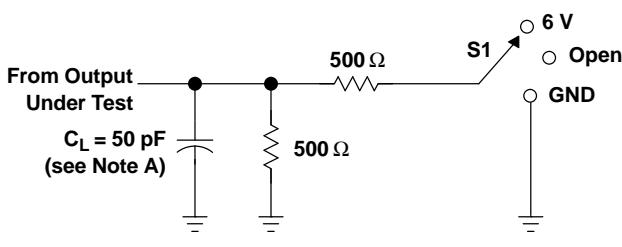
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMESVOLTAGE WAVEFORMS  
PULSE DURATIONVOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

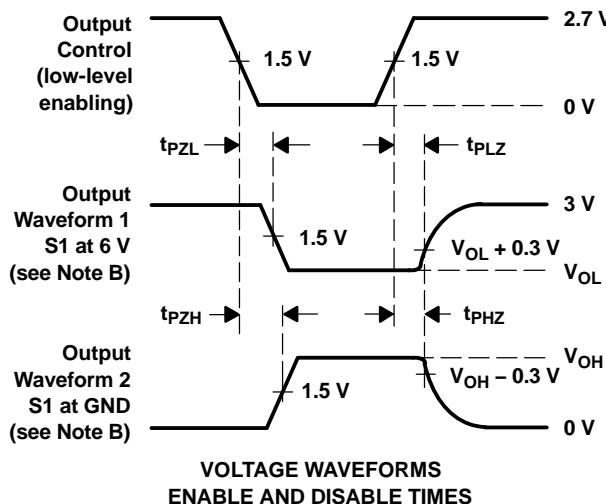
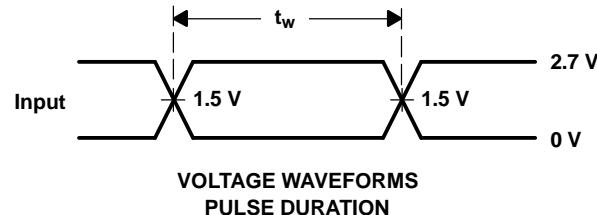
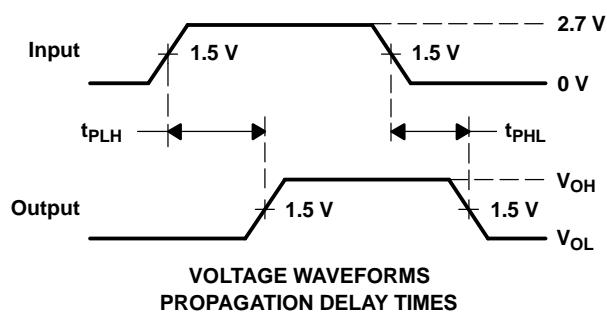
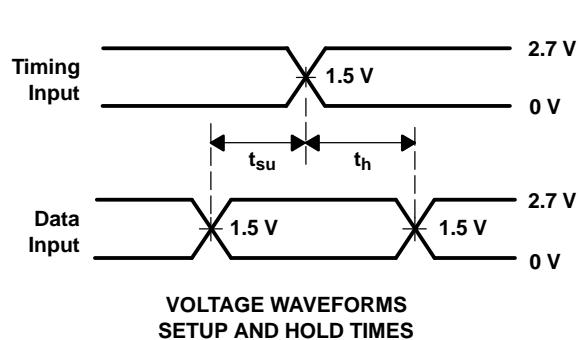
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND }3.3\text{ V} \pm 0.3\text{ V}$



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALVCF162835GR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCF162835	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74ALVCF162835VR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VF2835	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.



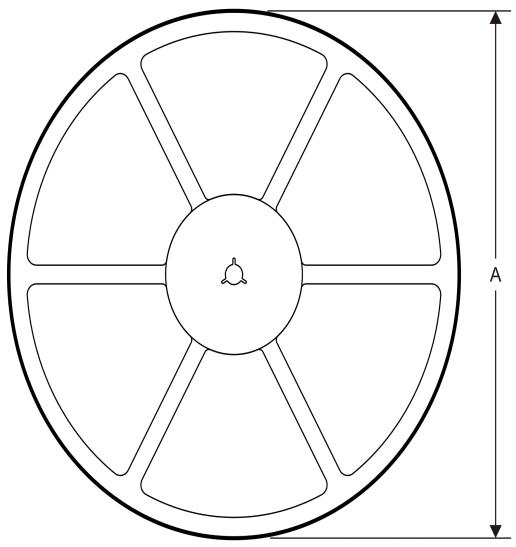
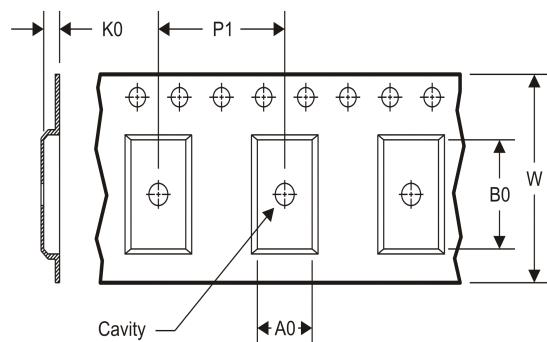
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## PACKAGE OPTION ADDENDUM

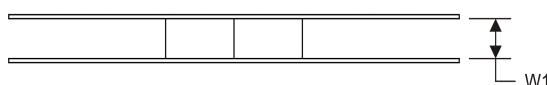
10-Jun-2014

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers


**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCF162835GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ALVCF162835VR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

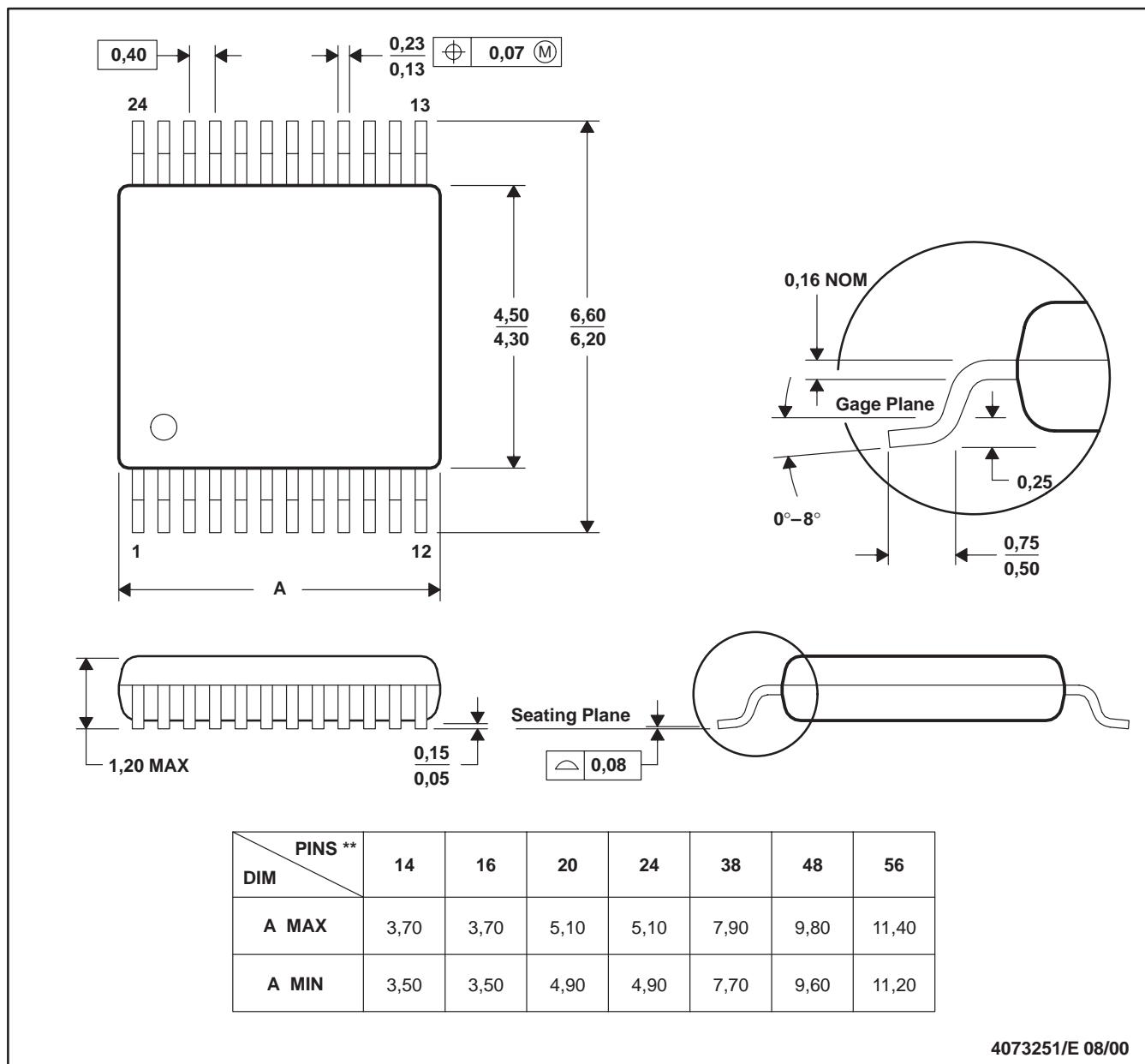
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCF162835GR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74ALVCF162835VR	TVSOP	DGV	56	2000	367.0	367.0	45.0

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

**24 PINS SHOWN**



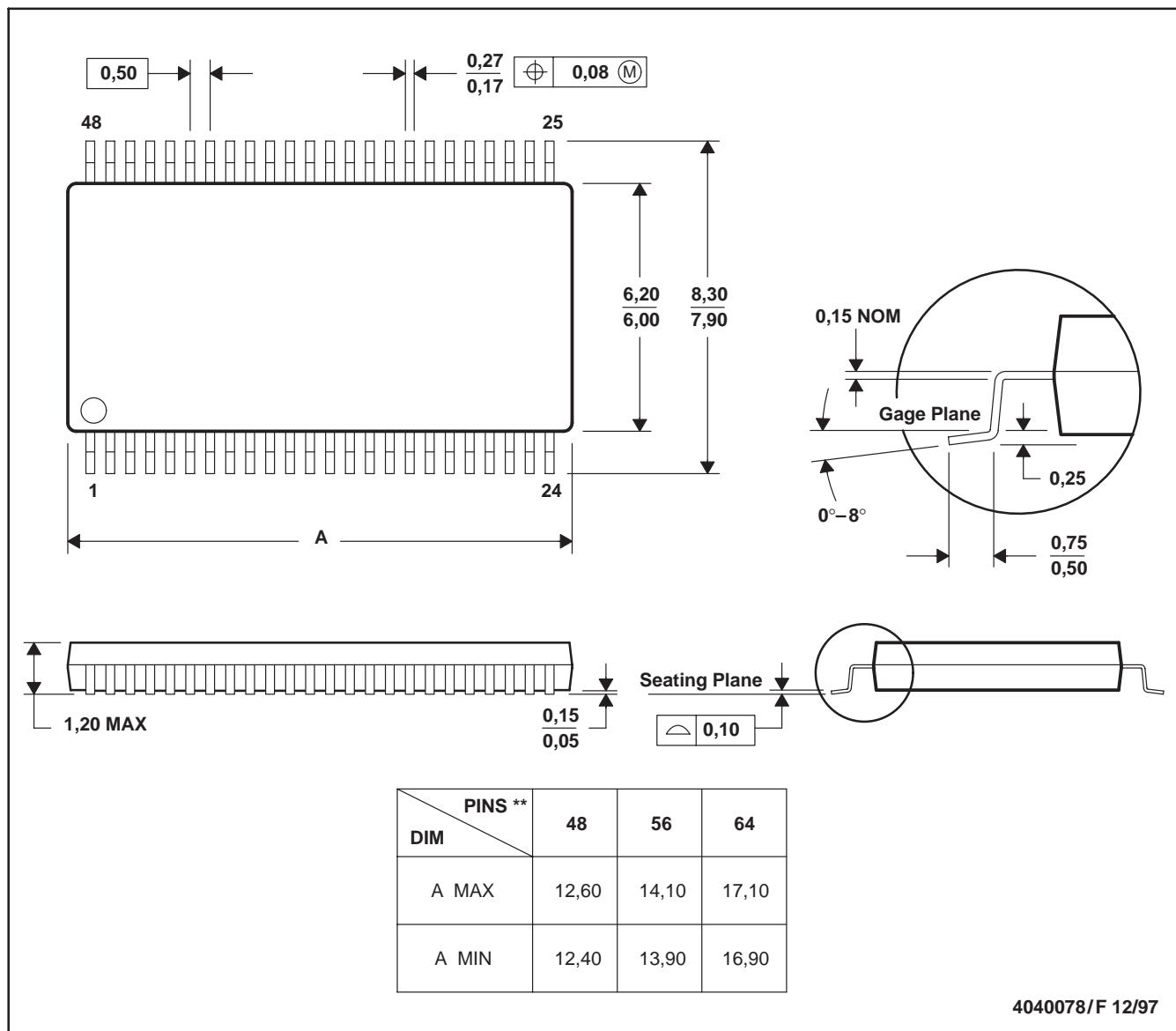
NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
D. Falls within JEDEC: 24/48 Pins – MO-153  
14/16/20/56 Pins – MO-194

14/16/20/56 Pins – MO-194

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

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