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NTE2764
Integrated Circuit
NMOS, 64K Erasable EPROM, 200ns

Description:

The NTE2764 is a 65,536–bit (8192 X 8 bit) Ultraviolet Erasable and Electrically Programmable Read–Only Memory (EPROM) in a 28–Lead DIP type package which operates from a single +5V supply, making it ideal for microprocessor applications. It features an output enable control and offers a standby mode with an attendant 67% savings in power consumption.

A distinctive feature of the NTE2764 is a separate output control, output enable ($\overline{OE}$) from the chip enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple–bus microprocessor systems. The NTE2764 features fast, simple one–pulse programming controlled by TTL–level signals. Total programming time for all 65,536 bits is 420 seconds.

Features:

- Ultraviolet Erasable and Electrically Programmable
- Access Time: 250ns Max
- Single Location Programming
- Programmable with Single Pulse
- Low Power Dissipation: 150mA Max (Active Current)
50mA Max (Standby Current)
- Input/Output TTL Compatible for Reading and Programming
- Single +5V Power Supply
- Three–State Outputs

Absolute Maximum Ratings: (T_A = +25°C, Note 1 unless otherwise specified)

Supply Voltage, V_{CC} . . . . . –0.6 to +6V
Supply Voltage, V_{PP} . . . . . –0.6 to +22V
Output Voltage, V_{OUT} . . . . . –0.6 to +6V
Input Voltage, V_{IN} . . . . . –0.6 to +6V
Operating Temperature Range, T_{opr} . . . . . –10°C to +80°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +125°C

Note 1. Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics: (V_{CC} = +5V ±5% unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Read Mode and Standby Mode (T_A = 0° to +70°C)						
Output High Voltage	V_{OH}	I_{OH} = –400µA	2.4	–	–	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Input High Voltage	V_{IH}		2.0	–	V_{CC} +1	V
Input Low Voltage	V_{IL}		–0.1	–	+0.8	V
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	µA
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	µA
V_{CC} Current Standby	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	50	mA
Active	I_{CC2}	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	–	–	150	mA
Program, Program Verify, and Program Inhibit Mode (T_A = +25° ±5°C, V_{PP} = +21V ±0.5V)						
Input High Voltage	V_{IH}		2.0	–	V_{CC} +1	V
Input Low Voltage	V_{IL}		–0.1	–	+0.8	V
Input Leakage Current	I_{LI}	V_{IN} = V_{IL} or V_{IN}	–	–	10	µA
Output High Voltage	V_{OH}	I_{OH} = –400µA	2.4	–	–	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
V_{CC} Current	I_{CC}		–	–	150	mA
V_{PP} Current	I_{PP}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = VIL	–	–	30	mA

AC Electrical Characteristics: (V_{CC} = +5V ±5% unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Read Mode and Standby Mode (T_A = 0° to +70°C, Note 2)						
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	–	250	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	–	250	ns
Output Enable to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	10	–	100	ns
Output Enable High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	–	90	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	–	ns
Read Mode and Standby Mode (T_A = +25°C ±5°C, V_{PP} = +21V ±5V, Note 3)						
Address Setup Time	t_{AS}		2	–	–	µs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	µs

Note 2. Test Conditions:

Output Load: 1 TTL gate and C_L = 100pF
Input Rise and fall Times: 20ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs: 1.0V and 2.0V
Outputs: 0.8V and 2.0V

Note 3. Test Conditions:

Input Pulse Levels: 0.8V to 2.2V
Input Timing Reference Level: 1.0V and 2.0V
Output Timing Reference Level: 0.8V and 2.0V
Input Rise and fall Times: 20ns

AC Electrical Characteristics (Cont'd): (V_{CC} = +5V ±5% unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Read Mode and Standby Mode (Cont'd) (T_A = +25°C ±5°C, V_{PP} = +21V ±5V, Note 3)						
Data Setup Time	t_{DS}		2	–	–	µs
Address Hold Time	t_{AH}		0	–	–	µs
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	µs
Data Hold Time	t_{DH}		2	–	–	µs
Chip Enable to Output Float Delay	t_{DF}		0	–	130	ns
Data Valid from $\overline{OE}$	t_{OE}		–	–	150	ns
Program Pulse Width	t_{PW}		45	50	55	ms
V_{PP} Setup Time	t_{VS}		2	–	–	µs

Note 3. Test Conditions:
Input Pulse Levels: 0.8V to 2.2V
Input Timing Reference Level: 1.0V and 2.0V
Output Timing Reference Level: 0.8V and 2.0V
Input Rise and fall Times: 20ns

Capacitance: (T_A = +25°C, f = 1MHz unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	–	12	pF

Mode Selection: (Note 4)

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	$O_0 - O_7$
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Stanby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z

Note 4. X can be either V_{IL} or V_{IH}.

Function:

The NTE2764 operates from a single +5V power supply, making it ideal for microprocessor applications.

Programming of the NTE2764 is achieved with a single 50ms TTL pulse. Total programming time for all 65,536 bits is 420 sec. Due to the simplicity of the programming requirements, devices on boards and in systems may be easily programmed without any special programmer.

The NTE2764 features a standby mode which reduces the power dissipation from a maximum active power dissipation of 788mW to a maximum standby power dissipation of 262mW. This results in a 67% savings with no increase in access time.

Erasure of the NTE2764 programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 Angstroms. It should be noted that constant exposure to direct sun-light or room level fluorescent lighting could erase the NTE2764. Consequently, if the NTE2764 is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure.

Function (Cont'd):

The recommended erasure procedure for the NTE2764 is exposure to ultraviolet light with wavelengths of 2,537 Angstroms. The integrated dose (i.e. UV intensity x exposure time) for erasure should be not less than 15W–sec/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12,000 μW/cm^2 power rating.

During erasure, the NTE2764 should be placed within 1 inch of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Operation:

The five operation modes of the NTE2764 are listed in the Mode Selection table. In READ mode, the only power supply required is a +5V supply. During programming, all inputs are TTL levels except for V_{PP} which is pulsed from TTL level to 21V.

Read Mode:

When $\overline{CE}$ and $\overline{OE}$ are at low (0) level, READ is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

Standby Mode:

The NTE2764 is placed in standby mode with the application of a high (1) level TTL signal to the CE input. In this mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input. The active power dissipation is reduced by 67% from 788mW to 262mW.

Programming:

Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The NTE2764 is placed in programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ and $\overline{PGM}$ with V_{pp} at +21V. The data to be programmed is applied to the output pins in 8–bit parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially or at random.

When multiple NTE2764s are connected in parallel except for $\overline{CE}$, individual NTE2764 can be programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ input of the desired NTE2764 to be programmed.

Programming of multiple NTE2764s in parallel with the same data is easily accomplished. All the like inputs are tied together and programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ inputs.

Programming Inhibit Mode:

Programming multiple NTE2764 in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$ (or $\overline{PGM}$) all like inputs (including $\overline{OE}$) of the parallel NTE2764 may be common. Programming is accomplished by applying a low (0) TTL–level program pulse to the $\overline{CE}$ (or $\overline{PGM}$) input with V_{PP} at +21V. A high (1) level applied to the CE (or $\overline{PGM}$) of the other NTE2764 will inhibit it from being programmed.

Program Verify Mode:

A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}$ at low (0) levels and PGM at high (1) level.

Output Deselect:

The data outputs of two or more NTE2764s may be wire–ORed together to the same data bus. In order to prevent bus contention problems between devices, all but the selected NTE2764s should be deselected by raising the $\overline{CE}$ input to a TTL high. $\overline{OE}$ input should be made common to all devices and connected to the READ line from the system control BUS. These connections offer the lowest average power consumption.

Pin Connection Diagram