Intel® Core™2 Duo Mobile Processor, Intel® Core™2 Solo Mobile Processor and Intel® Core™2 Extreme Mobile Processor on 45-nm Process

Datasheet

For platforms based on Mobile Intel® 4 Series Express Chipset Family

March 2009

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Contents

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Revision History

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320120	-001	Initial Release	July 2008
320120	-002	• Chapter Update — Chapter 1: Added introduction to the Intel Core 2 Duo Processor in SFF Package — Section 4.1: Added the package coplanarity information for the processors in SFF Package • Figure Update — Added Figure 7 — Added Figure 8 — Added Figure 14 — Added Figure 15 — Added Figure 18 through Figure 21 • Table Update — Added Table 9 — Added Table 10 — Added Table 11 — Added Table 12 — Updated Table 16: Added Intel Core 2 Duo SFF Package Processor Ball listing by Pin name — Added Table 18 — Added Table 23 — Added Table 24 — Added Table 25	August 2008
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1 Introduction

The Intel® Core™2 Duo mobile processor, Intel® Core™2 Duo mobile processor low-voltage (LV), ultra low-voltage (ULV) in small form factor (SFF) package and Intel® Core™2 Extreme mobile are high-performance, low-power mobile processor based on the Intel Core microarchitecture for Intel® Centrino® 2 processor technology.

This document contains electrical, mechanical and thermal specifications for the following processors:

- The Intel Core 2 Duo processors and Intel Core 2 Extreme processors support the Mobile Intel® 4 Series Express Chipset and Intel® ICH9M I/O controller.
  - Dual-core extreme edition (DC-XE)
  - Standard voltage (SV)
  - 25-W processor in standard package (Power Optimized Performance-POP)
- The Intel Core 2 Duo processor in SFF package supports the Mobile Intel® GS45 Express Chipset and Intel® ICH9M SFF I/O controller.

This document contains electrical, mechanical and thermal specifications for:

- Power Optimized Performance (POP) in SFF package
- Low-voltage (LV) Processor in SFF package
- Ultra-low voltage (ULV) dual-core (DC) and single-core (SC) Processors in SFF package

Notes: In this document

1. Intel Core 2 Duo processor, and the Intel Core 2 Extreme processor are referred to as the processor
2. Intel Core 2 Duo LV/ULV/POP processors are referred to as SFF processor
3. Mobile Intel 4 Series Express Chipset is referred as the GMCH.

Key features include:

- Dual-core processor for mobile with enhanced performance
- Supports Intel architecture with Intel® Wide Dynamic Execution
- Supports L1 cache-to-cache (C2C) transfer
- On-die, primary 32-KB instruction cache and 32-KB, write-back data cache in each core
- The processor in DC-XE, standard voltage (SV) and LV have an on-die, up to 6-MB second-level, shared cache with Advanced Transfer Cache architecture
- The processor in ULV single-core and dual-core have an on-die, up to 3-MB second-level, shared cache with Advanced Transfer Cache architecture
- Streaming SIMD extensions 2 (SSE2), streaming SIMD extensions 3 (SSE3), supplemental streaming SIMD extensions 3 (SSSE3) and SSE4.1 instruction sets
- The processor in DC-XE, SV and LV are offered at 1066-MHz, source-synchronous front side bus (FSB)
- The processor in ULV are offered at 800-MHz, source-synchronous FSB
- Advanced power management features including Enhanced Intel SpeedStep® Technology and dynamic FSB frequency switching

- Digital thermal sensor (DTS)
- Intel® 64 architecture
- Supports enhanced Intel® Virtualization Technology
- Enhanced Intel® Dynamic Acceleration Technology and Enhanced Multi-Threaded Thermal Management (EMTTM)
- Supports PSI2 functionality
- SV processor offered in Micro-FCPGA and Micro-FCBGA packaging technologies
- Processor in POP, LV and ULV are offered in Micro-FCBGA packaging technologies only
- Execute Disable Bit support for enhanced security
- Intel® Deep Power Down low-power state with P_LVL6 I/O support
- Support for Intel® Trusted Execution Technology
- Half ratio support (N/2) for core to bus ratio

1.1 Terminology

Term	Definition
#	A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the "#" symbol implies that the signal is inverted. For example, D[3:0] = "HLHL" refers to a hex 'A', and D[3:0]# = "LHLH" also refers to a hex "A" (H= High logic level, L= Low logic level).
Front Side Bus (FSB)	Refers to the interface between the processor and system core logic (also known as the chipset components).
AGTL+	Advanced Gunning Transceiver Logic. Used to refer to Assisted GTL+ signaling technology on some Intel processors.
Storage Conditions	Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
Enhanced Intel SpeedStep® Technology	Technology that provides power management capabilities to laptops.
Processor Core	Processor core die with integrated L1 and L2 cache. All AC timing and signal integrity specifications are at the pads of the processor core.

Term	Definition
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture.
Intel® Virtualization Technology	Processor virtualization that, when used in conjunction with Virtual Machine Monitor software, enables multiple, robust independent software environments inside a single platform.
Half ratio support (N/2) for Core to Bus ratio	Intel Core 2 Duo processors and Intel Core 2 Extreme processors support the N/2 feature that allows having fractional core-to-bus ratios. This feature provides the flexibility of having more frequency options and being able to have products with smaller frequency steps.
TDP	Thermal Design Power.
V_{CC}	The processor core power supply.
V_{SS}	The processor ground.
LV	Low-voltage
ULV	Ultra-Low-Voltage
DC-XE	Dual-core Extreme Edition

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document.

Document	Document Number
Intel® Core™2 Duo Mobile Processor, Intel® Core™2 Solo Mobile Processor, Intel® Core™2 Extreme Processor on 45-nm Technology Specification Update	320121
Mobile Intel® 4 Series Express Chipset Family Datasheet	320122
Mobile Intel® 4 Series Express Chipset Family Specification Update	320123
Intel® I/O Controller Hub 9 (ICH9)/ I/O Controller Hub 9M (ICH9M) Datasheet	316972
Intel® I/O Controller Hub 9 (ICH9)/ I/O Controller Hub 9M (ICH9M) Specification Update	316973
Intel® 64 and IA-32 Architectures Software Developer's Manuals	
Volume 1: Basic Architecture	253665
Volume 2A: Instruction Set Reference, A-M	253666

Document	Document Number
Volume 2B: Instruction Set Reference, N-Z	253667
Volume 3A: System Programming Guide	253668
Volume 3B: System Programming Guide	253669

NOTE: Contact your Intel representative for the latest revision of this document.

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2 Low Power Features

2.1 Clock Control and Low-Power States

The processor supports low-power states both at the individual core level and the package level for optimal power management.

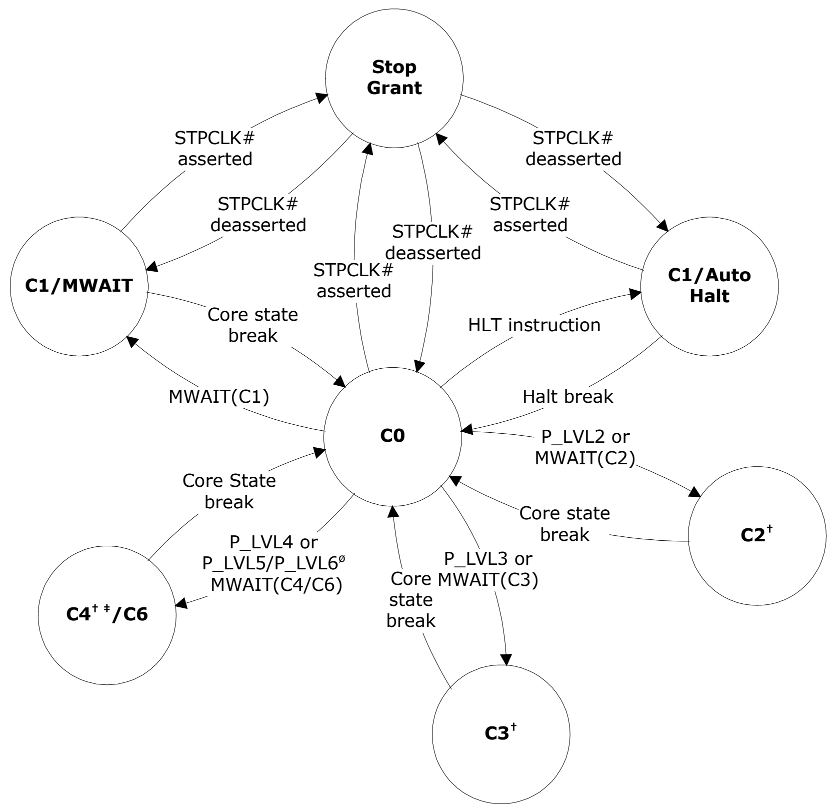
A core may independently enter the C1/AutoHALT, C1/MWAIT, C2, C3, C4, Intel® Enhanced Deeper Sleep and Intel® Deep Power Down Technology low-power states. When both cores coincide in a common core low-power state, the central power management logic ensures the entire processor enters the respective package low-power state by initiating a P_LVLx (P_LVL2, P_LVL3, P_LVL4, P_LVL5,P_LVL6) I/O read to the GMCH.

The processor implements two software interfaces for requesting low-power states: MWAIT instruction extensions with sub-state hints and P_LVLx reads to the ACPI P_BLK register block mapped in the processor's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor and do not directly result in I/O reads on the processor FSB. The P_LVLx I/O Monitor address does not need to be set up before using the P_LVLx I/O read interface. The sub-state hints used for each P_LVLx read can be configured through the IA32_MISC_ENABLES model specific register (MSR).

If a core encounters a GMCH break event while STPCLK# is asserted, it asserts the PBE# output signal. Assertion of PBE# when STPCLK# is asserted indicates to system logic that individual cores should return to the C0 state and the processor should return to the Normal state.

Figure 1 shows the core low-power states and Figure 2 shows the package low-power states for the processor. Table 1 maps the core low-power states to package low-power states.

Figure 1. Core Low-Power States



halt break = A20M# transition, INIT#, INTR, NMI, PREQ#, RESET#, SMI#, or APIC interrupt
core state break = (halt break OR Monitor event) AND STPCLK# high (not asserted)
† — STPCLK# assertion and de-assertion have no effect if a core is in C2, C3, or C4.
‡ — Core C4 state supports the package level Deep C4 sub-state.
Ø — P_LVL5/P_LVL6 read is issued once the L2 cache is reduced to zero.

Figure 2. Package Low-Power States

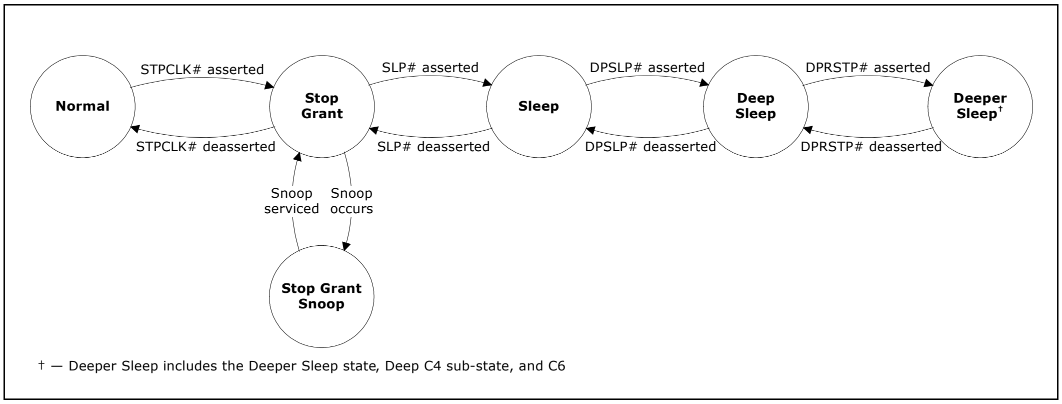


Table 1. Coordination of Core Low-Power States at the Package Level

Package State	Core1 State				
Core0 State	**C0**	**C1[1]**	**C2**	**C3**	**C4/Deep Power Down Technology State (Code Named C6 State)**
C0	Normal	Normal	Normal	Normal	Normal
C1[1]	Normal	Normal	Normal	Normal	Normal
C2	Normal	Normal	Stop-Grant	Stop-Grant	Stop-Grant
C3	Normal	Normal	Stop-Grant	Deep Sleep	Deep Sleep
C4/Deep Power Down Technology	Normal	Normal	Stop-Grant	Deep Sleep	Deeper Sleep /Intel® Enhanced Deeper Sleep/ Intel® Deep Power Down

NOTE:
1. AutoHALT or MWAIT/C1.

2.1.1 Core Low-Power State Descriptions

2.1.1.1 Core C0 State

This is the normal operating state for cores in the processor.

2.1.1.2 Core C1/AutoHALT Powerdown State

C1/AutoHALT is a low-power state entered when a core executes the HALT instruction. The processor core will transition to the C0 state upon occurrence of SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt messages. RESET# will cause the processor to immediately initialize itself.

A System Management Interrupt (SMI) handler will return execution to either Normal state or the AutoHALT Powerdown state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 3A/3B: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Powerdown state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT Powerdown state, the dual-core processor will process bus snoops and snoops from the other core. The processor core will enter a snoopable sub-state (not shown in Figure 1) to process the snoop and then return to the AutoHALT Powerdown state.

2.1.1.3 Core C1/MWAIT Powerdown State

C1/MWAIT is a low-power state entered when the processor core executes the MWAIT(C1) instruction. Processor behavior in the MWAIT state is identical to the AutoHALT state except that Monitor events can cause the processor core to return to the C0 state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 2A: Instruction Set Reference, A-M* and *Volume 2B: Instruction Set Reference, N-Z*, for more information.

2.1.1.4 Core C2 State

Individual cores of the dual-core processor can enter the C2 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C2) instruction, but the processor will not issue a Stop-Grant Acknowledge special bus cycle unless the STPCLK# pin is also asserted.

While in the C2 state, the dual-core processor will process bus snoops and snoops from the other core. The processor core will enter a snoopable sub-state (not shown in Figure 1) to process the snoop and then return to the C2 state.

2.1.1.5 Core C3 State

Individual cores of the dual-core processor can enter the C3 state by initiating a P_LVL3 I/O read to the P_BLK or an MWAIT(C3) instruction. Before entering C3, the processor core flushes the contents of its L1 caches into the processor's L2 cache. Except for the caches, the processor core maintains all its architectural states in the C3 state. The Monitor remains armed if it is configured. All of the clocks in the processor core are stopped in the C3 state.

Because the core's caches are flushed the processor keeps the core in the C3 state when the processor detects a snoop on the FSB or when the other core of the dual-core processor accesses cacheable memory. The processor core will transition to the C0 state upon occurrence of a Monitor event, SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt message. RESET# will cause the processor core to immediately initialize itself.

2.1.1.6 Core C4 State

Individual cores of the dual-core processor can enter the C4 state by initiating a P_LVL4 or P_LVL5 I/O read to the P_BLK or an MWAIT(C4) instruction. The processor core behavior in the C4 state is nearly identical to the behavior in the C3 state. The only difference is that if both processor cores are in C4, the central power management logic will request that the entire processor enter the Deeper Sleep package low-power state (see Section 2.1.2.6).

To enable the package-level Intel Enhanced Deeper Sleep state, Dynamic Cache Sizing and Intel Enhanced Deeper Sleep state fields must be configured in the PMG_CST_CONFIG_CONTROL MSR. Refer to Section 2.1.2.6 for further details on Intel Enhanced Deeper Sleep state.

2.1.1.7 Core Deep Power Down Technology (Code Name C6) State

Deep Power Down Technology state is a new, power-saving state which is being implemented on the processor. In Deep Power Down Technology the processor saves its entire architectural state onto an on-die SRAM hence allowing it to lower its main core voltage to any value, even as low as 0-V.

When the core enters Deep Power Down Technology state, it saves the processor state that is relevant to the processor context in an on-die SRAM that resides on a separate power plane V_{CCP} (I/O power supply). This allows the main core Vcc to be lowered to any arbitrary voltage including 0-V. The on-die storage for saving the processor state is implemented as a per-core SRAM.

2.1.2 Package Low-power State Descriptions

2.1.2.1 Normal State

This is the normal operating state for the processor. The processor remains in the Normal state when at least one of its cores is in the C0, C1/AutoHALT, or C1/MWAIT state.

2.1.2.2 Stop-Grant State

When the STPCLK# pin is asserted, each core of the dual-core processor enters the Stop-Grant state within 20 bus clocks after the response phase of the processor-issued Stop-Grant Acknowledge special bus cycle. Processor cores that are already in the C2, C3, or C4 state remain in their current low-power state. When the STPCLK# pin is deasserted, each core returns to its previous core low-power state.

Since the AGTL+ signal pins receive power from the FSB, these pins should not be driven (allowing the level to return to V_{CCP}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the FSB should be driven to the inactive state.

RESET# causes the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. When RESET# is asserted by the system, the STPCLK#, SLP#, DPSLP#, and DPRSTP# pins must be deasserted prior to RESET# deassertion as per AC Specification T45. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should be deasserted after the deassertion of SLP# as per AC Specification T75.

While in Stop-Grant state, the processor will service snoops and latch interrupts delivered on the FSB. The processor will latch SMI#, INIT# and LINT[1:0] interrupts and will service only one of each upon return to the Normal state.

The PBE# signal may be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt or Monitor event latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that the entire processor should return to the Normal state.

A transition to the Stop-Grant Snoop state occurs when the processor detects a snoop on the FSB (see Section 2.1.2.3). A transition to the Sleep state (see Section 2.1.2.4) occurs with the assertion of the SLP# signal.

2.1.2.3 Stop-Grant Snoop State

The processor responds to snoop or interrupt transactions on the FSB while in Stop-Grant state by entering the Stop-Grant Snoop state. The processor will stay in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB) or the interrupt has been latched. The processor returns to the Stop-Grant state once the snoop has been serviced or the interrupt has been latched.

2.1.2.4 Sleep State

The Sleep state is a low-power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and stops all internal clocks. The Sleep state is entered through assertion of the SLP# signal while in the Stop-Grant state. The SLP# pin should only be asserted when the processor is in the Stop-Grant state. SLP# assertions while the processor is not in the Stop-Grant state is out of specification and may result in unapproved operation.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP#, DPSLP# or RESET#) are allowed on the FSB while the processor is in Sleep state. Snoop events that occur while in Sleep state or during a transition into or out of Sleep state will cause unpredictable behavior. Any transition on an input signal before the processor has returned to the Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through the Stop-Grant state. If RESET# is driven active while the processor is in the Sleep state, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering an even lower power state, the Deep Sleep state, by asserting the DPSLP# pin (See Section 2.1.2.5). While the processor is in the Sleep state, the SLP# pin must be deasserted if another asynchronous FSB event needs to occur.

2.1.2.5 Deep Sleep State

The Deep Sleep state is entered through assertion of the DPSLP# pin while in the Sleep state. BCLK may be stopped during the Deep Sleep state for additional platform-level power savings. BCLK stop/restart timings on appropriate GMCH-based platforms with the CK505 clock chip are as follows:

- **Deep Sleep entry:** the system clock chip may stop/tristate BCLK within 2 BCLKs of DPSLP# assertion. It is permissible to leave BCLK running during Deep Sleep.
- **Deep Sleep exit:** the system clock chip must drive BCLK to differential DC levels within 2-3 ns of DPSLP# deassertion and start toggling BCLK within 10 BCLK periods.

To re-enter the Sleep state, the DPSLP# pin must be deasserted. BCLK can be re-started after DPSLP# deassertion as described above. A period of 15 microseconds (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep state. Once in the Sleep state, the SLP# pin must be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions of signals are allowed on the FSB while the processor is in Deep Sleep state. When the processor is in Deep Sleep state, it will not respond to interrupts or snoop transactions. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

2.1.2.6 Deeper Sleep State

The Deeper Sleep state is similar to the Deep Sleep state but further reduces core voltage levels. One of the potential lower core voltage levels is achieved by entering the base Deeper Sleep state. The Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep state. The following lower core voltage level is achieved by entering the Intel Enhanced Deeper Sleep state which is a sub-state of Deeper Sleep state. Intel Enhanced Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep only when the L2 cache has been completely shut down. Refer to Section 2.1.2.6.1 and Section 2.1.2.6.3 for further details on reducing the L2 cache and entering Intel Enhanced Deeper Sleep state.

In response to entering Deeper Sleep, the processor drives the VID code corresponding to the Deeper Sleep core voltage on the VID[6:0] pins.

Exit from Deeper Sleep or Intel Enhanced Deeper Sleep state is initiated by DPRSTP# deassertion when either core requests a core state other than C4 or either core requests a processor performance state other than the lowest operating point.

2.1.2.6.1 Intel® Enhanced Deeper Sleep State

Intel Enhanced Deeper Sleep state is a sub-state of Deeper Sleep that extends power-saving capabilities by allowing the processor to further reduce core voltage once the L2 cache has been reduced to zero ways and completely shut down. The following events occur when the processor enters Intel Enhanced Deeper Sleep state:

- The last core entering C4 issues a P_LVL4 or P_LVL5 I/O read or an MWAIT(C4) instruction and then progressively reduces the L2 cache to zero
- Once the L2 cache has been reduced to zero, the processor triggers a special chipset sequence to notify the chipset to redirect all FSB traffic, except APIC messages, to memory. The snoops are replied as misses by the chipset and are directed to main memory instead of the L2 cache. This allows for higher residency of the processor's Intel Enhanced Deeper Sleep state.
- The processor drives the VID code corresponding to the Intel Enhanced Deeper Sleep state core voltage on the VID[6:0] pins.

2.1.2.6.2 Deep Power Down State Technology (Code Named C6) State

When both cores have entered the CC6 state and the L2 cache has been shrunk down to zero ways, the processor will enter the Deep Power Down Technology state. To do so both cores save their architectural states in the on-die SRAM that resides in the V_{CCP} domain. At this point, the core V_{CC} will be dropped to the lowest core voltage closer to 0-V. The processor is now in an extremely low-power state.

In Intel Deep Power Down Technology state, the processor does not need to be snooped as all the caches are flushed before entering this state.

2.1.2.6.3 Dynamic Cache Sizing

Dynamic Cache Sizing allows the processor to flush and disable a programmable number of L2 cache ways upon each Deeper Sleep entry under the following conditions:

- The second core is already in C4 and Intel Enhanced Deeper Sleep state or Deep Power Down Technology state (C6) is enabled (as specified in Section 2.1.1.6).
- The C0 timer that tracks continuous residency in the Normal package state has not expired. This timer is cleared during the first entry into Deeper Sleep to allow consecutive Deeper Sleep entries to shrink the L2 cache as needed.
- The FSB speed to processor core speed ratio is below the predefined L2 shrink threshold.

The number of L2 cache ways disabled upon each Deeper Sleep entry is configured in the BBL_CR_CTL3 MSR. The C0 timer is referenced through the CLOCK_CORE_CST_CONTROL_STT MSR. The shrink threshold under which the L2 cache size is reduced is configured in the PMG_CST_CONFIG_CONTROL MSR. If the FSB speed to processor core speed ratio is above the predefined L2 shrink threshold, then L2 cache expansion will be requested. If the ratio is zero, then the ratio will not be taken into account for Dynamic Cache Sizing decisions.

Upon STPCLK# deassertion, the first core exiting Intel Enhanced Deeper Sleep state or Deep Power Down Technology state will expand the L2 cache to two ways and invalidate previously disabled cache ways. If the L2 cache reduction conditions stated above still exist when the last core returns to C4 and the package enters Intel Enhanced Deeper Sleep state or Deep Power Down Technology state (C6), then the L2 will be shrunk to zero again. If a core requests a processor performance state resulting in a higher ratio than the predefined L2 shrink threshold, the C0 timer expires, or the second core (not the one currently entering the interrupt routine) requests the C1, C2, or C3 states, then the whole L2 will be expanded upon the next interrupt event.

In addition, the processor supports Full Shrink on L2 cache. When the MWAIT Deep Power Down Technology state instruction is executed with a hint=0x2 in ECX[3:0], the micro code will shrink all the active ways of the L2 cache in one step. This ensures that the package enters Deep Power Down Technology immediately when both cores are in CC6 instead of iterating till the cache is reduced to zero. The operating system (OS) is expected to use this hint when it wants to enter the lowest power state and can tolerate the longer entry latency.

L2 cache shrink prevention may be enabled as needed on occasion through an MWAIT(C4) sub-state field. If shrink prevention is enabled, the processor does not enter Intel Enhanced Deeper Sleep state or Intel Deep Power Down state since the L2 cache remains valid and in full size.

2.2 Enhanced Intel SpeedStep® Technology

The processor features Enhanced Intel SpeedStep Technology. Following are the key features of Enhanced Intel SpeedStep Technology:

- Multiple voltage and frequency operating points provide optimal performance at the lowest power.
- Voltage and frequency selection is software-controlled by writing to processor MSRs:
  - If the target frequency is higher than the current frequency, V_{CC} is ramped up in steps by placing new values on the VID pins, and the PLL then locks to the new frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the new frequency and the V_{CC} is changed through the VID pin mechanism.
  - Software transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition completes.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Low transition latency and large number of transitions possible per second:
  - Processor core (including L2 cache) is unavailable for up to 10 μs during the frequency transition.
  - The bus protocol (BNR# mechanism) is used to block snooping.
- Improved Intel® Thermal Monitor mode:
  - When the on-die thermal sensor indicates that the die temperature is too high the processor can automatically perform a transition to a lower frequency and voltage specified in a software-programmable MSR.
  - The processor waits for a fixed time period. If the die temperature is down to acceptable levels, an up-transition to the previous frequency and voltage point occurs.
  - An interrupt is generated for the up and down Intel Thermal Monitor transitions enabling better system-level thermal management.
- Enhanced thermal management features:
  - Digital Thermal Sensor and Out of Specification detection.
  - Intel Thermal Monitor 1 (TM1) in addition to Intel Thermal Monitor 2 (TM2) in case of unsuccessful TM2 transition.
  - Dual-core thermal management synchronization.

Each core in the dual-core processor implements an independent MSR for controlling Enhanced Intel SpeedStep Technology, but both cores must operate at the same frequency and voltage. The processor has performance state coordination logic to resolve frequency and voltage requests from the two cores into a single frequency and voltage request for the package as a whole. If both cores request the same frequency and voltage, then the processor will transition to the requested common frequency and voltage. If the two cores have different frequency and voltage requests, then the processor will take the highest of the two frequencies and voltages as the resolved request and transition to that frequency and voltage.

The processor also supports Dynamic FSB Frequency Switching and Intel Dynamic Acceleration Technology mode on select SKUs. The operating system can take advantage of these features and request a lower operating point called SuperLFM (due to Dynamic FSB Frequency Switching) and a higher operating point Intel Dynamic Acceleration Technology mode.

2.3 Extended Low-Power States

Extended low-power states (CXE) optimize for power by forcibly reducing the performance state of the processor when it enters a package low-power state. Instead of directly transitioning into the package low-power state, the enhanced package low-power state first reduces the performance state of the processor by performing an Enhanced Intel SpeedStep Technology transition down to the lowest operating point. Upon receiving a break event from the package low-power state, control will be returned to software while an Enhanced Intel SpeedStep Technology transition up to the initial operating point occurs. The advantage of this feature is that it significantly reduces leakage while in the Stop-Grant and Deeper Sleep states.

Deep Power Down Technology is always enabled in the extended low power state as described above.

Note: Long-term reliability cannot be assured unless all the Extended Low Power States are enabled.

The processor implements two software interfaces for requesting enhanced package low-power states: MWAIT instruction extensions with sub-state hints and via BIOS by configuring IA32_MISC_ENABLES MSR bits to automatically promote package low-power states to enhanced package low-power states.

Caution: **Extended Stop-Grant and Enhanced Deeper Sleep must be enabled via the BIOS for the processor to remain within specification.** As processor technology changes, enabling the extended low power states becomes increasingly crucial when building computer systems. Maintaining the proper BIOS configuration is key to reliable, long-term system operation. Not complying to this guideline may affect the long-term reliability of the processor.

Caution: **Enhanced Intel SpeedStep Technology transitions are multistep processes that require clocked control.** These transitions cannot occur when the processor is in the Sleep or Deep Sleep package low-power states since processor clocks are not active in these states. Extended Deeper Sleep is an exception to this rule when the Hard C4E configuration is enabled in the IA32_MISC_ENABLES MSR. This Extended Deeper Sleep state configuration will lower core voltage to the Deeper Sleep level while in Deeper Sleep and, upon exit, will automatically transition to the lowest operating voltage and frequency to reduce snoop service latency. The transition to the lowest operating point or back to the original software-requested point may not be instantaneous. Furthermore, upon very frequent transitions between active and idle states, the transitions may lag behind the idle state entry resulting in the processor either executing for a longer time at the lowest operating point or running idle at a high operating point. Observations and analyses show this behavior should not significantly impact total power savings or performance score while providing power benefits in most other cases.

2.4 FSB Low Power Enhancements

The processor incorporates FSB low power enhancements:

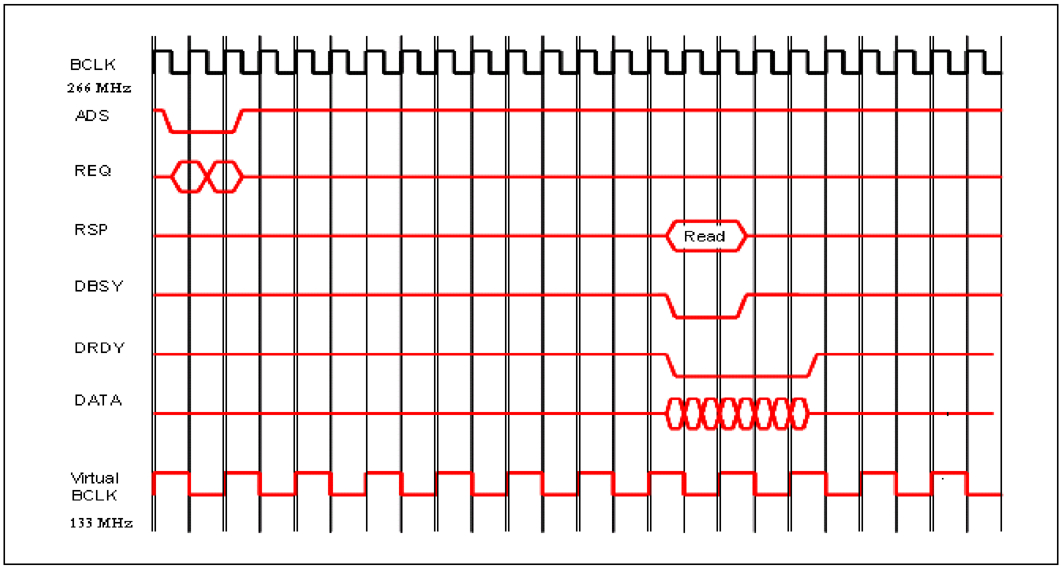
- Dynamic FSB Power Down
- BPRI# control for address and control input buffers
- Dynamic Bus Parking
- Dynamic On-Die Termination disabling
- Low V_{CCP} (I/O termination voltage)
- Dynamic FSB frequency switching

The processor incorporates the DPWR# signal that controls the data bus input buffers on the processor. The DPWR# signal disables the buffers when not used and activates them only when data bus activity occurs, resulting in significant power savings with no performance impact. BPRI# control also allows the processor address and control input buffers to be turned off when the BPRI# signal is inactive. Dynamic Bus Parking allows a reciprocal power reduction in GMCH address and control input buffers when the processor deasserts its BR0# pin. The On-Die Termination on the processor FSB buffers is disabled when the signals are driven low, resulting in additional power savings. The low I/O termination voltage is on a dedicated voltage plane independent of the core voltage, enabling low I/O switching power at all times.

2.4.1 Dynamic FSB Frequency Switching

Dynamic FSB frequency switching effectively reduces the internal bus clock frequency in half to further decrease the minimum processor operating frequency from the Enhanced Intel SpeedStep Technology performance states and achieve the Super Low Frequency Mode (Super LFM). This feature is supported at FSB frequencies of 1066 MHz, 800 MHz and 667 MHz and does not entail a change in the external bus signal (BCLK) frequency. Instead, both the processor and GMCH internally lower their BCLK reference frequency to 50% of the externally visible frequency. Both the processor and GMCH maintain a virtual BCLK signal (VBCLK) that is aligned to the external BCLK but at half the frequency. After a downward shift, it would appear externally as if the bus is running with a 133-MHz base clock in all aspects, except that the actual external BCLK remains at 266 MHz. See Figure 3 for details. The transition into Super LFM, a "down-shift," is done following a handshake between the processor and GMCH. A similar handshake is used to indicate an "up-shift," a change back to normal operating mode. Please ensure this feature is enabled and supported in the BIOS.

Figure 3. Dynamic FSB Frequency Switching Protocol



NOTES:
1. All common clock signals will be active for two BCLKs instead of one (e.g., ADS#, HIT#).
2. The double-pumped signal strobes will have only one transition per BCLK when active, instead of two.
3. The quad-pumped signal strobes will have only two transitions per BCLK when active, instead of four.
4. Same setup and hold times apply, but relative to every second rising BCLK.
5. Following a RESET#, the bus will be in the legacy full-frequency mode.
6. There will not be a down-shift right after RESET# deassertion.
7. There is no backing out of a transition into or out of half-frequency mode. Once the sequence starts it must be completed.

2.4.2 Enhanced Intel® Dynamic Acceleration Technology

The processor supports Intel Dynamic Acceleration Technology mode. The Intel Dynamic Acceleration Technology feature allows one core of the processor to operate at a higher frequency point when the other core is inactive and the operating system requests increased performance. This higher frequency is called the opportunistic frequency and the maximum rated operating frequency is the ensured frequency.

The processor includes a hysteresis mechanism that improves overall Intel Dynamic Acceleration Technology performance by decreasing unnecessary transitions of the cores in and out of Intel Dynamic Acceleration Technology mode. Normally, the processor would exit Intel Dynamic Acceleration Technology as soon as two cores are active. This can become an issue if the idle core is frequently awakened for a short periods (i.e., high timer tick rates). The hysteresis mechanism allows two cores to be active for a limited time before it transitions out of Intel Dynamic Acceleration Technology mode.

Intel Dynamic Acceleration Technology mode enabling requires:

- Exposure, via BIOS, of the opportunistic frequency as the highest ACPI P state
- Enhanced Multi-Threaded Thermal Management (EMTTM)
- Intel Dynamic Acceleration Technology mode and EMTTM MSR configuration via BIOS.

When in Intel Dynamic Acceleration Technology mode, it is possible for both cores to be active under certain internal conditions. In such a scenario the processor may draw a Instantaneous current ($I_{CC\_CORE\_INST}$) for a short duration of t_{INST}; however, the average I_{CC} current will be lesser than or equal to I_{CCDES} current specification. Please refer to the Processor DC Specifications section for more details.

2.5 VID-x

The processor implements the VID-x feature for improved control of core voltage levels when the processor enters a reduced power consumption state. VID-x applies only when the processor is in the Intel Dynamic Acceleration Technology performance state and one or more cores are in low-power state (i.e., CC3/CC4/CC6). VID-x provides the ability for the processor to request core voltage level reductions greater than one VID tick. The amount of VID tick reduction is fixed and only occurs while the processor is in Intel Dynamic Acceleration Technology mode. This improved voltage regulator efficiency during periods of reduced power consumption allows for leakage current reduction which results in platform power savings and extended battery life.

When in Intel Dynamic Acceleration Technology mode, it is possible for both cores to be active under certain internal conditions. In such a scenario the processor may draw a Instantaneous current ($I_{CC\_CORE\_INST}$) for a short duration of t_{INST}; however, the average I_{CC} current will be lesser than or equal to I_{CCDES} current specification. Please refer to the Processor DC Specifications section for more details.

2.6 Processor Power Status Indicator (PSI-2) Signal

The processor incorporates the PSI# signal that is asserted when the processor is in a reduced power consumption state. PSI# can be used to improve intermediate and light load efficiency of the voltage regulator, resulting in platform power savings and extended battery life. The algorithm that the processor uses for determining when to assert PSI# is different from the algorithm used in previous mobile processors. PSI-2 functionality is expanded further to support three processor states:

- Both cores are in idle state
- Only one core active state
- Both cores are in active state

PSI-2 functionality improves overall voltage regulator efficiency over a wide power range based on the C-state and P-state of the two cores. The combined C-state and P-state of both cores are used to dynamically predict processor power.

The real-time power prediction is compared against a set of predefined and configured values of **CHH** and **CHL**. **CHH** is indicative of the active C-state of both the cores and **CHL** is indicative that only one core is in active C-state and the other core is in low power core state. PSI-2# output is asserted upon crossing these thresholds indicating that the processor requires lower power. The voltage regulator will adapt its power output accordingly. Additionally the voltage regulator may switch to a single phase and/or asynchronous mode when the processor is idle and fused leakage limit is less than or equal to the BIOS threshold value.

§

3 Electrical Specifications

3.1 Power and Ground Pins

For clean, on-chip power distribution, the processor will have a large number of V_{CC} (power) and V_{SS} (ground) inputs. All power pins must be connected to V_{CC} power planes while all V_{SS} pins must be connected to system ground planes. Use of multiple power and ground planes is recommended to reduce I*R drop. The processor V_{CC} pins must be supplied the voltage determined by the VID (Voltage ID) pins.

3.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Larger bulk storage, such as electrolytic capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in the tables in Section 3.10. Failure to do so can result in timing violations or reduced lifetime of the component.

3.2.1 V_{CC} Decoupling

V_{CC} regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep a low interconnect resistance from the regulator to the socket. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low-power states, should be provided by the voltage regulator solution depending on the specific system design.

3.2.2 FSB AGTL+ Decoupling

The processors integrate signal termination on the die as well as incorporate high frequency decoupling capacitance on the processor package. Decoupling must also be provided by the system motherboard for proper AGTL+ bus operation.

3.2.3 FSB Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous-generation processors, the processor core frequency is a multiple of the BCLK[1:0] frequency. The processor bus ratio multiplier will be set at its default ratio at manufacturing. The processor uses a differential clocking implementation.

3.3 Voltage Identification and Power Sequencing

The processor uses seven voltage identification pins,VID[6:0], to support automatic selection of power supply voltages. The VID pins for the processor are CMOS outputs driven by the processor VID circuitry. Table 2 specifies the voltage level corresponding to the state of VID[6:0]. A 1 in the table refers to a high-voltage level and a 0 refers to a low-voltage level.

Table 2. Voltage Identification Definition (Sheet 1 of 3)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125

Table 2. Voltage Identification Definition (Sheet 2 of 3)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250

Table 2. Voltage Identification Definition (Sheet 3 of 3)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000

3.4 Catastrophic Thermal Protection

The processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of approximately 125°C (maximum), or if the THERMTRIP# signal is asserted, the V_{CC} supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway of the processor. THERMTRIP# functionality is not ensured if the PWRGOOD signal is not asserted, and during Deep Power Down Technology State (C6).

3.5 Reserved and Unused Pins

All RESERVED (RSVD) pins must remain unconnected. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Section 4.2 for a pin listing of the processor and the location of all RSVD pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active low AGTL+ inputs may be left as no-connects if AGTL+ termination is provided on the processor silicon. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected. The TEST1,TEST2,TEST3,TEST4,TEST5,TEST6,TEST7 pins are used for test purposes internally and can be left as “No Connects”.

3.6 FSB Frequency Select Signals (BSEL[2:0])

The BSEL[2:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). These signals should be connected to the clock chip and the appropriate chipset on the platform. The BSEL encoding for BCLK[1:0] is shown in Table 3.

Table 3. BSEL[2:0] Encoding for BCLK Frequency

BSEL[2]	BSEL[1]	BSEL[0]	BCLK Frequency
L	L	L	266 MHz
L	L	H	RESERVED
L	H	H	RESERVED
L	H	L	200 MHz
H	H	L	RESERVED
H	H	H	RESERVED
H	L	H	RESERVED
H	L	L	RESERVED

3.7 FSB Signal Groups

The FSB signals have been combined into groups by buffer type in the following sections. In this document, the term "AGTL+ Input" refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, "AGTL+ Output" refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source-synchronous data bus, two sets of timing parameters are specified. One set is for common clock signals, which are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.), and the second set is for the source-synchronous signals which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 4 identifies which signals are common clock, source synchronous, and asynchronous.

Table 4. FSB Pin Groups

<table>
<tr><th>Signal Group</th><th>Type</th><th>Signals[1]</th></tr>
<tr><td>AGTL+ Common Clock Input</td><td>Synchronous to BCLK[1:0]</td><td>BPRI#, DEFER#, PREQ#[5], RESET#, RS[2:0]#, TRDY#</td></tr>
<tr><td>AGTL+ Common Clock I/O</td><td>Synchronous to BCLK[1:0]</td><td>ADS#, BNR#, BPM[3:0]#[3], BR0#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, PRDY#[3], DPWR#</td></tr>
<tr><td>AGTL+ Source Synchronous I/O</td><td>Synchronous to assoc. strobe</td><td><table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB[0]#</td></tr>
<tr><td>A[35:17]#</td><td>ADSTB[1]#</td></tr>
<tr><td>D[15:0]#, DINV0#</td><td>DSTBP0#, DSTBN0#</td></tr>
<tr><td>D[31:16]#, DINV1#</td><td>DSTBP1#, DSTBN1#</td></tr>
<tr><td>D[47:32]#, DINV2#</td><td>DSTBP2#, DSTBN2#</td></tr>
<tr><td>D[63:48]#, DINV3#</td><td>DSTBP3#, DSTBN3#</td></tr>
</table></td></tr>
<tr><td>AGTL+ Strobes</td><td>Synchronous to BCLK[1:0]</td><td>ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#</td></tr>
<tr><td>CMOS Input</td><td>Asynchronous</td><td>A20M#, DPRSTP#, DPSLP#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, STPCLK#</td></tr>
<tr><td>Open Drain Output</td><td>Asynchronous</td><td>FERR#, IERR#, THERMTRIP#</td></tr>
<tr><td>Open Drain I/O</td><td>Asynchronous</td><td>PROCHOT#[4]</td></tr>
<tr><td>CMOS Output</td><td>Asynchronous</td><td>PSI#, VID[6:0], BSEL[2:0]</td></tr>
<tr><td>CMOS Input</td><td>Synchronous to TCK</td><td>TCK, TDI, TMS, TRST#</td></tr>
<tr><td>Open Drain Output</td><td>Synchronous to TCK</td><td>TDO</td></tr>
<tr><td>FSB Clock</td><td>Clock</td><td>BCLK[1:0]</td></tr>
<tr><td>Power/Other</td><td></td><td>COMP[3:0], DBR#[2], GTLREF, RSVD, TEST2, TEST1, THERMDA, THERMDC, V_{CC}, V_{CCA}, V_{CCP}, V_{CC_SENSE}, V_{SS}, V_{SS_SENSE}</td></tr>
</table>

NOTES: See next page

1. Refer to Chapter 4 for signal descriptions and termination requirements.
2. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
3. BPM[2:1]# and PRDY# are AGTL+ output-only signals.
4. PROCHOT# signal type is open drain output and CMOS input.
5. On-die termination differs from other AGTL+ signals.

3.8 CMOS Signals

CMOS input signals are shown in Table 4. Legacy output FERR#, IERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) use Open Drain output buffers. These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the CMOS signals are required to be asserted for more than four BCLKs for the processor to recognize them. See Section 3.10 for the DC specifications for the CMOS signal groups.

3.9 Maximum Ratings

Table 5 specifies absolute maximum and minimum ratings only, which lie outside the functional limits of the processor. Only within specified operation limits, can functionality and long-term reliability be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded.

Caution: Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 5. Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes[1,2]
$T_{STORAGE}$	Processor Storage Temperature	-40	85	°C	3,4,5
$T_{STORAGE}$	Processor Storage Temperature	-25		°C	6
V_{CC}	Any Processor Supply Voltage with Respect to V_{SS}	-0.3	1.45	V	
$V_{inAGTL+}$	AGTL+ Buffer DC Input Voltage with Respect to V_{SS}	-0.1	1.45	V	
$V_{inAsynch\_CMOS}$	CMOS Buffer DC Input Voltage with Respect to V_{SS}	-0.1	1.45	V	

NOTES:
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.

2. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
4. This rating applies to the processor and does not include any tray or packaging.
5. Failure to adhere to this specification can affect the long-term reliability of the processor.
6. For Intel® Core™2 Duo mobile processors in 22x22 mm package.

3.10 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise.

The tables list the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. The Highest Frequency Mode (HFM) and Lowest Frequency Mode (LFM) refer to the highest and lowest core operating frequencies supported on the processor. Active mode load line specifications apply in all states except in the Deep Sleep and Deeper Sleep states. $V_{CC,BOOT}$ is the default voltage driven by the voltage regulator at power up in order to set the VID values. Unless specified otherwise, all specifications for the processor are at T_J = 105 °C. Read all notes associated with each parameter.

Table 6. Voltage and Current Specifications for the Dual-Core, Extreme Edition Processors (Sheet 1 of 2)

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CCDAM}	V_{CC} in Enhanced Intel® Dynamic Acceleration Technology Mode		1.0		1.325	V	1, 2
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)		1.0	—	1.275	V	1, 2
V_{CCLFM}	V_{CC} at Lowest Frequency Mode (LFM)		0.85	—	1.1	V	1, 2
V_{CCSLFM}	V_{CC} at Super Low Frequency Mode (Super LFM)		0.8	—	1.0	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up		—	1.20		V	2, 6
V_{CCP}	AGTL+ Termination Voltage		1.00	1.05	1.10	V	
V_{CCA}	PLL Supply Voltage		1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep		0.65	—	0.85	V	1, 2
V_{DC4}	V_{CC} at Intel® Enhanced Deeper Sleep State		0.6	—	0.85	V	1, 2
$V_{CCDPPWDN}$	V_{CC} at Deep Power Down Technology State (C6)		0.35	—	0.7	V	
I_{CCDES}	I_{CC} for Processors Recommended Design Target		—	—	60	A	12
I_{CC}	I_{CC} for Processors		—	—	—		
	Processor Number	Core Frequency/Voltage	—	—	—		
	X9100	3.06 GHz & V_{CCHFM} 1.6 GHz & V_{CCLFM} 0.8 GHz & V_{CCSLFM}	—	—	59 34 24	A	3, 4, 10

Table 6. Voltage and Current Specifications for the Dual-Core, Extreme Edition Processors (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant HFM SuperLFM	—	—	29.7 16.7	A	3, 4, 10
I_{SLP}	I_{CC} Sleep HFM SuperLFM	—	—	28.8 16.5	A	3, 4, 10
I_{DSLP}	I_{CC} Deep Sleep HFM SuperLFM	—	—	26.8 16.0	A	3, 4, 10
I_{DPRSLP}	I_{CC} Deeper Sleep (C4)	—	—	12.2	A	3, 4
I_{DC4}	I_{CC} Intel Enhanced Deeper Sleep State	—	—	11.7	A	3, 4
I_{PPWDN}	I_{CC} Deep Power Down Technology State (C6)	—	—	11.0	A	3, 4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin	—	—	600	mA/µs	5, 7
I_{CCA}	I_{CC} for V_{CCA} Supply	—	—	130	mA	
I_{CCP}	I_{CC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP} Supply after V_{CC} Stable	—	—	4.5 2.5	A A	8 9

NOTES:
1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or Enhanced Halt State).
2. The voltage specifications are assumed to be measured across V_{CC_SENSE} and V_{SS_SENSE} pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 105 °C T_J.
4. Specified at the nominal V_{CC}.
5. Measured at the bulk capacitors on the motherboard.
6. $V_{CC,BOOT}$ tolerance shown in Figure 4 and Figure 5.
7. Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal V_{CC}. Not 100% tested.
8. This is a power-up peak current specification, which is applicable when V_{CCP} is high and V_{CC_CORE} is low.
9. This is a steady-state I_{CC} current specification, which is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. The maximum delta between Intel Enhanced Deeper Sleep and LFM on the processor will be lesser than or equal to 300 mV.
11. The I_{CCDES} (max) specification of 60 A is for Intel® Core™2 Extreme processors only.

Table 7. Voltage and Current Specifications for the Dual-Core, Standard-Voltage Processors

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CCDAM}	V_{CC} in Enhanced Intel® Dynamic Acceleration Technology Mode	1.0		1.3	V	1, 2
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)	1.0		1.25	V	1, 2
V_{CCLFM}	V_{CC} at Lowest Frequency Mode (LFM)	0.85	—	1.1	V	1, 2
V_{CCSLFM}	V_{CC} at Super Low Frequency Mode (Super LFM)	0.75	—	0.95	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up	—	1.2	—	V	2, 6
V_{CCP}	AGTL+ Termination Voltage	1.0	1.05	1.1	V	
V_{CCA}	PLL Supply Voltage	1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep	0.65	—	0.85	V	1, 2
V_{DC4}	V_{CC} at Intel® Enhanced Deeper Sleep State	0.6	—	0.85	V	1, 2
$V_{CCDPPWDN}$	V_{CC} at Deep Power Down Technology State (C6)	0.35	—	0.7	V	1, 2
I_{CCDES}	I_{CC} for Processors Recommended Design Target	—	—	47	A	12
I_{CC}	I_{CC} for Processors	—	—	—		
	Processor Number | Core Frequency/Voltage	—	—	—		
	T9900 | 3.06 GHz & V_{CCHFM} T9800 | 2.93 GHz & V_{CCHFM} T9600 | 2.80 GHz & V_{CCHFM} T9550 | 2.66 GHz & V_{CCHFM} T9400 | 2.53 GHz & V_{CCHFM} 1.6 GHz & V_{CCLFM} 0.8 GHz & V_{CCSLFM}	—	—	47 47 47 47 47 31.4 22.4	A	3, 4, 10
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant HFM SuperLFM	—	—	 25.4 13.7	A	3, 4, 10
I_{SLP}	I_{CC} Sleep HFM SuperLFM	—	—	 24.7 13.5	A	3, 4, 10
I_{DSLP}	I_{CC} Deep Sleep HFM SuperLFM	—	—	 22.9 13.0	A	3, 4, 10
I_{DPRSLP}	I_{CC} Deeper Sleep (C4)	—	—	11.7	A	3, 4
I_{DC4}	I_{CC} Intel Enhanced Deeper Sleep	—	—	10.5	A	3, 4
I_{PPWDN}	I_{CC} Deep Power Down Technology State (C6)	—	—	5.7	A	3, 4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin	—	—	600	mA/µs	5, 7
I_{CCA}	I_{CC} for V_{CCA} Supply	—	—	130	mA	
I_{CCP}	I_{CCC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP} Supply after V_{CC} Stable	—	—	4.5 2.5	A A	8 9

NOTES: See next page.

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or Enhanced Halt State).
2. The voltage specifications are assumed to be measured across V_{CC_SENSE} and V_{SS_SENSE} pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 105 °C T_J.
4. Specified at the nominal V_{CC}.
5. Measured at the bulk capacitors on the motherboard.
6. $V_{CC,BOOT}$ tolerance shown in Figure 7 and Figure 8.
7. Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal V_{CC}. Not 100% tested.
8. This is a power-up peak current specification that is applicable when V_{CCP} is high and V_{CC_CORE} is low.
9. This is a steady-state I_{CC}current specification that is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. Processor I_{CC} requirements in Intel Dynamic Acceleration Technology mode are lesser than I_{CC} in HFM
11. The maximum delta between Intel Enhanced Deeper Sleep and LFM on the processor will be lesser than or equal to 300 mV.
12. Instantaneous current $I_{CC\_CORE\_INST}$ of 57 A has to be sustained for short time (t_{INST}) of 35 µs. Average current will be less than maximum specified I_{CCDES}. VR OCP threshold should be high enough to support current levels described herein.

Table 8. Voltage and Current Specifications for the Dual-Core, Low-Power Standard-Voltage Processors (25 W) in Standard Package

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CCDAM}	V_{CC} in Enhanced Intel® Dynamic Acceleration Technology Mode		0.9		1.3	V	1, 2
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)		0.9		1.25	V	1, 2
V_{CCLFM}	V_{CC} at Lowest Frequency Mode (LFM)		0.85	—	1.025	V	1, 2
V_{CCSLFM}	V_{CC} at Super Low Frequency Mode (Super LFM)		0.75	—	0.95	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up		—	1.2	—	V	2, 6
V_{CCP}	AGTL+ Termination Voltage		1.0	1.05	1.1	V	
V_{CCA}	PLL Supply Voltage		1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep		0.65	—	0.85	V	1, 2
V_{DC4}	V_{CC} at Intel® Enhanced Deeper Sleep State		0.6	—	0.85	V	1, 2
$V_{CCDPPWDN}$	V_{CC} at Deep Power Down Technology State (C6)		0.35	—	0.7	V	1, 2
I_{CCDES}	I_{CC} for Processors Recommended Design Target		—	—	38	A	12
I_{CC}	I_{CC} for Processors		—	—	—		
	Processor Number	Core Frequency/Voltage	—	—	—		
	P9700 P9600 P8800 P9500 P8700 P8600 P8400	2.8 GHz & V_{CCHFM} 2.667 GHz & V_{CCHFM} 2.667 GHz & V_{CCHFM} 2.53 GHz & V_{CCHFM} 2.53 GHz & V_{CCHFM} 2.4 GHz & V_{CCHFM} 2.267 GHz & V_{CCHFM} 1.6 GHz & V_{CCLFM} 0.8 GHz & V_{CCSLFM}	—	—	38 38 38 38 38 38 38 27.7 17.5	A	3, 4, 10

Table 8. Voltage and Current Specifications for the Dual-Core, Low-Power Standard-Voltage Processors (25 W) in Standard Package

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant HFM SuperLFM	—	—	15.3 10.5	A	3, 4, 10
I_{SLP}	I_{CC} Sleep HFM SuperLFM	—	—	14.6 10.3	A	3, 4, 10
I_{DSLP}	I_{CC} Deep Sleep HFM SuperLFM	—	—	12.9 9.8	A	3, 4, 10
I_{DPRSLP}	I_{CC} Deeper Sleep	—	—	7.3	A	3, 4
I_{DC4}	I_{CC} Intel Enhanced Deeper Sleep	—	—	6.7	A	3, 4
I_{PPWDN}	I_{CC} Deep Power Down Technology State (C6)	—	—	4.3	A	3, 4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin	—	—	600	mA/µs	5, 7
I_{CCA}	I_{CC} for V_{CCA} Supply	—	—	130	mA	
I_{CCP}	I_{CCC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP} Supply after V_{CC} Stable	—	—	4.5 2.5	A A	8 9

NOTES:.

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or Enhanced Halt State).
2. The voltage specifications are assumed to be measured across V_{CC_SENSE} and V_{SS_SENSE} pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 105 °C T_J.
4. Specified at the nominal V_{CC}.
5. Measured at the bulk capacitors on the motherboard.
6. $V_{CC,BOOT}$ tolerance shown in Figure 4 and Figure 5.
7. Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal V_{CC}. Not 100% tested.
8. This is a power-up peak current specification that is applicable when V_{CCP} is high and V_{CC_CORE} is low.
9. This is a steady-state I_{CC}current specification that is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. Processor I_{CC} requirements in Intel Dynamic Acceleration Technology mode are lesser than I_{CC} in HFM
11. The maximum delta between Intel Enhanced Deeper Sleep and LFM on the processor will be lesser than or equal to 300 mV.
12. Instantaneous current $I_{CC\_CORE\_INST}$ of 49 A has to be sustained for short time (t_{INST}) of 35 µs. Average current will be less than maximum specified I_{CCDES}. VR OCP threshold should be high enough to support current levels described herein.

Table 9. Voltage and Current Specifications for the Dual-Core, Power Optimized Performance (25 W) SFF Processors

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CCDAM}	V_{CC} in Enhanced Intel® Dynamic Acceleration Technology Mode		0.9	—	1.275	V	1, 2
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)		0.9	—	1.2125	V	1, 2
V_{CCLFM}	V_{CC} at Lowest Frequency Mode (LFM)		0.85	—	1.025	V	1, 2
V_{CCSLFM}	V_{CC} at Super Low Frequency Mode (Super LFM)		0.75	—	0.95	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up		—	1.20	—	V	2, 6, 8
V_{CCP}	AGTL+ Termination Voltage		1.00	1.05	1.10	V	
V_{CCA}	PLL Supply Voltage		1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep		0.65	—	0.85	V	1, 2
V_{DC4}	V_{CC} at Intel® Enhanced Deeper Sleep State		0.6	—	0.85	V	1, 2
$V_{CCDPPWDN}$	V_{CC} at Deep Power Down Technology State (C6)		0.35	—	0.7	V	1, 2
I_{CCDES}	I_{CC} for Processors Recommended Design Target		—	—	37	A	5
I_{CC}	Processor Number	Core Frequency/Voltage	—	—	—		
	SP9600 SP9400 SP9300	2.53 GHz & V_{CCHFM} 2.4 GHz & V_{CCHFM} 2.26 GHz & V_{CCHFM} 1.2 GHz & V_{CCLFM} 0.8 GHz & V_{CCSLFM}	—	—	37 37 37 28 17	A	3, 4, 12
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant HFM SuperLFM		—	—	14.8 8.8	A	3, 4, 12
I_{SLP}	I_{CC} Sleep HFM SuperLFM		—	—	14.2 8.6	A	3, 4, 12
I_{DSLP}	I_{CC} Deep Sleep HFM SuperLFM		—	—	12.5 8.1	A	3, 4, 12
I_{DPRSLP}	I_{CC} Deeper Sleep		—	—	6.9	A	3, 4
I_{DC4}	I_{CC} Intel Enhanced Deeper Sleep State		—	—	5.9	A	3, 4
I_{DPWDN}	I_{CC} Deep Power Down Technology State (C6)		—	—	3.5	A	3, 4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin		—	—	600	mA/µs	7, 9
I_{CCA}	I_{CC} for V_{CCA} Supply		—	—	130	mA	
I_{CCP}	I_{CC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP}Supply after V_{CC} Stable		—	—	4.5 2.5	A A	10 11

NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note

that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or Enhanced Halt State).

2. The voltage specifications are assumed to be measured across V_{CC_SENSE} and V_{SS_SENSE} pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 105 °C T_J.
4. Specified at the nominal V_{CC}.
5. Measured at the bulk capacitors on the motherboard.
6. $V_{CC,BOOT}$ tolerance shown in Figure 7 and Figure 8.
7. Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal V_{CC}. Not 100% tested.
8. This is a power-up peak current specification that is applicable when V_{CCP} is high and V_{CC_CORE} is low.
9. This is a steady-state I_{CC} current specification that is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. Processor I_{CC} requirements in Intel Dynamic Acceleration Technology mode are lesser than I_{CC} in HFM
11. The maximum delta between Intel Enhanced Deeper Sleep and LFM on the processor will be lesser than or equal to 300 mV.
12. Instantaneous current $I_{CC\_CORE\_INST}$ of 44 A has to be sustained for short time (t_{INST}) of 35 µs. Average current will be less than maximum specified I_{CCDES}. VR OCP threshold should be high enough to support current levels described herein.

Table 10. Voltage and Current Specifications for the Dual-Core, Low-Voltage SFF Processor

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CCDAM}	V_{CC} in Enhanced Intel® Dynamic Acceleration Technology Mode		0.9	—	1.25	V	1, 2
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)		0.9	—	1.175	V	1, 2
V_{CCLFM}	V_{CC} at Lowest Frequency Mode (LFM)		0.85	—	1.025	V	1, 2
V_{CCSLFM}	V_{CC} at Super Low Frequency Mode (Super LFM)		0.75	—	0.95	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up		—	1.20	—	V	2, 6, 8
V_{CCP}	AGTL+ Termination Voltage		1.00	1.05	1.10	V	
V_{CCA}	PLL Supply Voltage		1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep		0.65	—	0.85	V	1, 2
V_{DC4}	V_{CC} at Intel® Enhanced Deeper Sleep State		0.6	—	0.85	V	1, 2
$V_{CCDPPWDN}$	V_{CC} at Deep Power Down Technology State (C6)		0.35	—	0.7	V	1, 2
I_{CCDES}	I_{CC} for Processors Recommended Design Target		—	—	27	A	5
I_{CC}	Processor Number	Core Frequency/Voltage	—	—	—		
	SL9600 SL9400 SL9300	2.13 GHz & V_{CCHFM} 1.86 GHz & V_{CCHFM} 1.6 GHz & V_{CCHFM} 1.6 GHz & V_{CCLFM} 0.8 GHz & V_{CCSLFM}	—	—	27 27 27 25.5 15	A	3, 4, 12
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant HFM SuperLFM		—	—	12.3 8.2	A	3, 4, 12
I_{SLP}	I_{CC} Sleep HFM SuperLFM		—	—	11.8 8.0	A	3, 4, 12

Table 10. Voltage and Current Specifications for the Dual-Core, Low-Voltage SFF Processor

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{DSLP}	I_{CC} Deep Sleep HFM SuperLFM	—	—	10.5 7.5	A	3, 4, 12
I_{DPRSLP}	I_{CC} Deeper Sleep	—	—	6.5	A	3, 4
I_{DC4}	I_{CC} Intel Enhanced Deeper Sleep	—	—	5.6	A	3, 4
I_{DPWDN}	I_{CC} Deep Power Down Technology State (C6)	—	—	3.2	A	3, 4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin	—	—	600	mA/µs	7, 9
I_{CCA}	I_{CC} for V_{CCA} Supply	—	—	130	mA	
I_{CCP}	I_{CC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP} Supply after V_{CC} Stable	—	—	4.5 2.5	A A	10 11

NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or Enhanced Halt State).
2. The voltage specifications are assumed to be measured across V_{CC_SENSE} and V_{SS_SENSE} pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 105 °C T_J.
4. Specified at the nominal V_{CC}.
5. Measured at the bulk capacitors on the motherboard.
6. $V_{CC,BOOT}$ tolerance shown in Figure 7 and Figure 8.
7. Based on simulations and averaged over the duration of any change in current. Specified by design/ characterization at nominal V_{CC}. Not 100% tested.
8. This is a power-up peak current specification that is applicable when V_{CCP} is high and V_{CC_CORE} is low.
9. This is a steady-state I_{CC} current specification that is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. Processor I_{CC} requirements in Intel Dynamic Acceleration Technology mode are lesser than I_{CC} in HFM
11. The maximum delta between Intel Enhanced Deeper Sleep and LFM on the processor will be lesser than or equal to 300 mV.
12. Instantaneous current $I_{CC\_CORE\_INST}$ of 36 A has to be sustained for short time (t_{INST}) of 35 µs. Average current will be less than maximum specified I_{CCDES}. VR OCP threshold should be high enough to support current levels described herein.

Table 11. Voltage and Current Specifications for the Dual-Core, Ultra-Low-Voltage SFF Processor

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CCDAM}	V_{CC} in Enhanced Intel® Dynamic Acceleration Technology Mode		0.8	—	1.1625	V	1, 2
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)		0.775	—	1.1	V	1, 2
V_{CCLFM}	V_{CC} at Lowest Frequency Mode (LFM)		0.8	—	0.975	V	1, 2
V_{CCSLFM}	V_{CC} at Super Low Frequency Mode (Super LFM)		0.725	—	0.925	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up		—	1.20	—	V	2, 6, 8
V_{CCP}	AGTL+ Termination Voltage		1.00	1.05	1.10	V	
V_{CCA}	PLL Supply Voltage		1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep		0.65	—	0.8	V	1, 2
V_{DC4}	V_{CC} at Intel® Enhanced Deeper Sleep State		0.6	—	0.8	V	1, 2
$V_{CCDPPWDN}$	V_{CC} at Deep Power Down Technology State (C6)		0.35	—	0.6	V	1, 2
I_{CCDES}	I_{CC} for Processors Recommended Design Target		—	—	18	A	5
I_{CC}	Processor Number	Core Frequency/Voltage	—	—	—		
	SU9600 SU9400 SU9300	1.6 GHz & V_{CCHFM} 1.4 GHz & V_{CCHFM} 1.2 GHz & V_{CCHFM} 1.2 GHz & V_{CCLFM} 0.8 GHz & V_{CCSLFM}	—	—	18 18 18 18 13	A	3, 4, 12
$I_{AH,}$ I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant HFM SuperLFM		—	—	6.3 4.4	A	3, 4, 12
I_{SLP}	I_{CC} Sleep HFM SuperLFM		—	—	5.9 4.2	A	3, 4, 12
I_{DSLP}	I_{CC} Deep Sleep HFM SuperLFM		—	—	5.0 3.7	A	3, 4, 12
I_{DPRSLP}	I_{CC} Deeper Sleep		—	—	3.2	A	3, 4
I_{DC4}	I_{CC} Intel Enhanced Deeper Sleep State		—	—	2.8	A	3, 4
I_{DPWDN}	I_{CC} Deep Power Down Technology State (C6)		—	—	2.4	A	3, 4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin		—	—	600	mA/µs	7, 9
I_{CCA}	I_{CC} for V_{CCA} Supply		—	—	130	mA	
I_{CCP}	I_{CC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP}Supply after V_{CC} Stable		—	—	4.5 2.5	A A	10 11

NOTES: See next page.

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or Enhanced Halt State).
2. The voltage specifications are assumed to be measured across V_{CC_SENSE} and V_{SS_SENSE} pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 105 °C T_J.
4. Specified at the nominal V_{CC}.
5. Measured at the bulk capacitors on the motherboard.
6. $V_{CC,BOOT}$ tolerance shown in Figure 7 and Figure 8.
7. Based on simulations and averaged over the duration of any change in current. Specified by design/ characterization at nominal V_{CC}. Not 100% tested.
8. This is a power-up peak current specification that is applicable when V_{CCP} is high and V_{CC_CORE} is low.
9. This is a steady-state I_{CC} current specification that is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. Processor I_{CC} requirements in Intel Dynamic Acceleration Technology mode are lesser than I_{CC} in HFM
11. The maximum delta between Intel Enhanced Deeper Sleep and LFM on the processor will be lesser than or equal to 300 mV.
12. Instantaneous current $I_{CC\_CORE\_INST}$ of 24 A has to be sustained for short time (t_{INST}) of 35µs. Average current will be less than maximum specified I_{CCDES}. VR OCP threshold should be high enough to support current levels described herein.

Table 12. Voltage and Current Specifications for the Ultra-Low-Voltage, Single-Core (5.5 W) SFF Processor

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)		0.775	—	1.1	V	1, 2
V_{CCLFM}	V_{CC} at Lowest Frequency Mode (LFM)		0.8	—	0.975	V	1, 2
V_{CCSLFM}	V_{CC} at Super Low Frequency Mode (Super LFM)		0.725	—	0.925	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up		—	1.20	—	V	2, 6, 8
V_{CCP}	AGTL+ Termination Voltage		1.00	1.05	1.10	V	
V_{CCA}	PLL Supply Voltage		1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep		0.65	—	0.8	V	1, 2
V_{DC4}	V_{CC} at Intel® Enhanced Deeper Sleep State		0.6	—	0.8	V	1, 2
$V_{CCDPPWDN}$	V_{CC} at Deep Power Down Technology State (C6)		0.35	—	0.6	V	1, 2
I_{CCDES}	I_{CC} for Processors Recommended Design Target		—	—	9	A	5
I_{CC}	Processor Number	Core Frequency/Voltage	—	—	—		
	SU3500 SU3300	1.4 GHz & V_{CCHFM} 1.2 GHz & V_{CCHFM} 1.2 GHz & V_{CCLFM} 0.8 GHz & V_{CCSLFM}	—	—	9 9 9 7	A	3, 4, 12
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant HFM SuperLFM		—	—	 4.4 3.7	A	3, 4, 12
I_{SLP}	I_{CC} Sleep HFM SuperLFM		—	—	 4.1 3.5	A	3, 4, 12

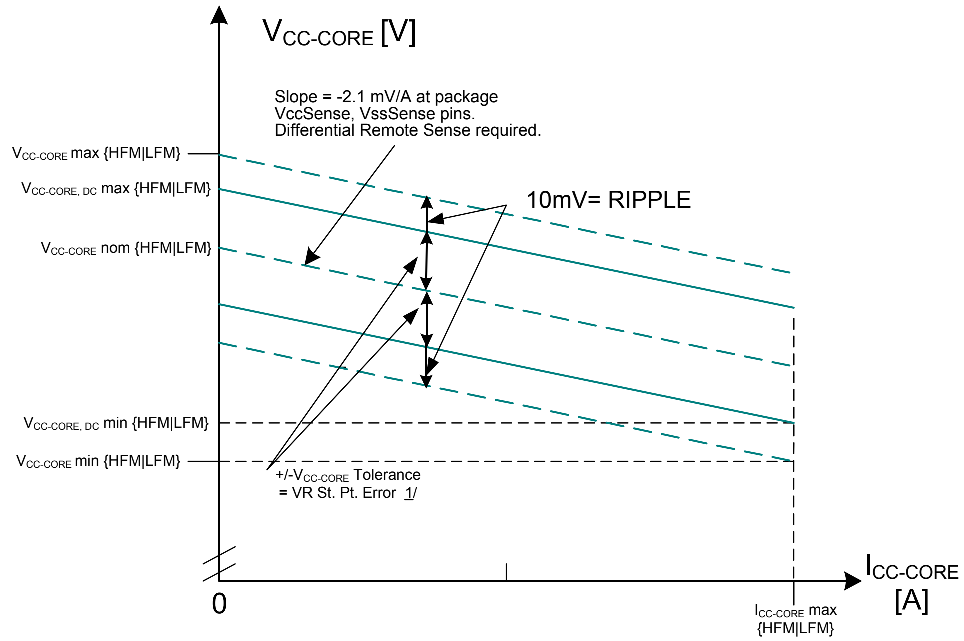
Table 12. Voltage and Current Specifications for the Ultra-Low-Voltage, Single-Core (5.5 W) SFF Processor

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{DSLP}	I_{CC} Deep Sleep HFM SuperLFM	—	—	 3.3 3.0	A	3, 4, 12
I_{DPRSLP}	I_{CC} Deeper Sleep	—	—	2.1	A	3, 4
I_{DC4}	I_{CC} Intel Enhanced Deeper Sleep State	—	—	1.9	A	3, 4
I_{DPWDN}	I_{CC} Deep Power Down Technology State (C6)	—	—	1.7	A	3, 4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin	—	—	600	mA/µs	7, 9
I_{CCA}	I_{CC} for V_{CCA} Supply	—	—	130	mA	
I_{CCP}	I_{CC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP}Supply after V_{CC} Stable	—	—	4.5 2.5	A A	10 11

NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or Enhanced Halt State).
2. The voltage specifications are assumed to be measured across V_{CC_SENSE} and V_{SS_SENSE} pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 100 °C T_J.
4. Specified at the nominal V_{CC}.
5. Measured at the bulk capacitors on the motherboard.
6. $V_{CC,BOOT}$ tolerance shown in Figure 4 and Figure 5.
7. Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal V_{CC}. Not 100% tested.
8. This is a power-up peak current specification that is applicable when V_{CCP} is high and V_{CC_CORE} is low.
9. This is a steady-state I_{CC} current specification that is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. Processor I_{CC} requirements in Intel Dynamic Acceleration Technology mode are lesser than I_{CC} in HFM
11. The maximum delta between Intel Enhanced Deeper Sleep and LFM on the processor will be lesser than or equal to 300 mV.

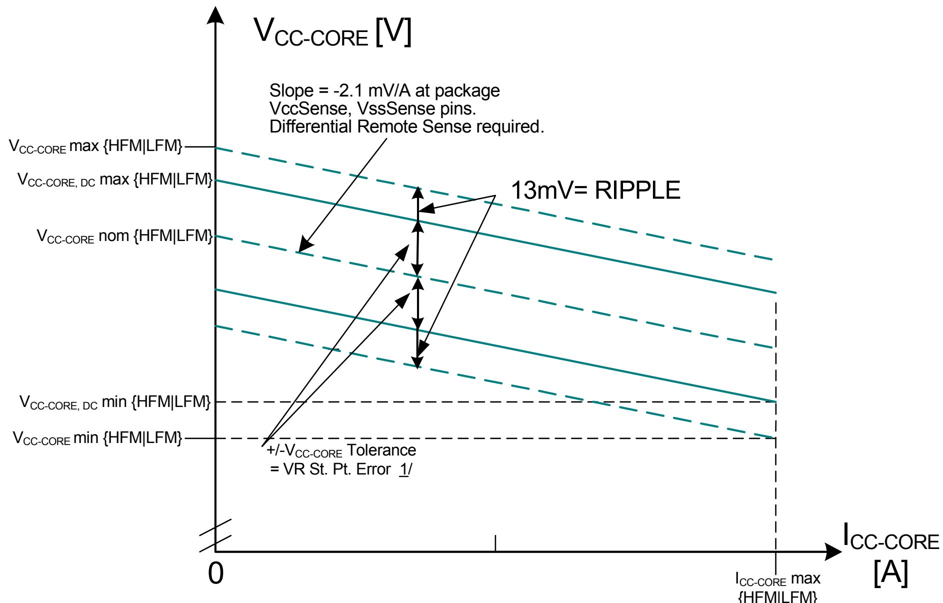
Figure 4. Active V_{CC} and I_{CC} Loadline for Standard Voltage, Low-Power SV (25 W) and Dual-Core, Extreme Edition Processors



Note 1/ $V_{CC\text{-}CORE}$ Set Point Error Tolerance is per below:

Tolerance	$V_{CC\text{-}CORE}$ VID Voltage Range
+/-1.5%	$V_{CC\text{-}CORE}$ > 0.7500V
+/-11.5mV	0.5000V </= Vcc_core </= 0.75000V

Figure 5. Deeper Sleep V_{CC} and I_{CC} Loadline for Standard-Voltage, Low-Power SV (25 W) and Dual-Core Extreme Edition Processors

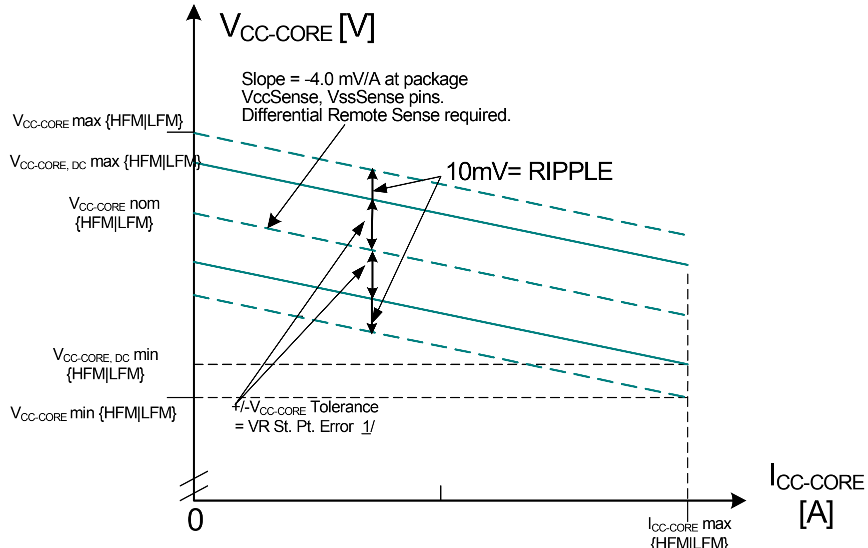


Note 1/ $V_{CC\text{-}CORE}$ Set Point Error Tolerance is per below:

Tolerance	$V_{CC\text{-}CORE}$ VID Voltage Range
+/-[(VID*1.5%)-3mV]	$V_{CC\text{-}CORE}$ > 0.7500V
+/-(11.5mV-3mV)	0.5000V </= $V_{CC\text{-}CORE}$ </= 0.7500V
Total tolerance window including ripple is +/-35mV for C6	0.3000V </= $V_{CC\text{-}CORE}$ < 0.5000V

NOTE: Deeper Sleep mode tolerance depends on VID value.

Figure 6. Deeper Sleep V_{CC} and I_{CC} Loadline for Low-Power Standard-Voltage Processors



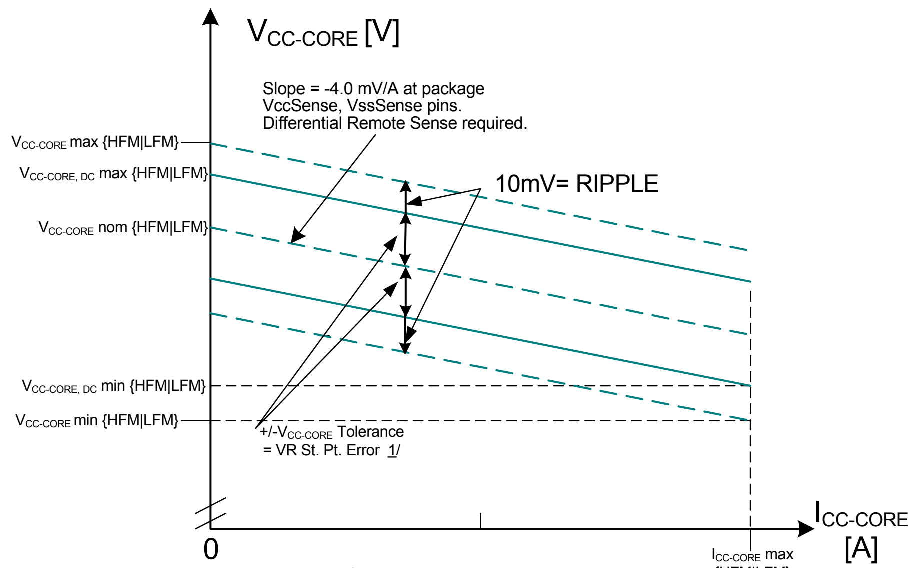
Note 1/ $V_{CC\text{-}CORE}$ Set Point Error Tolerance is per below:

Tolerance	$V_{CC\text{-}CORE}$ VID Voltage Range
+/-[(VID*1.5%)-3mV]	$V_{CC\text{-}CORE}$ > 0.7500V
+/-(11.5mV-3mV)	0.5000V </= $V_{CC\text{-}CORE}$ </= 0.7500V
Total tolerance window including ripple is +/-35mV for C6	0.3000V </= $V_{CC\text{-}CORE}$ < 0.5000V

NOTES:

1. Applies to low-power standard-voltage 22-mm (dual-core) processors.
2. Deeper Sleep mode tolerance depends on VID value.

Figure 7. Active VCC and ICC Loadline for Low-Voltage, Ultra-Low-Voltage and Power Optimized Performance Processor



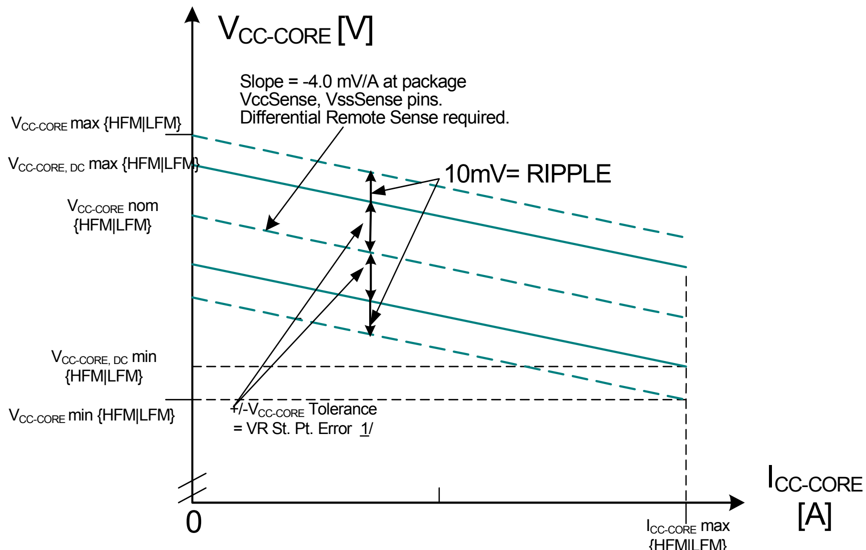
Note 1/ $V_{CC\text{-}CORE}$ Set Point Error Tolerance is per below:

Tolerance	$V_{CC\text{-}CORE}$ VID Voltage Range
+/-1.5%	$V_{CC\text{-}CORE}$ > 0.7500V
+/-11.5mV	0.5000V </= $V_{CC\text{-}CORE}$ </= 0.7500V
+/-25mV	0.3000V </= $V_{CC\text{-}CORE}$ < 0.5000V

NOTES:

1. Applies to Low-Voltage, Ultra-Low-Voltage and Power Optimised Performance processors in 22 mmx22 mm package.
2. Active mode tolerance depends on VID value

Figure 8. Deeper Sleep VCC and ICC Loadline for Low-Voltage, Ultra-Low-Voltage and Power Optimized Performance Processor



Note 1/ $V_{CC\text{-}CORE}$ Set Point Error Tolerance is per below:

Tolerance	$V_{CC\text{-}CORE}$ VID Voltage Range
+/-[(VID*1.5%)-3mV]	$V_{CC\text{-}CORE}$ > 0.7500V
+/-(11.5mV-3mV)	0.5000V </= $V_{CC\text{-}CORE}$ </= 0.7500V
Total tolerance window including ripple is +/-35mV for C6	0.3000V </= $V_{CC\text{-}CORE}$ < 0.5000V

NOTES:
1. Applies to Low-Voltage, Ultra-Low-Voltage and Power Optimised Performance processors in 22 mmx22 mm package.
2. Deeper Sleep mode tolerance depends on VID value.

Table 13. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CCP}	I/O Voltage	1.00	1.05	1.10	V	
GTLREF	Reference Voltage	0.65	0.70	0.72	V	6
R_{COMP}	Compensation Resistor	27.23	27.5	27.78	Ω	10
$R_{ODT/A}$	Termination Resistor Address	49	55	63	Ω	11, 12
$R_{ODT/D}$	Termination Resistor Data	49	55	63	Ω	11, 13
$R_{ODT/Cntrl}$	Termination Resistor Control	49	55	63	Ω	11, 14
V_{IH}	Input High Voltage	0.82	1.05	1.20	V	3,6
V_{IL}	Input Low Voltage	-0.10	0	0.55	V	2,4
V_{OH}	Output High Voltage	0.90	V_{CCP}	1.10	V	6
$R_{TT/A}$	Termination Resistance Address	50	55	61	Ω	7, 12
$R_{TT/D}$	Termination Resistance Data	50	55	61	Ω	7, 13
$R_{TT/Cntrl}$	Termination Resistance Control	50	55	61	Ω	7, 14
$R_{ON/A}$	Buffer On Resistance Address	23	25	29	Ω	5, 12
$R_{ON/D}$	Buffer On Resistance Data	23	25	29	Ω	5, 13
$R_{ON/Cntrl}$	Buffer On Resistance Control	23	25	29	Ω	5, 14
I_{LI}	Input Leakage Current	—	—	± 100	µA	8
Cpad	Pad Capacitance	1.80	2.30	2.75	pF	9

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{CCP}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pulldown driver resistance. Measured at 0.31*V_{CCP}. R_{ON} (min) = 0.418*R_{TT}, R_{ON} (typ) = 0.455*R_{TT},
   R_{ON} (max) = 0.527*R_{TT}. R_{TT} typical value of 55 Ω is used for R_{ON} typ/min/max calculations.
6. GTLREF should be generated from V_{CCP} with a 1% tolerance resistor divider. The V_{CCP} referred to in these specifications is the instantaneous V_{CCP}.
7. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver. Measured at 0.31*V_{CCP}. R_{TT} is connected to V_{CCP} on die. Refer to processor I/O buffer models for I/V characteristics.
8. Specified with on-die R_{TT} and R_{ON} turned off. Vin between 0 and V_{CCP}.
9. Cpad includes die capacitance only. No package parasitics are included.
10. This is the external resistor on the comp pins.
11. On-die termination resistance, measured at 0.33*V_{CCP}.
12. Applies to Signals A[35:3].
13. Applies to Signals D[63:0].
14. Applies to Signals BPRI#, DEFER#, PREQ#, PREST#, RS[2:0]#, TRDY#, ADS#, BNR#, BPM[3:0], BR0#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, PRDY#, DPWR#, DSTB[1:0]#, DSTBP[3:0] and DSTBN[3:0]#.

Table 14. CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CCP}	I/O Voltage	1.00	1.05	1.10	V	
V_{IL}	Input Low Voltage CMOS	-0.10	0.00	$0.3*V_{CCP}$	V	2
V_{IH}	Input High Voltage	$0.7*V_{CCP}$	V_{CCP}	$V_{CCP}+0.1$	V	2
V_{OL}	Output Low Voltage	-0.10	0	$0.1*V_{CCP}$	V	2
V_{OH}	Output High Voltage	$0.9*V_{CCP}$	V_{CCP}	$V_{CCP}+0.1$	V	2
I_{OL}	Output Low Current	1.5	—	4.1	mA	3
I_{OH}	Output High Current	1.5	—	4.1	mA	4
I_{LI}	Input Leakage Current	—	—	±100	µA	5
Cpad1	Pad Capacitance	1.80	2.30	2.75	pF	6
Cpad2	Pad Capacitance for CMOS Input	0.95	1.2	1.45	pF	7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{CCP} referred to in these specifications refers to instantaneous V_{CCP}.
3. Measured at 0.1 $*V_{CCP}$.
4. Measured at 0.9 $*V_{CCP}$.
5. For Vin between 0 V and V_{CCP}. Measured when the driver is tristated.
6. Cpad1 includes die capacitance only for DPRSTP#, DPSLP#, PWRGOOD. No package parasitics are included.
7. Cpad2 includes die capacitance for all other CMOS input signals. No package parasitics are included.

Table 15. Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{OH}	Output High Voltage	V_{CCP}–5%	V_{CCP}	V_{CCP}+5%	V	3
V_{OL}	Output Low Voltage	0	—	0.20	V	
I_{OL}	Output Low Current	16	—	50	mA	2
I_{LO}	Output Leakage Current	—	—	±200	µA	4
Cpad	Pad Capacitance	1.80	2.30	2.75	pF	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at 0.2 V.
3. V_{OH} is determined by value of the external pull-up resistor to V_{CCP}.
4. For Vin between 0 V and V_{OH}.
5. Cpad includes die capacitance only. No package parasitics are included.

§

4 Package Mechanical Specifications and Pin Information

4.1 Package Mechanical Specifications

The processor (XE and SV) is available in 478-pin Micro-FCPGA packages as well as 479-ball Micro-FCBGA packages. The package mechanical dimensions are shown in Figure 9 through Figure 13.

The processor (POP, LV, ULV DC and ULV SC) is available 956-ball Micro-FCBGA packages. The package mechanical dimensions are shown in Figure 14 and Figure 15. The maximum outgoing co-planarity is 0.2 mm (8 mils) for SFF processors.

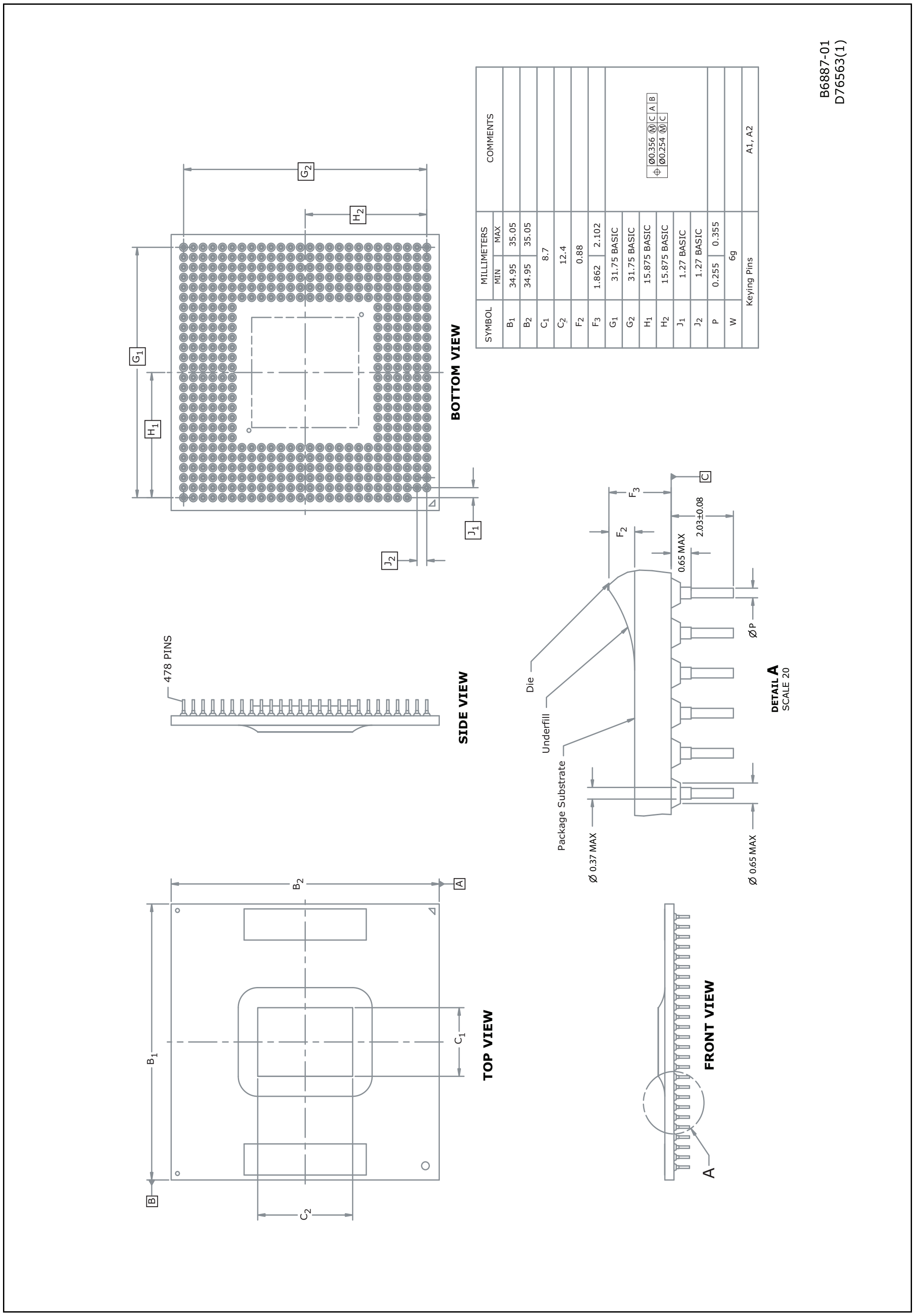
The mechanical package pressure specifications are in a direction normal to the surface of the processor. This protects the processor die from fracture risk due to uneven die pressure distribution under tilt, stack-up tolerances and other similar conditions. These specifications assume that a mechanical attach is designed specifically to load one type of processor.

A 15-lbf load limit should not be exceeded on BGA packages so as to not impact solder joint reliability after reflow. This load limit ensures that impact to the package solder joints due to transient bend, shock, or tensile loading is minimized. The 15-lbf metric should be used **in parallel** with the 689-kPa (100 psi) pressure limit as long as neither limits are exceeded. In some cases, designing to 15 lbf will exceed the pressure specification of 689 kPa (100 psi) and therefore should be reduced to ensure both limits are maintained.

Moreover, the processor package substrate should not be used as a mechanical reference or load-bearing surface for the thermal or mechanical solution.

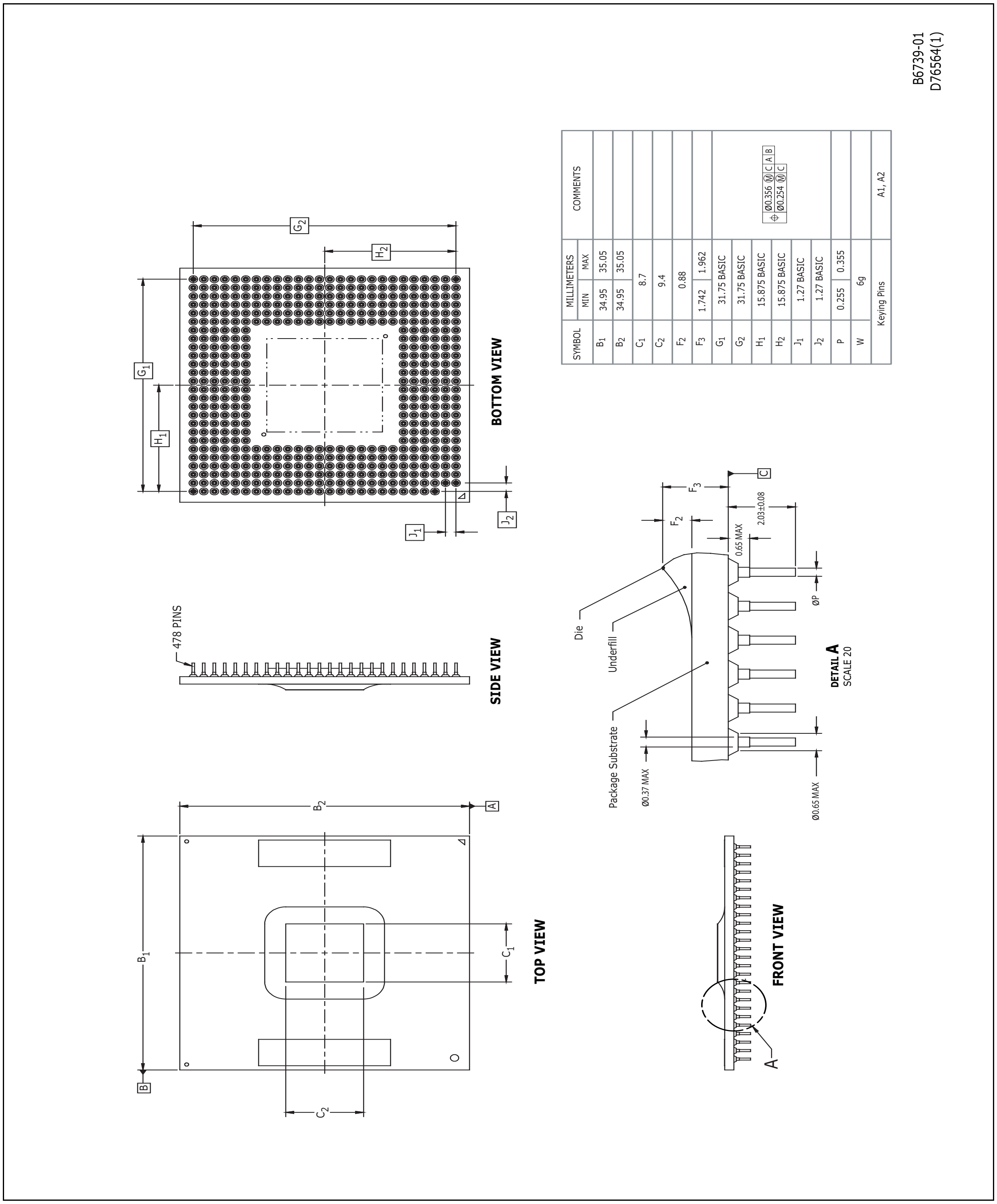
Caution: The Micro-FCBGA package incorporates land-side capacitors. The land-side capacitors are electrically conductive so care should be taken to avoid contacting the capacitors with other electrically conductive materials on the motherboard. Doing so may short the capacitors and possibly damage the device or render it inactive.

Figure 9. 6-MB and 3-MB on 6-MB Die Micro-FCPGA Package Drawing (Sheet 1 of 2)



SYMBOL	MILLIMETERS MIN	MILLIMETERS MAX	COMMENTS
B_1	34.95	35.05	
B_2	34.95	35.05	
C_1	8.7		
C_2	12.4		
F_2	0.88		
F_3	1.862	2.102	
G_1	31.75 BASIC		⌖ Ø0.356 Ⓜ C A B / Ø0.254 Ⓜ C
G_2	31.75 BASIC		
H_1	15.875 BASIC		
H_2	15.875 BASIC		
J_1	1.27 BASIC		
J_2	1.27 BASIC		
P	0.255	0.355	
W	6g		
Keying Pins			A1, A2

Figure 10. 3-MB die Micro-FCPGA Processor Package Drawing (Sheet 1 of 2)



SYMBOL	MILLIMETERS MIN	MILLIMETERS MAX	COMMENTS
B_1	34.95	35.05	
B_2	34.95	35.05	
C_1	8.7		
C_2	9.4		
F_2		0.88	
F_3	1.742	1.962	
G_1	31.75 BASIC		⌖ Ø0.356 Ⓜ C A B / Ø0.254 Ⓜ C
G_2	31.75 BASIC		
H_1	15.875 BASIC		
H_2	15.875 BASIC		
J_1	1.27 BASIC		
J_2	1.27 BASIC		
P	0.255	0.355	
W	6g		
	Keying Pins		A1, A2

Figure 11. 3-MB Die Micro-FCPGA Processor Package Drawing (Sheet 2 of 2)

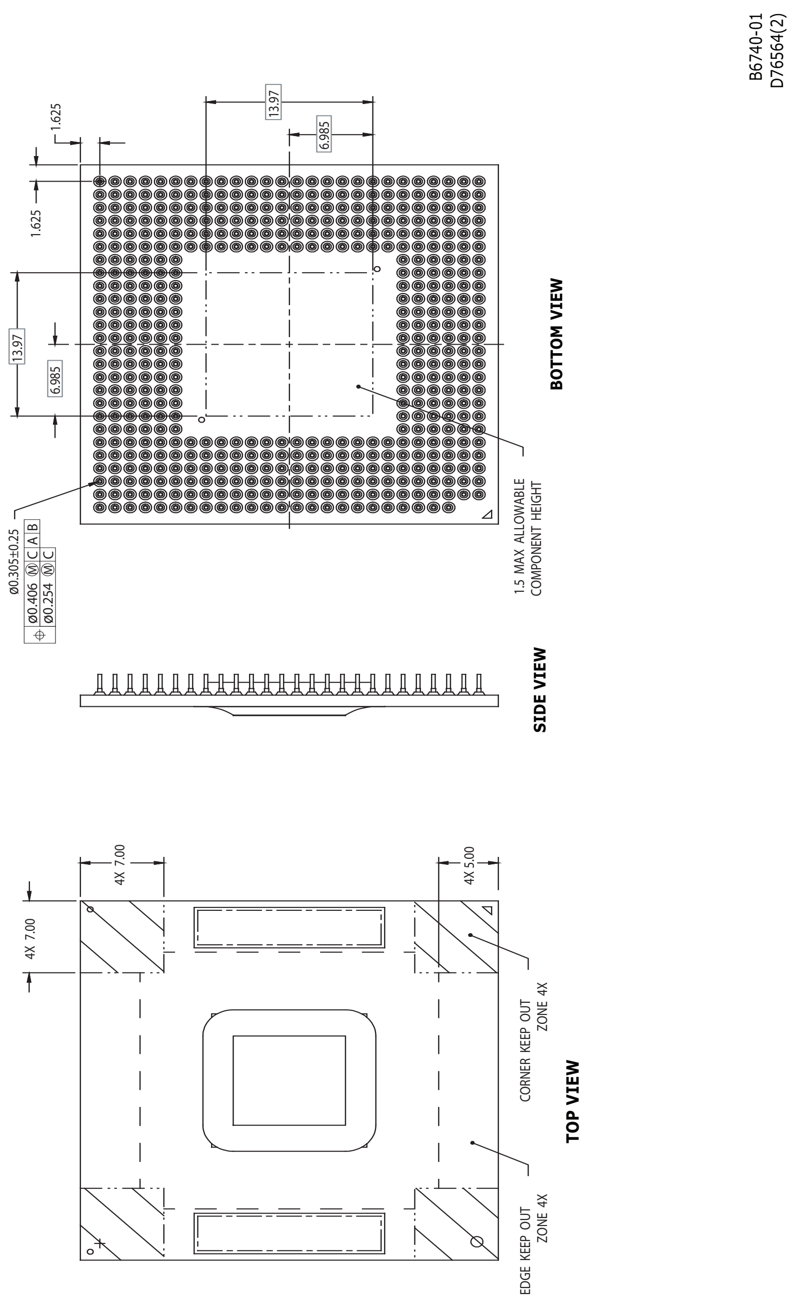
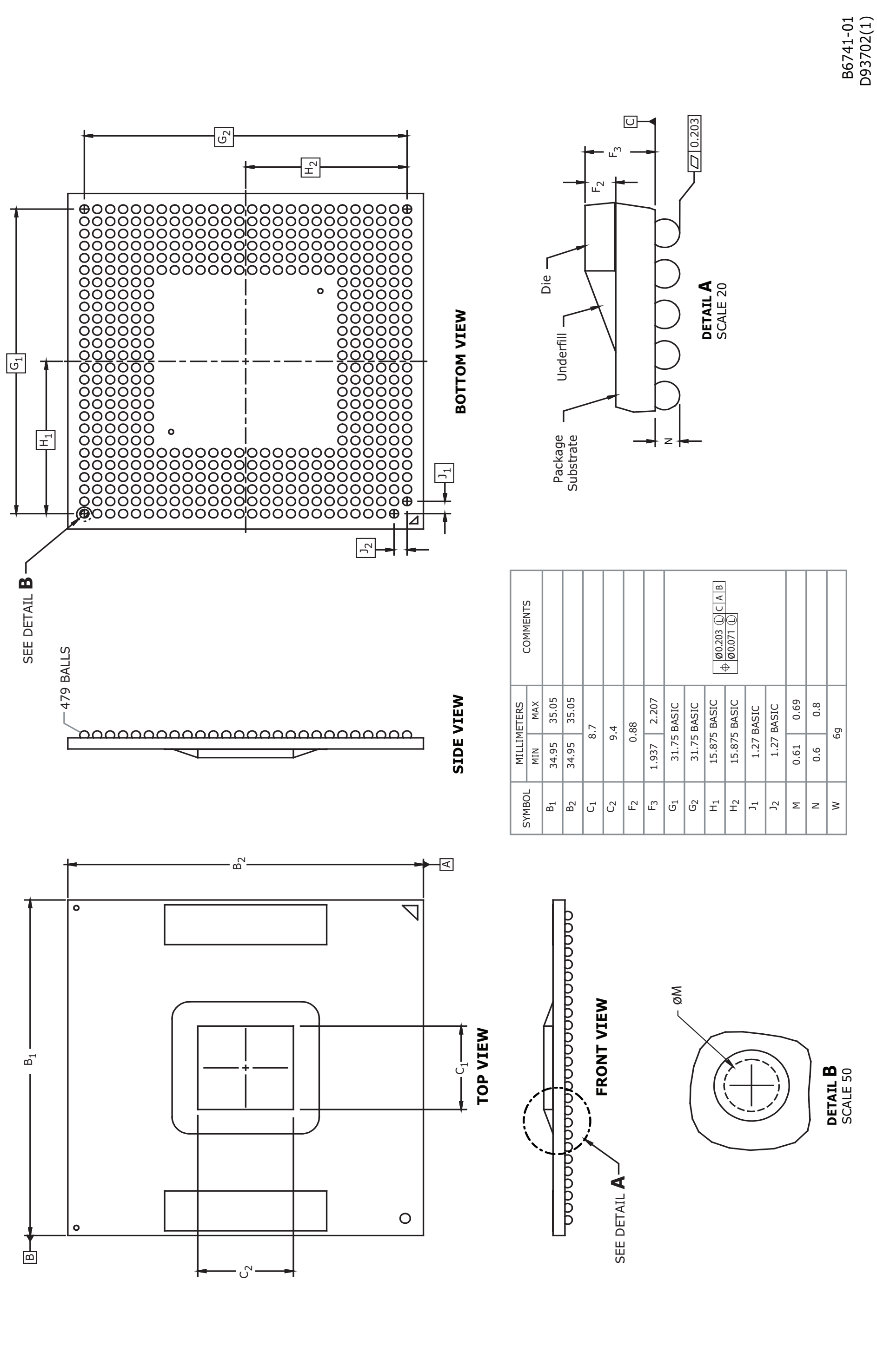


Figure 12. 3-MB Die Micro-FCBGA Processor Package Drawing (Sheet 1 of 2)



SYMBOL	MILLIMETERS MIN	MILLIMETERS MAX	COMMENTS
B_1	34.95	35.05	
B_2	34.95	35.05	
C_1	8.7		
C_2	9.4		
F_2	0.88		
F_3	1.937	2.207	
G_1	31.75 BASIC		⌀0.203 Ⓛ C A B / ⌀0.071 Ⓛ
G_2	31.75 BASIC		
H_1	15.875 BASIC		
H_2	15.875 BASIC		
J_1	1.27 BASIC		
J_2	1.27 BASIC		
M	0.61	0.69	
N	0.6	0.8	
W	6g		

Figure 13. 3-MB Die Micro-FCBGA Processor Package Drawing (Sheet 2 of 2)

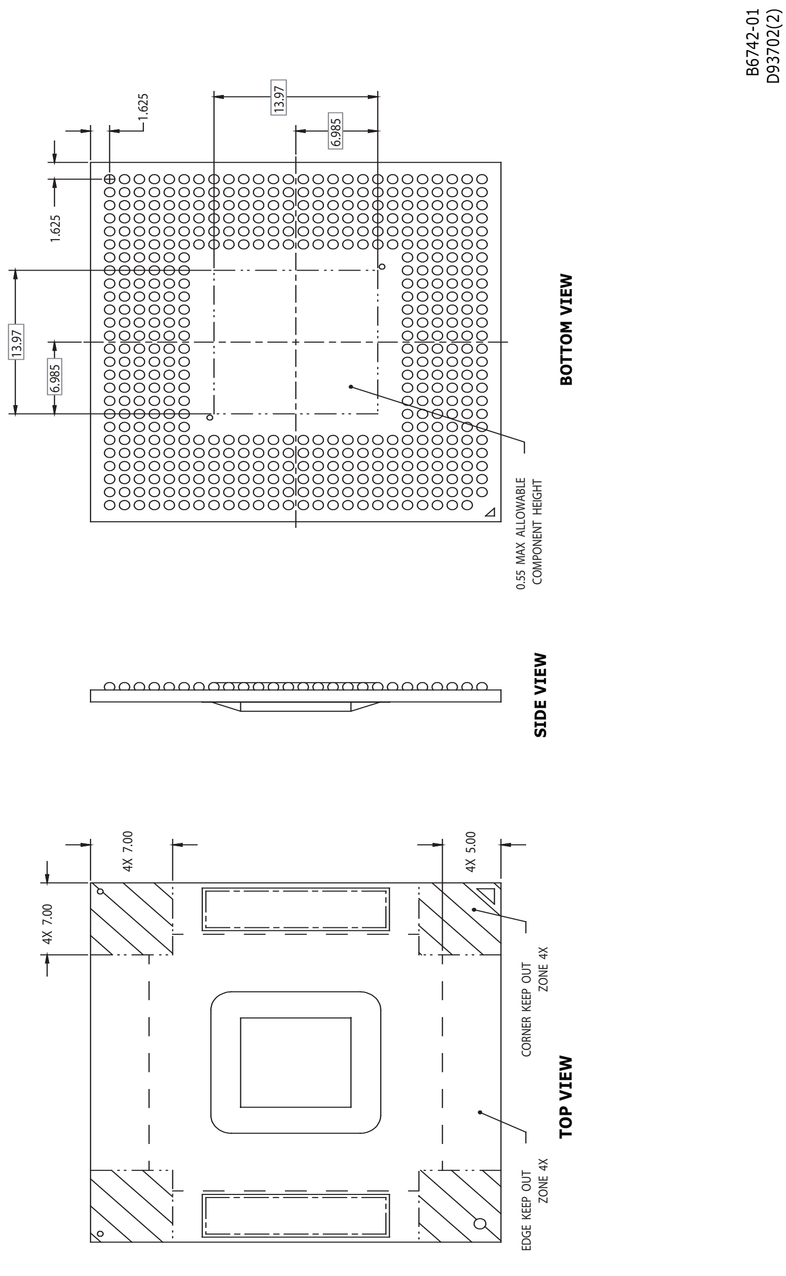
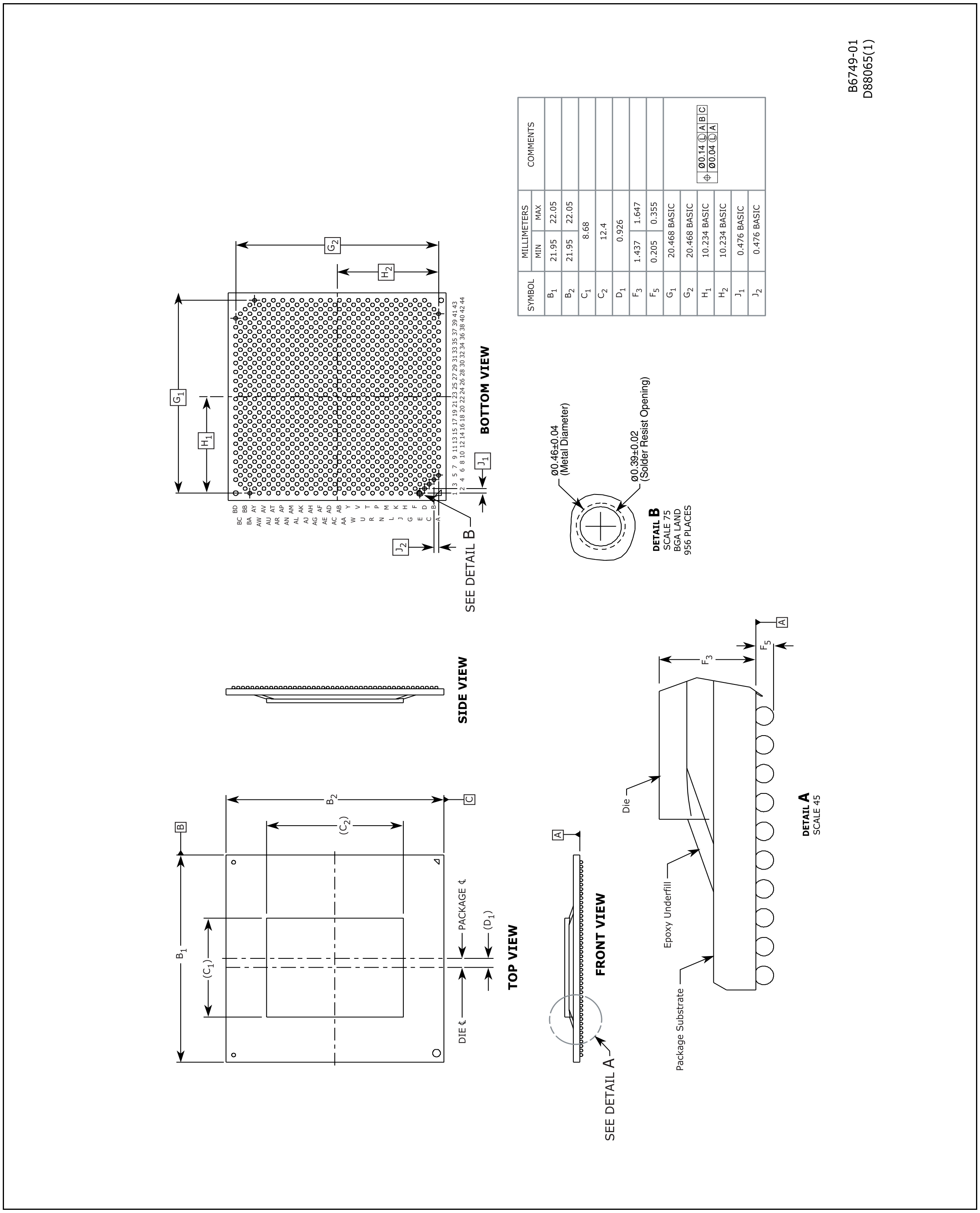
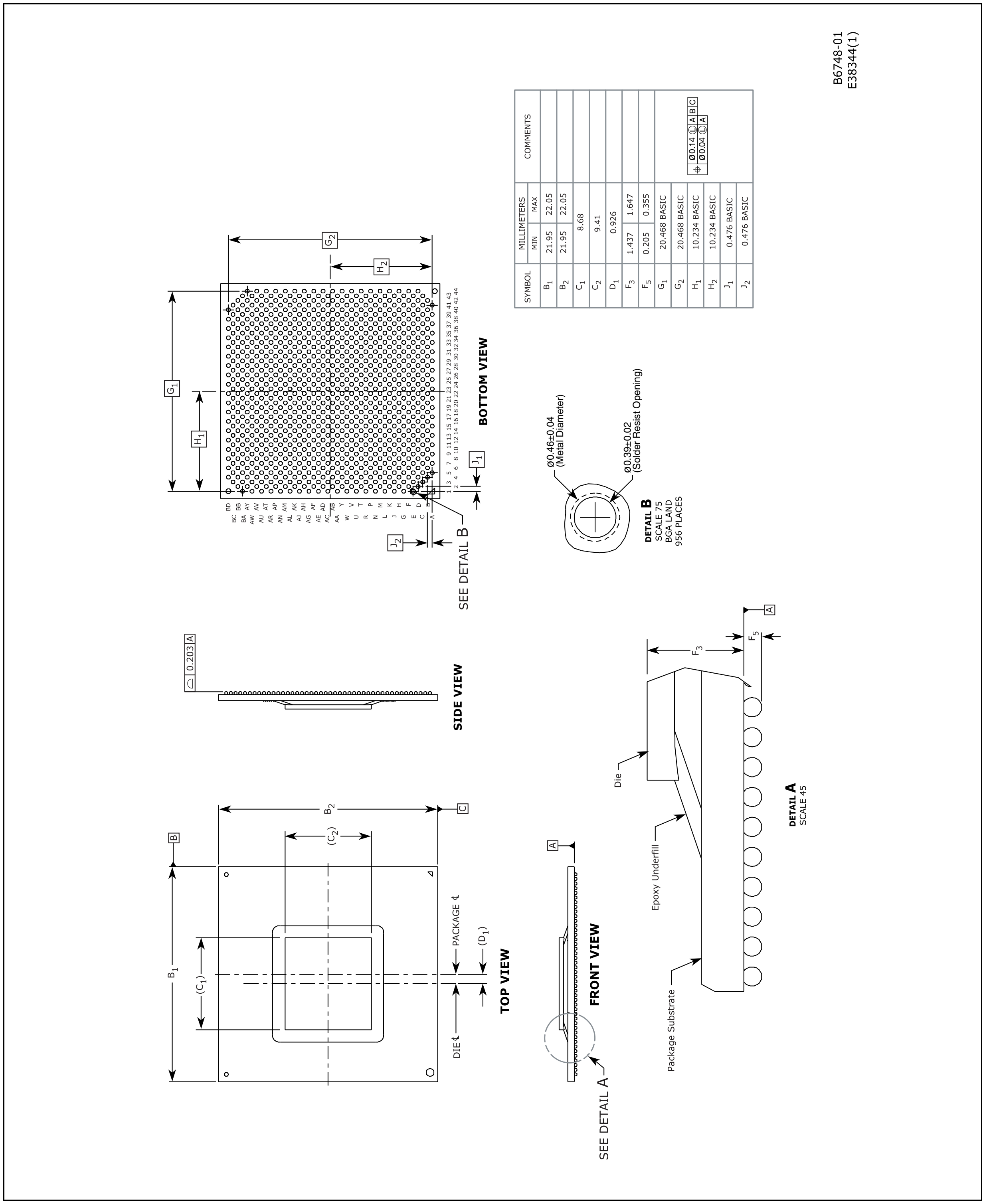


Figure 14. Intel Core 2 Duo Mobile Processor (POP and LV) Die Micro-FCBGA Processor Package Drawing



SYMBOL	MILLIMETERS MIN	MILLIMETERS MAX	COMMENTS
B_1	21.95	22.05	
B_2	21.95	22.05	
C_1	8.68		
C_2	12.4		
D_1	0.926		
F_3	1.437	1.647	
F_5	0.205	0.355	
G_1	20.468 BASIC		
G_2	20.468 BASIC		
H_1	10.234 BASIC		⌖ Ø0.14 Ⓛ A B C Ø0.04 Ⓛ A
H_2	10.234 BASIC		
J_1	0.476 BASIC		
J_2	0.476 BASIC		

Figure 15. Intel Core 2 Duo Mobile Processor (ULV SC and ULV DC) Die Micro-FCBGA Processor Package Drawing



SYMBOL	MILLIMETERS MIN	MILLIMETERS MAX	COMMENTS
B_1	21.95	22.05	
B_2	21.95	22.05	
C_1	8.68		
C_2	9.41		
D_1	0.926		
F_3	1.437	1.647	
F_5	0.205	0.355	
G_1	20.468 BASIC		⌖ Ø0.14 Ⓛ A B C; Ø0.04 Ⓛ A
G_2	20.468 BASIC		
H_1	10.234 BASIC		
H_2	10.234 BASIC		
J_1	0.476 BASIC		
J_2	0.476 BASIC		

4.2 Processor Pinout and Pin List

Figure 16 and Figure 17 show the processor (SV and XE) pinout as viewed from the top of the package. Table 16 provides the pin list, arranged numerically by pin number. Figure 16 through Figure 18 show the top view of the LV and ULV processor package. Table 18 lists the SFF processor ballout alphabetically by signal name. For signal descriptions, refer to Section 4.3.

Figure 16. Processor Pinout (Top Package View, Left Side)

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A[1]		VSS	SMI#	VSS	FERR#	A20M#	VCC	VSS	VCC	VCC	VSS	VCC	VCC	A
B[1]		RSVD	INIT#	LINT1	DPSLP#	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VSS	B
C	RESET#	VSS	TEST7	IGNNE #	VSS	LINT0	THERM TRIP#	VSS	VCC	VCC	VSS	VCC	VCC	C
D	VSS	RSVD	RSVD	VSS	STPCLK #	PWRGO OD	SLP#	VSS	VCC	VCC	VSS	VCC	VSS	D
E	DBSY#	BNR#	VSS	HITM#	DPRSTP #	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VCC	E
F	BR0#	VSS	RS[0]#	RS[1]#	VSS	RSVD	VCC	VSS	VCC	VCC	VSS	VCC	VSS	F
G	VSS	TRDY#	RS[2]#	VSS	BPRI#	HIT#								G
H	ADS#	REQ[1] #	VSS	LOCK#	DEFER#	VSS								H
J	A[9]#	VSS	REQ[3] #	A[3]#	VSS	VCCP								J
K	VSS	REQ[2] #	REQ[0] #	VSS	A[6]#	VCCP								K
L	REQ[4]#	A[13]#	VSS	A[5]#	A[4]#	VSS								L
M	ADSTB[0] #	VSS	A[7]#	RSVD	VSS	VCCP								M
N	VSS	A[8]#	A[10]#	VSS	RSVD	VCCP								N
P	A[15]#	A[12]#	VSS	A[14]#	A[11]#	VSS								P
R	A[16]#	VSS	A[19]#	A[24]#	VSS	VCCP								R
T	VSS	RSVD	A[26]#	VSS	A[25]#	VCCP								T
U	A[23]#	A[30]#	VSS	A[21]#	A[18]#	VSS								U
V	ADSTB[1] #	VSS	RSVD	A[31]#	VSS	VCCP								V
W	VSS	A[27]#	A[32]#	VSS	A[28]#	A[20]#								W
Y	COMP[3]	A[17]#	VSS	A[29]#	A[22]#	VSS								Y
AA	COMP[2]	VSS	A[35]#	A[33]#	VSS	TDI	VCC	VSS	VCC	VCC	VSS	VCC	VCC	AA
AB	VSS	A[34]#	TDO	VSS	TMS	TRST#	VCC	VSS	VCC	VCC	VSS	VCC	VSS	AB
AC	PREQ#	PRDY#	VSS	BPM[3] #	TCK	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VCC	AC
AD	BPM[2]#	VSS	BPM[1] #	BPM[0] #	VSS	VID[0]	VCC	VSS	VCC	VCC	VSS	VCC	VSS	AD
AE	VSS	VID[6]	VID[4]	VSS	VID[2]	PSI#	VSS SENSE	VSS	VCC	VCC	VSS	VCC	VCC	AE
AF	TEST5	VSS	VID[5]	VID[3]	VID[1]	VSS	VCC SENSE	VSS	VCC	VCC	VSS	VCC	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

NOTES:
1. Keying option for Micro-FCPGA, A1 and B1 are de-populated.
2. Keying option for Micro-FCBGA, A1 is de-populated and B1 is VSS.

Figure 17. Processor Pinout (Top Package View, Right Side)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VCC	VSS	VCC	VCC	VSS	VCC	BCLK[1]	BCLK[0]	VSS	THRMDA	VSS	TEST6	A
B	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VSS	BSEL[0]	BSEL[1]	VSS	THRMDC	VCCA	B
C	VSS	VCC	VSS	VCC	VCC	VSS	DBR#	BSEL[2]	VSS	TEST1	TEST3	VSS	VCCA	C
D	VCC	VCC	VSS	VCC	VCC	VSS	IERR#	PROCHOT#	RSVD	VSS	DPWR#	TEST2	VSS	D
E	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VSS	D[0]#	D[7]#	VSS	D[6]#	D[2]#	E
F	VCC	VCC	VSS	VCC	VCC	VSS	VCC	DRDY#	VSS	D[4]#	D[1]#	VSS	D[13]#	F
G								VCCP	D[3]#	VSS	D[9]#	D[5]#	VSS	G
H								VSS	D[12]#	D[15]#	VSS	DINV[0]#	DSTBP[0]#	H
J								VCCP	VSS	D[11]#	D[10]#	VSS	DSTBN[0]#	J
K								VCCP	D[14]#	VSS	D[8]#	D[17]#	VSS	K
L								VSS	D[22]#	D[20]#	VSS	D[29]#	DSTBN[1]#	L
M								VCCP	VSS	D[23]#	D[21]#	VSS	DSTBP[1]#	M
N								VCCP	D[16]#	VSS	DINV[1]#	D[31]#	VSS	N
P								VSS	D[26]#	D[25]#	VSS	D[24]#	D[18]#	P
R								VCCP	VSS	D[19]#	D[28]#	VSS	COMP[0]	R
T								VCCP	D[37]#	VSS	D[27]#	D[30]#	VSS	T
U								VSS	DINV[2]#	D[39]#	VSS	D[38]#	COMP[1]	U
V								VCCP	VSS	D[36]#	D[34]#	VSS	D[35]#	V
W								VCCP	D[41]#	VSS	D[43]#	D[44]#	VSS	W
Y								VSS	D[32]#	D[42]#	VSS	D[40]#	DSTBN[2]#	Y
AA	VSS	VCC	VSS	VCC	VCC	VSS	VCC	D[50]#	VSS	D[45]#	D[46]#	VSS	DSTBP[2]#	AA
AB	VCC	VCC	VSS	VCC	VCC	VSS	VCC	D[52]#	D[51]#	VSS	D[33]#	D[47]#	VSS	AB
AC	VSS	VCC	VSS	VCC	VCC	VSS	DINV[3]#	VSS	D[60]#	D[63]#	VSS	D[57]#	D[53]#	AC
AD	VCC	VCC	VSS	VCC	VCC	VSS	D[54]#	D[59]#	VSS	D[61]#	D[49]#	VSS	GTLREF	AD
AE	VSS	VCC	VSS	VCC	VCC	VSS	VCC	D[58]#	D[55]#	VSS	D[48]#	DSTBN[3]#	VSS	AE
AF	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VSS	D[62]#	D[56]#	DSTBP[3]#	VSS	TEST4	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
A[3]#	J4	Source Synch	Input/ Output
A[4]#	L5	Source Synch	Input/ Output
A[5]#	L4	Source Synch	Input/ Output
A[6]#	K5	Source Synch	Input/ Output
A[7]#	M3	Source Synch	Input/ Output
A[8]#	N2	Source Synch	Input/ Output
A[9]#	J1	Source Synch	Input/ Output
A[10]#	N3	Source Synch	Input/ Output
A[11]#	P5	Source Synch	Input/ Output
A[12]#	P2	Source Synch	Input/ Output
A[13]#	L2	Source Synch	Input/ Output
A[14]#	P4	Source Synch	Input/ Output
A[15]#	P1	Source Synch	Input/ Output
A[16]#	R1	Source Synch	Input/ Output
A[17]#	Y2	Source Synch	Input/ Output
A[18]#	U5	Source Synch	Input/ Output
A[19]#	R3	Source Synch	Input/ Output
A[20]#	W6	Source Synch	Input/ Output
A[21]#	U4	Source Synch	Input/ Output
A[22]#	Y5	Source Synch	Input/ Output
A[23]#	U1	Source Synch	Input/ Output

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
A[24]#	R4	Source Synch	Input/ Output
A[25]#	T5	Source Synch	Input/ Output
A[26]#	T3	Source Synch	Input/ Output
A[27]#	W2	Source Synch	Input/ Output
A[28]#	W5	Source Synch	Input/ Output
A[29]#	Y4	Source Synch	Input/ Output
A[30]#	U2	Source Synch	Input/ Output
A[31]#	V4	Source Synch	Input/ Output
A[32]#	W3	Source Synch	Input/ Output
A[33]#	AA4	Source Synch	Input/ Output
A[34]#	AB2	Source Synch	Input/ Output
A[35]#	AA3	Source Synch	Input/ Output
A20M#	A6	CMOS	Input
ADS#	H1	Common Clock	Input/ Output
ADSTB[0]#	M1	Source Synch	Input/ Output
ADSTB[1]#	V1	Source Synch	Input/ Output
BCLK[0]	A22	Bus Clock	Input
BCLK[1]	A21	Bus Clock	Input
BNR#	E2	Common Clock	Input/ Output
BPM[0]#	AD4	Common Clock	Input/ Output
BPM[1]#	AD3	Common Clock	Output
BPM[2]#	AD1	Common Clock	Output
BPM[3]#	AC4	Common Clock	Input/ Output

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
BPRI#	G5	Common Clock	Input
BR0#	F1	Common Clock	Input/ Output
BSEL[0]	B22	CMOS	Output
BSEL[1]	B23	CMOS	Output
BSEL[2]	C21	CMOS	Output
COMP[0]	R26	Power/ Other	Input/ Output
COMP[1]	U26	Power/ Other	Input/ Output
COMP[2]	AA1	Power/ Other	Input/ Output
COMP[3]	Y1	Power/ Other	Input/ Output
D[0]#	E22	Source Synch	Input/ Output
D[1]#	F24	Source Synch	Input/ Output
D[2]#	E26	Source Synch	Input/ Output
D[3]#	G22	Source Synch	Input/ Output
D[4]#	F23	Source Synch	Input/ Output
D[5]#	G25	Source Synch	Input/ Output
D[6]#	E25	Source Synch	Input/ Output
D[7]#	E23	Source Synch	Input/ Output
D[8]#	K24	Source Synch	Input/ Output
D[9]#	G24	Source Synch	Input/ Output
D[10]#	J24	Source Synch	Input/ Output
D[11]#	J23	Source Synch	Input/ Output
D[12]#	H22	Source Synch	Input/ Output
D[13]#	F26	Source Synch	Input/ Output

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
D[14]#	K22	Source Synch	Input/ Output
D[15]#	H23	Source Synch	Input/ Output
D[16]#	N22	Source Synch	Input/ Output
D[17]#	K25	Source Synch	Input/ Output
D[18]#	P26	Source Synch	Input/ Output
D[19]#	R23	Source Synch	Input/ Output
D[20]#	L23	Source Synch	Input/ Output
D[21]#	M24	Source Synch	Input/ Output
D[22]#	L22	Source Synch	Input/ Output
D[23]#	M23	Source Synch	Input/ Output
D[24]#	P25	Source Synch	Input/ Output
D[25]#	P23	Source Synch	Input/ Output
D[26]#	P22	Source Synch	Input/ Output
D[27]#	T24	Source Synch	Input/ Output
D[28]#	R24	Source Synch	Input/ Output
D[29]#	L25	Source Synch	Input/ Output
D[30]#	T25	Source Synch	Input/ Output
D[31]#	N25	Source Synch	Input/ Output
D[32]#	Y22	Source Synch	Input/ Output
D[33]#	AB24	Source Synch	Input/ Output
D[34]#	V24	Source Synch	Input/ Output
D[35]#	V26	Source Synch	Input/ Output

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
D[36]#	V23	Source Synch	Input/ Output
D[37]#	T22	Source Synch	Input/ Output
D[38]#	U25	Source Synch	Input/ Output
D[39]#	U23	Source Synch	Input/ Output
D[40]#	Y25	Source Synch	Input/ Output
D[41]#	W22	Source Synch	Input/ Output
D[42]#	Y23	Source Synch	Input/ Output
D[43]#	W24	Source Synch	Input/ Output
D[44]#	W25	Source Synch	Input/ Output
D[45]#	AA23	Source Synch	Input/ Output
D[46]#	AA24	Source Synch	Input/ Output
D[47]#	AB25	Source Synch	Input/ Output
D[48]#	AE24	Source Synch	Input/ Output
D[49]#	AD24	Source Synch	Input/ Output
D[50]#	AA21	Source Synch	Input/ Output
D[51]#	AB22	Source Synch	Input/ Output
D[52]#	AB21	Source Synch	Input/ Output
D[53]#	AC26	Source Synch	Input/ Output
D[54]#	AD20	Source Synch	Input/ Output
D[55]#	AE22	Source Synch	Input/ Output
D[56]#	AF23	Source Synch	Input/ Output
D[57]#	AC25	Source Synch	Input/ Output

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
D[58]#	AE21	Source Synch	Input/ Output
D[59]#	AD21	Source Synch	Input/ Output
D[60]#	AC22	Source Synch	Input/ Output
D[61]#	AD23	Source Synch	Input/ Output
D[62]#	AF22	Source Synch	Input/ Output
D[63]#	AC23	Source Synch	Input/ Output
DBR#	C20	CMOS	Output
DBSY#	E1	Common Clock	Input/ Output
DEFER#	H5	Common Clock	Input
DINV[0]#	H25	Source Synch	Input/ Output
DINV[1]#	N24	Source Synch	Input/ Output
DINV[2]#	U22	Source Synch	Input/ Output
DINV[3]#	AC20	Source Synch	Input/ Output
DPRSTP#	E5	CMOS	Input
DPSLP#	B5	CMOS	Input
DPWR#	D24	Common Clock	Input/ Output
DRDY#	F21	Common Clock	Input/ Output
DSTBN[0]#	J26	Source Synch	Input/ Output
DSTBN[1]#	L26	Source Synch	Input/ Output
DSTBN[2]#	Y26	Source Synch	Input/ Output
DSTBN[3]#	AE25	Source Synch	Input/ Output
DSTBP[0]#	H26	Source Synch	Input/ Output
DSTBP[1]#	M26	Source Synch	Input/ Output

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
DSTBP[2]#	AA26	Source Synch	Input/ Output
DSTBP[3]#	AF24	Source Synch	Input/ Output
FERR#	A5	Open Drain	Output
GTLREF	AD26	Power/ Other	Input
HIT#	G6	Common Clock	Input/ Output
HITM#	E4	Common Clock	Input/ Output
IERR#	D20	Open Drain	Output
IGNNE#	C4	CMOS	Input
INIT#	B3	CMOS	Input
LINT0	C6	CMOS	Input
LINT1	B4	CMOS	Input
LOCK#	H4	Common Clock	Input/ Output
PRDY#	AC2	Common Clock	Output
PREQ#	AC1	Common Clock	Input
PROCHOT#	D21	Open Drain	Input/ Output
PSI#	AE6	CMOS	Output
PWRGOOD	D6	CMOS	Input
REQ[0]#	K3	Source Synch	Input/ Output
REQ[1]#	H2	Source Synch	Input/ Output
REQ[2]#	K2	Source Synch	Input/ Output
REQ[3]#	J3	Source Synch	Input/ Output
REQ[4]#	L1	Source Synch	Input/ Output
RESET#	C1	Common Clock	Input
RS[0]#	F3	Common Clock	Input

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
RS[1]#	F4	Common Clock	Input
RS[2]#	G3	Common Clock	Input
RSVD	B2	Reserved	
RSVD	D2	Reserved	
RSVD	D3	Reserved	
RSVD	D22	Reserved	
RSVD	F6	Reserved	
RSVD	M4	Reserved	
RSVD	N5	Reserved	
RSVD	T2	Reserved	
RSVD	V3	Reserved	
SLP#	D7	CMOS	Input
SMI#	A3	CMOS	Input
STPCLK#	D5	CMOS	Input
TCK	AC5	CMOS	Input
TDI	AA6	CMOS	Input
TDO	AB3	Open Drain	Output
TEST1	C23	Test	
TEST2	D25	Test	
TEST3	C24	Test	
TEST4	AF26	Test	
TEST5	AF1	Test	
TEST6	A26	Test	
TEST7	C3	Test	
THERMTRIP #	C7	Open Drain	Output
THRMDA	A24	Power/ Other	
THRMDC	B25	Power/ Other	
TMS	AB5	CMOS	Input
TRDY#	G2	Common Clock	Input
TRST#	AB6	CMOS	Input
VCC	A7	Power/ Other	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
VCC	A9	Power/ Other	
VCC	A10	Power/ Other	
VCC	A12	Power/ Other	
VCC	A13	Power/ Other	
VCC	A15	Power/ Other	
VCC	A17	Power/ Other	
VCC	A18	Power/ Other	
VCC	A20	Power/ Other	
VCC	AA7	Power/ Other	
VCC	AA9	Power/ Other	
VCC	AA10	Power/ Other	
VCC	AA12	Power/ Other	
VCC	AA13	Power/ Other	
VCC	AA15	Power/ Other	
VCC	AA17	Power/ Other	
VCC	AA18	Power/ Other	
VCC	AA20	Power/ Other	
VCC	AB7	Power/ Other	
VCC	AB9	Power/ Other	
VCC	AB10	Power/ Other	
VCC	AB12	Power/ Other	
VCC	AB14	Power/ Other	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
VCC	AB15	Power/ Other	
VCC	AB17	Power/ Other	
VCC	AB18	Power/ Other	
VCC	AB20	Power/ Other	
VCC	AC7	Power/ Other	
VCC	AC9	Power/ Other	
VCC	AC10	Power/ Other	
VCC	AC12	Power/ Other	
VCC	AC13	Power/ Other	
VCC	AC15	Power/ Other	
VCC	AC17	Power/ Other	
VCC	AC18	Power/ Other	
VCC	AD7	Power/ Other	
VCC	AD9	Power/ Other	
VCC	AD10	Power/ Other	
VCC	AD12	Power/ Other	
VCC	AD14	Power/ Other	
VCC	AD15	Power/ Other	
VCC	AD17	Power/ Other	
VCC	AD18	Power/ Other	
VCC	AE9	Power/ Other	
VCC	AE10	Power/ Other	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
VCC	AE12	Power/ Other	
VCC	AE13	Power/ Other	
VCC	AE15	Power/ Other	
VCC	AE17	Power/ Other	
VCC	AE18	Power/ Other	
VCC	AE20	Power/ Other	
VCC	AF9	Power/ Other	
VCC	AF10	Power/ Other	
VCC	AF12	Power/ Other	
VCC	AF14	Power/ Other	
VCC	AF15	Power/ Other	
VCC	AF17	Power/ Other	
VCC	AF18	Power/ Other	
VCC	AF20	Power/ Other	
VCC	B7	Power/ Other	
VCC	B9	Power/ Other	
VCC	B10	Power/ Other	
VCC	B12	Power/ Other	
VCC	B14	Power/ Other	
VCC	B15	Power/ Other	
VCC	B17	Power/ Other	
VCC	B18	Power/ Other	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
VCC	B20	Power/ Other	
VCC	C9	Power/ Other	
VCC	C10	Power/ Other	
VCC	C12	Power/ Other	
VCC	C13	Power/ Other	
VCC	C15	Power/ Other	
VCC	C17	Power/ Other	
VCC	C18	Power/ Other	
VCC	D9	Power/ Other	
VCC	D10	Power/ Other	
VCC	D12	Power/ Other	
VCC	D14	Power/ Other	
VCC	D15	Power/ Other	
VCC	D17	Power/ Other	
VCC	D18	Power/ Other	
VCC	E7	Power/ Other	
VCC	E9	Power/ Other	
VCC	E10	Power/ Other	
VCC	E12	Power/ Other	
VCC	E13	Power/ Other	
VCC	E15	Power/ Other	
VCC	E17	Power/ Other	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
VCC	E18	Power/ Other	
VCC	E20	Power/ Other	
VCC	F7	Power/ Other	
VCC	F9	Power/ Other	
VCC	F10	Power/ Other	
VCC	F12	Power/ Other	
VCC	F14	Power/ Other	
VCC	F15	Power/ Other	
VCC	F17	Power/ Other	
VCC	F18	Power/ Other	
VCC	F20	Power/ Other	
VCCA	B26	Power/ Other	
VCCA	C26	Power/ Other	
VCCP	G21	Power/ Other	
VCCP	J6	Power/ Other	
VCCP	J21	Power/ Other	
VCCP	K6	Power/ Other	
VCCP	K21	Power/ Other	
VCCP	M6	Power/ Other	
VCCP	M21	Power/ Other	
VCCP	N6	Power/ Other	
VCCP	N21	Power/ Other	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
VCCP	R6	Power/ Other	
VCCP	R21	Power/ Other	
VCCP	T6	Power/ Other	
VCCP	T21	Power/ Other	
VCCP	V6	Power/ Other	
VCCP	V21	Power/ Other	
VCCP	W21	Power/ Other	
VCCSENSE	AF7	Power/ Other	
VID[0]	AD6	CMOS	Output
VID[1]	AF5	CMOS	Output
VID[2]	AE5	CMOS	Output
VID[3]	AF4	CMOS	Output
VID[4]	AE3	CMOS	Output
VID[5]	AF3	CMOS	Output
VID[6]	AE2	CMOS	Output
VSS	A2	Power/ Other	
VSS	A4	Power/ Other	
VSS	A8	Power/ Other	
VSS	A11	Power/ Other	
VSS	A14	Power/ Other	
VSS	A16	Power/ Other	
VSS	A19	Power/ Other	
VSS	A23	Power/ Other	
VSS	A25	Power/ Other	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	AA2	Power/ Other	
VSS	AA5	Power/ Other	
VSS	AA8	Power/ other	
VSS	AA11	Power/ Other	
VSS	AA14	Power/ Other	
VSS	AA16	Power/ Other	
VSS	AA19	Power/ Other	
VSS	AA22	Power/ Other	
VSS	AA25	Power/ Other	
VSS	AB1	Power/ Other	
VSS	AB4	Power/ Other	
VSS	AB8	Power/ Other	
VSS	AB11	Power/ Other	
VSS	AB13	Power/ Other	
VSS	AB16	Power/ Other	
VSS	AB19	Power/ Other	
VSS	AB23	Power/ Other	
VSS	AB26	Power/ Other	
VSS	AC3	Power/ Other	
VSS	AC6	Power/ Other	
VSS	AC8	Power/ Other	
VSS	AC11	Power/ Other	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	AC14	Power/ Other	
VSS	AC16	Power/ Other	
VSS	AC19	Power/ Other	
VSS	AC21	Power/ Other	
VSS	AC24	Power/ Other	
VSS	AD2	Power/ Other	
VSS	AD5	Power/ Other	
VSS	AD8	Power/ Other	
VSS	AD11	Power/ Other	
VSS	AD13	Power/ Other	
VSS	AD16	Power/ Other	
VSS	AD19	Power/ Other	
VSS	AD22	Power/ Other	
VSS	AD25	Power/ Other	
VSS	AE1	Power/ Other	
VSS	AE4	Power/ Other	
VSS	AE8	Power/ Other	
VSS	AE11	Power/ Other	
VSS	AE14	Power/ Other	
VSS	AE16	Power/ Other	
VSS	AE19	Power/ Other	
VSS	AE23	Power/ Other	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	AE26	Power/ Other	
VSS	AF2	Power/ Other	
VSS	AF6	Power/ Other	
VSS	AF8	Power/ Other	
VSS	AF11	Power/ Other	
VSS	AF13	Power/ Other	
VSS	AF16	Power/ Other	
VSS	AF19	Power/ Other	
VSS	AF21	Power/ Other	
VSS	AF25	Power/ Other	
VSS	B6	Power/ Other	
VSS	B8	Power/ Other	
VSS	B11	Power/ Other	
VSS	B13	Power/ Other	
VSS	B16	Power/ Other	
VSS	B19	Power/ Other	
VSS	B21	Power/ Other	
VSS	B24	Power/ Other	
VSS	C2	Power/ Other	
VSS	C5	Power/ Other	
VSS	C8	Power/ Other	
VSS	C11	Power/ Other	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	C14	Power/ Other	
VSS	C16	Power/ Other	
VSS	C19	Power/ Other	
VSS	C22	Power/ Other	
VSS	C25	Power/ Other	
VSS	D1	Power/ Other	
VSS	D4	Power/ Other	
VSS	D8	Power/ Other	
VSS	D11	Power/ Other	
VSS	D13	Power/ Other	
VSS	D16	Power/ Other	
VSS	D19	Power/ Other	
VSS	D23	Power/ Other	
VSS	D26	Power/ Other	
VSS	E3	Power/ Other	
VSS	E6	Power/ Other	
VSS	E8	Power/ Other	
VSS	E11	Power/ Other	
VSS	E14	Power/ Other	
VSS	E16	Power/ Other	
VSS	E19	Power/ Other	
VSS	E21	Power/ Other	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	E24	Power/ Other	
VSS	F2	Power/ Other	
VSS	F5	Power/ Other	
VSS	F8	Power/ Other	
VSS	F11	Power/ Other	
VSS	F13	Power/ Other	
VSS	F16	Power/ Other	
VSS	F19	Power/ Other	
VSS	F22	Power/ Other	
VSS	F25	Power/ Other	
VSS	G1	Power/ Other	
VSS	G4	Power/ Other	
VSS	G23	Power/ Other	
VSS	G26	Power/ Other	
VSS	H3	Power/ Other	
VSS	H6	Power/ Other	
VSS	H21	Power/ Other	
VSS	H24	Power/ Other	
VSS	J2	Power/ Other	
VSS	J5	Power/ Other	
VSS	J22	Power/ Other	
VSS	J25	Power/ Other	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	K1	Power/ Other	
VSS	K4	Power/ Other	
VSS	K23	Power/ Other	
VSS	K26	Power/ Other	
VSS	L3	Power/ Other	
VSS	L6	Power/ Other	
VSS	L21	Power/ Other	
VSS	L24	Power/ Other	
VSS	M2	Power/ Other	
VSS	M5	Power/ Other	
VSS	M22	Power/ Other	
VSS	M25	Power/ Other	
VSS	N1	Power/ Other	
VSS	N4	Power/ Other	
VSS	N23	Power/ Other	
VSS	N26	Power/ Other	
VSS	P3	Power/ Other	
VSS	P6	Power/ Other	
VSS	P21	Power/ Other	
VSS	P24	Power/ Other	
VSS	R2	Power/ Other	
VSS	R5	Power/ Other	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	R22	Power/ Other	
VSS	R25	Power/ Other	
VSS	T1	Power/ Other	
VSS	T4	Power/ Other	
VSS	T23	Power/ Other	
VSS	T26	Power/ Other	
VSS	U3	Power/ Other	
VSS	U6	Power/ Other	
VSS	U21	Power/ Other	
VSS	U24	Power/ Other	
VSS	V2	Power/ Other	
VSS	V5	Power/ Other	
VSS	V22	Power/ Other	
VSS	V25	Power/ Other	
VSS	W1	Power/ Other	
VSS	W4	Power/ Other	
VSS	W23	Power/ Other	
VSS	W26	Power/ Other	
VSS	Y3	Power/ Other	
VSS	Y6	Power/ Other	

Table 16. Pin Name Listing

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	Y21	Power/ Other	
VSS	Y24	Power/ Other	
VSSSENSE	AE7	Power/ Other	Output

Table 17. Pin # Listing

Pin #	Pin Name	Signal Buffer Type	Direction
A2	VSS	Power/Other	
A3	SMI#	CMOS	Input
A4	VSS	Power/Other	
A5	FERR#	Open Drain	Output
A6	A20M#	CMOS	Input
A7	VCC	Power/Other	
A8	VSS	Power/Other	
A9	VCC	Power/Other	
A10	VCC	Power/Other	
A11	VSS	Power/Other	
A12	VCC	Power/Other	
A13	VCC	Power/Other	
A14	VSS	Power/Other	
A15	VCC	Power/Other	
A16	VSS	Power/Other	
A17	VCC	Power/Other	
A18	VCC	Power/Other	
A19	VSS	Power/Other	
A20	VCC	Power/Other	
A21	BCLK[1]	Bus Clock	Input
A22	BCLK[0]	Bus Clock	Input
A23	VSS	Power/Other	
A24	THRMDA	Power/Other	
A25	VSS	Power/Other	
A26	TEST6	Test	
AA1	COMP[2]	Power/Other	Input/ Output
AA2	VSS	Power/Other	
AA3	A[35]#	Source Synch	Input/ Output
AA4	A[33]#	Source Synch	Input/ Output
AA5	VSS	Power/Other	
AA6	TDI	CMOS	Input
AA7	VCC	Power/Other	
AA8	VSS	Power/other	
AA9	VCC	Power/Other	
AA10	VCC	Power/Other	
AA11	VSS	Power/Other	
AA12	VCC	Power/Other	

Table 17. Pin # Listing

Pin #	Pin Name	Signal Buffer Type	Direction
AA13	VCC	Power/Other	
AA14	VSS	Power/Other	
AA15	VCC	Power/Other	
AA16	VSS	Power/Other	
AA17	VCC	Power/Other	
AA18	VCC	Power/Other	
AA19	VSS	Power/Other	
AA20	VCC	Power/Other	
AA21	D[50]#	Source Synch	Input/ Output
AA22	VSS	Power/Other	
AA23	D[45]#	Source Synch	Input/ Output
AA24	D[46]#	Source Synch	Input/ Output
AA25	VSS	Power/Other	
AA26	DSTBP[2]#	Source Synch	Input/ Output
AB1	VSS	Power/Other	
AB2	A[34]#	Source Synch	Input/ Output
AB3	TDO	Open Drain	Output
AB4	VSS	Power/Other	
AB5	TMS	CMOS	Input
AB6	TRST#	CMOS	Input
AB7	VCC	Power/Other	
AB8	VSS	Power/Other	
AB9	VCC	Power/Other	
AB10	VCC	Power/Other	
AB11	VSS	Power/Other	
AB12	VCC	Power/Other	
AB13	VSS	Power/Other	
AB14	VCC	Power/Other	
AB15	VCC	Power/Other	
AB16	VSS	Power/Other	
AB17	VCC	Power/Other	
AB18	VCC	Power/Other	
AB19	VSS	Power/Other	
AB20	VCC	Power/Other	
AB21	D[52]#	Source Synch	Input/ Output

Table 17. Pin # Listing

Pin #	Pin Name	Signal Buffer Type	Direction
AB22	D[51]#	Source Synch	Input/ Output
AB23	VSS	Power/Other	
AB24	D[33]#	Source Synch	Input/ Output
AB25	D[47]#	Source Synch	Input/ Output
AB26	VSS	Power/Other	
AC1	PREQ#	Common Clock	Input
AC2	PRDY#	Common Clock	Output
AC3	VSS	Power/Other	
AC4	BPM[3]#	Common Clock	Input/ Output
AC5	TCK	CMOS	Input
AC6	VSS	Power/Other	
AC7	VCC	Power/Other	
AC8	VSS	Power/Other	
AC9	VCC	Power/Other	
AC10	VCC	Power/Other	
AC11	VSS	Power/Other	
AC12	VCC	Power/Other	
AC13	VCC	Power/Other	
AC14	VSS	Power/Other	
AC15	VCC	Power/Other	
AC16	VSS	Power/Other	
AC17	VCC	Power/Other	
AC18	VCC	Power/Other	
AC19	VSS	Power/Other	
AC20	DINV[3]#	Source Synch	Input/ Output
AC21	VSS	Power/Other	
AC22	D[60]#	Source Synch	Input/ Output
AC23	D[63]#	Source Synch	Input/ Output
AC24	VSS	Power/Other	
AC25	D[57]#	Source Synch	Input/ Output
AC26	D[53]#	Source Synch	Input/ Output
AD1	BPM[2]#	Common Clock	Output
AD2	VSS	Power/Other	

Table 17. Pin # Listing

Pin #	Pin Name	Signal Buffer Type	Direction
AD3	BPM[1]#	Common Clock	Output
AD4	BPM[0]#	Common Clock	Input/ Output
AD5	VSS	Power/Other	
AD6	VID[0]	CMOS	Output
AD7	VCC	Power/Other	
AD8	VSS	Power/Other	
AD9	VCC	Power/Other	
AD10	VCC	Power/Other	
AD11	VSS	Power/Other	
AD12	VCC	Power/Other	
AD13	VSS	Power/Other	
AD14	VCC	Power/Other	
AD15	VCC	Power/Other	
AD16	VSS	Power/Other	
AD17	VCC	Power/Other	
AD18	VCC	Power/Other	
AD19	VSS	Power/Other	
AD20	D[54]#	Source Synch	Input/ Output
AD21	D[59]#	Source Synch	Input/ Output
AD22	VSS	Power/Other	
AD23	D[61]#	Source Synch	Input/ Output
AD24	D[49]#	Source Synch	Input/ Output
AD25	VSS	Power/Other	
AD26	GTLREF	Power/Other	Input
AE1	VSS	Power/Other	
AE2	VID[6]	CMOS	Output
AE3	VID[4]	CMOS	Output
AE4	VSS	Power/Other	
AE5	VID[2]	CMOS	Output
AE6	PSI#	CMOS	Output
AE7	VSSSENSE	Power/Other	Output
AE8	VSS	Power/Other	
AE9	VCC	Power/Other	
AE10	VCC	Power/Other	
AE11	VSS	Power/Other	
AE12	VCC	Power/Other	

Table 17. Pin # Listing

Pin #	Pin Name	Signal Buffer Type	Direction
AE13	VCC	Power/Other	
AE14	VSS	Power/Other	
AE15	VCC	Power/Other	
AE16	VSS	Power/Other	
AE17	VCC	Power/Other	
AE18	VCC	Power/Other	
AE19	VSS	Power/Other	
AE20	VCC	Power/Other	
AE21	D[58]#	Source Synch	Input/ Output
AE22	D[55]#	Source Synch	Input/ Output
AE23	VSS	Power/Other	
AE24	D[48]#	Source Synch	Input/ Output
AE25	DSTBN[3]#	Source Synch	Input/ Output
AE26	VSS	Power/Other	
AF1	TEST5	Test	
AF2	VSS	Power/Other	
AF3	VID[5]	CMOS	Output
AF4	VID[3]	CMOS	Output
AF5	VID[1]	CMOS	Output
AF6	VSS	Power/Other	
AF7	VCCSENSE	Power/Other	
AF8	VSS	Power/Other	
AF9	VCC	Power/Other	
AF10	VCC	Power/Other	
AF11	VSS	Power/Other	
AF12	VCC	Power/Other	
AF13	VSS	Power/Other	
AF14	VCC	Power/Other	
AF15	VCC	Power/Other	
AF16	VSS	Power/Other	
AF17	VCC	Power/Other	
AF18	VCC	Power/Other	
AF19	VSS	Power/Other	
AF20	VCC	Power/Other	
AF21	VSS	Power/Other	

Table 17. Pin # Listing

Pin #	Pin Name	Signal Buffer Type	Direction
AF22	D[62]#	Source Synch	Input/ Output
AF23	D[56]#	Source Synch	Input/ Output
AF24	DSTBP[3]#	Source Synch	Input/ Output
AF25	VSS	Power/Other	
AF26	TEST4	Test	
B2	RSVD	Reserved	
B3	INIT#	CMOS	Input
B4	LINT1	CMOS	Input
B5	DPSLP#	CMOS	Input
B6	VSS	Power/Other	
B7	VCC	Power/Other	
B8	VSS	Power/Other	
B9	VCC	Power/Other	
B10	VCC	Power/Other	
B11	VSS	Power/Other	
B12	VCC	Power/Other	
B13	VSS	Power/Other	
B14	VCC	Power/Other	
B15	VCC	Power/Other	
B16	VSS	Power/Other	
B17	VCC	Power/Other	
B18	VCC	Power/Other	
B19	VSS	Power/Other	
B20	VCC	Power/Other	
B21	VSS	Power/Other	
B22	BSEL[0]	CMOS	Output
B23	BSEL[1]	CMOS	Output
B24	VSS	Power/Other	
B25	THRMDC	Power/Other	
B26	VCCA	Power/Other	
C1	RESET#	Common Clock	Input
C2	VSS	Power/Other	
C3	TEST7	Test	
C4	IGNNE#	CMOS	Input
C5	VSS	Power/Other	
C6	LINT0	CMOS	Input
C7	THERMTRIP#	Open Drain	Output

Table 17. Pin # Listing

Pin #	Pin Name	Signal Buffer Type	Direction
C8	VSS	Power/Other	
C9	VCC	Power/Other	
C10	VCC	Power/Other	
C11	VSS	Power/Other	
C12	VCC	Power/Other	
C13	VCC	Power/Other	
C14	VSS	Power/Other	
C15	VCC	Power/Other	
C16	VSS	Power/Other	
C17	VCC	Power/Other	
C18	VCC	Power/Other	
C19	VSS	Power/Other	
C20	DBR#	CMOS	Output
C21	BSEL[2]	CMOS	Output
C22	VSS	Power/Other	
C23	TEST1	Test	
C24	TEST3	Test	
C25	VSS	Power/Other	
C26	VCCA	Power/Other	
D1	VSS	Power/Other	
D2	RSVD	Reserved	
D3	RSVD	Reserved	
D4	VSS	Power/Other	
D5	STPCLK#	CMOS	Input
D6	PWRGOOD	CMOS	Input
D7	SLP#	CMOS	Input
D8	VSS	Power/Other	
D9	VCC	Power/Other	
D10	VCC	Power/Other	
D11	VSS	Power/Other	
D12	VCC	Power/Other	
D13	VSS	Power/Other	
D14	VCC	Power/Other	
D15	VCC	Power/Other	
D16	VSS	Power/Other	
D17	VCC	Power/Other	
D18	VCC	Power/Other	
D19	VSS	Power/Other	
D20	IERR#	Open Drain	Output
D21	PROCHOT#	Open Drain	Input/Output
D22	RSVD	Reserved	
D23	VSS	Power/Other	
D24	DPWR#	Common Clock	Input/Output
D25	TEST2	Test	
D26	VSS	Power/Other	
E1	DBSY#	Common Clock	Input/Output
E2	BNR#	Common Clock	Input/Output
E3	VSS	Power/Other	
E4	HITM#	Common Clock	Input/Output
E5	DPRSTP#	CMOS	Input
E6	VSS	Power/Other	
E7	VCC	Power/Other	
E8	VSS	Power/Other	
E9	VCC	Power/Other	
E10	VCC	Power/Other	
E11	VSS	Power/Other	
E12	VCC	Power/Other	
E13	VCC	Power/Other	
E14	VSS	Power/Other	
E15	VCC	Power/Other	
E16	VSS	Power/Other	
E17	VCC	Power/Other	
E18	VCC	Power/Other	
E19	VSS	Power/Other	
E20	VCC	Power/Other	
E21	VSS	Power/Other	
E22	D[0]#	Source Synch	Input/Output
E23	D[7]#	Source Synch	Input/Output
E24	VSS	Power/Other	
E25	D[6]#	Source Synch	Input/Output
E26	D[2]#	Source Synch	Input/Output
F1	BR0#	Common Clock	Input/Output

Table 17. Pin # Listing

Pin #	Pin Name	Signal Buffer Type	Direction
F2	VSS	Power/Other	
F3	RS[0]#	Common Clock	Input
F4	RS[1]#	Common Clock	Input
F5	VSS	Power/Other	
F6	RSVD	Reserved	
F7	VCC	Power/Other	
F8	VSS	Power/Other	
F9	VCC	Power/Other	
F10	VCC	Power/Other	
F11	VSS	Power/Other	
F12	VCC	Power/Other	
F13	VSS	Power/Other	
F14	VCC	Power/Other	
F15	VCC	Power/Other	
F16	VSS	Power/Other	
F17	VCC	Power/Other	
F18	VCC	Power/Other	
F19	VSS	Power/Other	
F20	VCC	Power/Other	
F21	DRDY#	Common Clock	Input/ Output
F22	VSS	Power/Other	
F23	D[4]#	Source Synch	Input/ Output
F24	D[1]#	Source Synch	Input/ Output
F25	VSS	Power/Other	
F26	D[13]#	Source Synch	Input/ Output
G1	VSS	Power/Other	
G2	TRDY#	Common Clock	Input
G3	RS[2]#	Common Clock	Input
G4	VSS	Power/Other	
G5	BPRI#	Common Clock	Input
G6	HIT#	Common Clock	Input/ Output
G21	VCCP	Power/Other	
G22	D[3]#	Source Synch	Input/ Output
G23	VSS	Power/Other	
G24	D[9]#	Source Synch	Input/ Output

Table 17. Pin # Listing

Pin #	Pin Name	Signal Buffer Type	Direction
G25	D[5]#	Source Synch	Input/ Output
G26	VSS	Power/Other	
H1	ADS#	Common Clock	Input/ Output
H2	REQ[1]#	Source Synch	Input/ Output
H3	VSS	Power/Other	
H4	LOCK#	Common Clock	Input/ Output
H5	DEFER#	Common Clock	Input
H6	VSS	Power/Other	
H21	VSS	Power/Other	
H22	D[12]#	Source Synch	Input/ Output
H23	D[15]#	Source Synch	Input/ Output
H24	VSS	Power/Other	
H25	DINV[0]#	Source Synch	Input/ Output
H26	DSTBP[0]#	Source Synch	Input/ Output
J1	A[9]#	Source Synch	Input/ Output
J2	VSS	Power/Other	
J3	REQ[3]#	Source Synch	Input/ Output
J4	A[3]#	Source Synch	Input/ Output
J5	VSS	Power/Other	
J6	VCCP	Power/Other	
J21	VCCP	Power/Other	
J22	VSS	Power/Other	
J23	D[11]#	Source Synch	Input/ Output
J24	D[10]#	Source Synch	Input/ Output
J25	VSS	Power/Other	
J26	DSTBN[0]#	Source Synch	Input/ Output
K1	VSS	Power/Other	
K2	REQ[2]#	Source Synch	Input/ Output

Table 17. Pin # Listing

Pin #	Pin Name	Signal Buffer Type	Direction
K3	REQ[0]#	Source Synch	Input/ Output
K4	VSS	Power/Other	
K5	A[6]#	Source Synch	Input/ Output
K6	VCCP	Power/Other	
K21	VCCP	Power/Other	
K22	D[14]#	Source Synch	Input/ Output
K23	VSS	Power/Other	
K24	D[8]#	Source Synch	Input/ Output
K25	D[17]#	Source Synch	Input/ Output
K26	VSS	Power/Other	
L1	REQ[4]#	Source Synch	Input/ Output
L2	A[13]#	Source Synch	Input/ Output
L3	VSS	Power/Other	
L4	A[5]#	Source Synch	Input/ Output
L5	A[4]#	Source Synch	Input/ Output
L6	VSS	Power/Other	
L21	VSS	Power/Other	
L22	D[22]#	Source Synch	Input/ Output
L23	D[20]#	Source Synch	Input/ Output
L24	VSS	Power/Other	
L25	D[29]#	Source Synch	Input/ Output
L26	DSTBN[1]#	Source Synch	Input/ Output
M1	ADSTB[0]#	Source Synch	Input/ Output
M2	VSS	Power/Other	
M3	A[7]#	Source Synch	Input/ Output
M4	RSVD	Reserved	
M5	VSS	Power/Other	
M6	VCCP	Power/Other	
M21	VCCP	Power/Other	

Table 17. Pin # Listing

Pin #	Pin Name	Signal Buffer Type	Direction
M22	VSS	Power/Other	
M23	D[23]#	Source Synch	Input/ Output
M24	D[21]#	Source Synch	Input/ Output
M25	VSS	Power/Other	
M26	DSTBP[1]#	Source Synch	Input/ Output
N1	VSS	Power/Other	
N2	A[8]#	Source Synch	Input/ Output
N3	A[10]#	Source Synch	Input/ Output
N4	VSS	Power/Other	
N5	RSVD	Reserved	
N6	VCCP	Power/Other	
N21	VCCP	Power/Other	
N22	D[16]#	Source Synch	Input/ Output
N23	VSS	Power/Other	
N24	DINV[1]#	Source Synch	Input/ Output
N25	D[31]#	Source Synch	Input/ Output
N26	VSS	Power/Other	
P1	A[15]#	Source Synch	Input/ Output
P2	A[12]#	Source Synch	Input/ Output
P3	VSS	Power/Other	
P4	A[14]#	Source Synch	Input/ Output
P5	A[11]#	Source Synch	Input/ Output
P6	VSS	Power/Other	
P21	VSS	Power/Other	
P22	D[26]#	Source Synch	Input/ Output
P23	D[25]#	Source Synch	Input/ Output
P24	VSS	Power/Other	
P25	D[24]#	Source Synch	Input/ Output

Table 17. Pin # Listing

Pin #	Pin Name	Signal Buffer Type	Direction
P26	D[18]#	Source Synch	Input/ Output
R1	A[16]#	Source Synch	Input/ Output
R2	VSS	Power/Other	
R3	A[19]#	Source Synch	Input/ Output
R4	A[24]#	Source Synch	Input/ Output
R5	VSS	Power/Other	
R6	VCCP	Power/Other	
R21	VCCP	Power/Other	
R22	VSS	Power/Other	
R23	D[19]#	Source Synch	Input/ Output
R24	D[28]#	Source Synch	Input/ Output
R25	VSS	Power/Other	
R26	COMP[0]	Power/Other	Input/ Output
T1	VSS	Power/Other	
T2	RSVD	Reserved	
T3	A[26]#	Source Synch	Input/ Output
T4	VSS	Power/Other	
T5	A[25]#	Source Synch	Input/ Output
T6	VCCP	Power/Other	
T21	VCCP	Power/Other	
T22	D[37]#	Source Synch	Input/ Output
T23	VSS	Power/Other	
T24	D[27]#	Source Synch	Input/ Output
T25	D[30]#	Source Synch	Input/ Output
T26	VSS	Power/Other	
U1	A[23]#	Source Synch	Input/ Output
U2	A[30]#	Source Synch	Input/ Output
U3	VSS	Power/Other	
U4	A[21]#	Source Synch	Input/ Output

Table 17. Pin # Listing

Pin #	Pin Name	Signal Buffer Type	Direction
U5	A[18]#	Source Synch	Input/ Output
U6	VSS	Power/Other	
U21	VSS	Power/Other	
U22	DINV[2]#	Source Synch	Input/ Output
U23	D[39]#	Source Synch	Input/ Output
U24	VSS	Power/Other	
U25	D[38]#	Source Synch	Input/ Output
U26	COMP[1]	Power/Other	Input/ Output
V1	ADSTB[1]#	Source Synch	Input/ Output
V2	VSS	Power/Other	
V3	RSVD	Reserved	
V4	A[31]#	Source Synch	Input/ Output
V5	VSS	Power/Other	
V6	VCCP	Power/Other	
V21	VCCP	Power/Other	
V22	VSS	Power/Other	
V23	D[36]#	Source Synch	Input/ Output
V24	D[34]#	Source Synch	Input/ Output
V25	VSS	Power/Other	
V26	D[35]#	Source Synch	Input/ Output
W1	VSS	Power/Other	
W2	A[27]#	Source Synch	Input/ Output
W3	A[32]#	Source Synch	Input/ Output
W4	VSS	Power/Other	
W5	A[28]#	Source Synch	Input/ Output
W6	A[20]#	Source Synch	Input/ Output
W21	VCCP	Power/Other	
W22	D[41]#	Source Synch	Input/ Output
W23	VSS	Power/Other	

Table 17. Pin # Listing

Pin #	Pin Name	Signal Buffer Type	Direction
W24	D[43]#	Source Synch	Input/ Output
W25	D[44]#	Source Synch	Input/ Output
W26	VSS	Power/Other	
Y1	COMP[3]	Power/Other	Input/ Output
Y2	A[17]#	Source Synch	Input/ Output
Y3	VSS	Power/Other	
Y4	A[29]#	Source Synch	Input/ Output
Y5	A[22]#	Source Synch	Input/ Output
Y6	VSS	Power/Other	
Y21	VSS	Power/Other	
Y22	D[32]#	Source Synch	Input/ Output
Y23	D[42]#	Source Synch	Input/ Output
Y24	VSS	Power/Other	
Y25	D[40]#	Source Synch	Input/ Output
Y26	DSTBN[2]#	Source Synch	Input/ Output

Figure 18. Intel Core 2 Duo Mobile Processor in SFF Package Top View Upper Left Side

	BD	BC	BB	BA	AY	AW	AV	AU	AT	AR	AP	AN	AM	AL	AK	AJ	AH	AG	AF	AE	AD	AC
1				VSS		VSS		TDO		A[35]#		A[17]#		A[31]#		A[30]#		A[19]#		COMP[2]		A[16]#
2			VSS		BPM[3]#		PREQ#		A[22]#		A[34]#		A[32]#		A[21]#		A[23]#		COMP[3]		A[11]#	
3		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
4	VSS		VID[5]		VID[6]		TCK		A[20]#		A[28]#		A[27]#		A[18]#		A[26]#		A[24]#		A[12]#	
5		VID[4]		BPM[2]#		TMS		A[33]#		A[29]#		ADSTB[1]#		RSVD04		A[25]#		RSVD03		A[14]#		A[10]#
6	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	
7		VID[1]		BPM[1]#		TDI		VSS		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP
8	VID[0]		VID[3]		BPM[0]#		TRST#		VSS		VSS		VSS		VSS		VSS		VSS		VSS	
9		VSS		VSS		VSS		VSS		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP
10	PSI#		VID[2]		TEST5		PRDY#		VSS		VCCP		VSS		VCCP		VSS		VCCP		VSS	
11		VSS		VSS		VSS		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP
12	VCCSENSE		VSS		VSS		VSS		VSS		VCCP		VSS		VCCP		VSS		VCCP		VSS	
13		VSSSENSE		VSS		VSS		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP
14	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCCP		VCCP		VCCP		VCCP	
15		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
16	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
17		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
18	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
19		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
20	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
21		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
22	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	

Figure 19. Intel Core 2 Duo Mobile Processor in SFF Package Top View Upper Right Side

	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1		A[7]#		A[5]#		REQ[2]#		REQ[0]#		LOCK#		TRDY#		DBSY#		VSS		VSS				
2	A[15]#		RSVD02		RSVD01		A[9]#		A[3]#		BR0#		RS[0]#		HIT#		HITM#		VSS			
3		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		
4	A[8]#		ADSTB[0]#		A[4]#		A[6]#		REQ[3]#		ADS#		RS[2]#		RS[1]#		RSVD06		FERR#		VSS	
5		A[13]#		REQ[4]#		VSS		REQ[1]#		DEFER#		BPRI#		BNR#		RESET#		SMI#		LINT1		VSS
6	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	
7		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		DBR#		DPRSTP#		PWRGOOD		A20M#		VSS
8	VSS		VSS		VSS		VSS		VSS		VSS		VSS		RSVD07		STPCLK#		INIT#		DPSLP#	
9		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		RSVD05		VSS		VSS		LINT0		VSS
10	VCCP		VSS		VCCP		VSS		VCCP		VSS		VCCP		VSS		IGNNE#		SLP#		THERMTRIP#	
11		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VSS		VSS
12	VCCP		VSS		VCCP		VSS		VCCP		VSS		VCCP		VCCP		VCCP		VCCP		VCCP	
13		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP
14	VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP	
15		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
16	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
17		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
18	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
19		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
20	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
21		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
22	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	

Figure 20. Intel Core 2 Duo Mobile Processor in SFF Package Top View Lower Left Side

	BD	BC	BB	BA	AY	AW	AV	AU	AT	AR	AP	AN	AM	AL	AK	AJ	AH	AG	AF	AE	AD	AC
23		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
24	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
25		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
26	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
27		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
28	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
29		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
30	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
31		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
32	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
33		VSS		VSS		VSS		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC
34	THRM DC		THRM DA		VSS		VSS		VCC		VSS		VSS		VSS		VSS		VSS		VSS	
35		D[58]#		D[62]#		VSS		VSS		VSS		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP
36	VSS		VSS		D[56]#		VSS		VSS		VCCP		VSS		VCCP		VSS		VCCP		VSS	
37		DINV[3]#		D[54]#		VSS		VSS		VSS		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP
38	VSS		D[55]#		DSTBP[3]#		D[48]#		VSS		VCCP		VSS		VCCP		VSS		VCCP		VSS	
39		D[59]#		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
40	VSS		D[61]#		DSTBN[3]#		D[50]#		D[57]#		D[45]#		D[42]#		D[43]#		D[34]#		D[35]#		D[26]#	
41		VSS		D[60]#		D[52]#		D[51]#		D[53]#		D[46]#		D[47]#		DINV[2]#		D[37]#		TEST4		D[27]#
42			VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	
43				VSS		GTLREF		D[63]#		D[33]#		D[41]#		DSTBP[2]#		D[36]#		D[44]#		COMP[0]		TEST6
44					VSS		VSS		D[49]#		D[32]#		D[40]#		DSTBN[2]#		D[39]#		D[38]#		COMP[1]	

Figure 21. Intel Core 2 Duo Mobile Processor in SFF Package Top View Lower Right Side

	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
23		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
24	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
25		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
26	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
27		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
28	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
29		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
30	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
31		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
32	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCCP		VCCP	
33		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCCP		VCCP		VCCP
34	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VCCP		VCCA		VCCA	
35		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		BCLK[1]		BCLK[0]
36	VCCP		VSS		VCCP		VSS		VCCP		VSS		VCCP		VCCP		VCCP		VSS		VSS	
37		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VSS		TEST1		BSEL[1]		BSEL[0]
38	VCCP		VSS		VCCP		VSS		VCCP		VSS		VCCP		VSS		DRDY#		PROCHOT#		BSEL[2]	
39		VSS		VSS		VSS		VSS		VSS		VSS		VSS		D[6]#		VSS		VSS		VSS
40	D[25]#		D[29]#		D[17]#		D[11]#		DINV[0]#		D[12]#		DSTBN[0]#		D[4]#		D[0]#		TEST2		IERR#	
41		D[24]#		D[21]#		D[23]#		D[20]#		D[10]#		D[8]#		DSTBP[0]#		D[13]#		D[7]#		DPWR#		VSS
42	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	
43		D[28]#		DSTBP[1]#		DSTBN[1]#		DINV[1]#		D[22]#		D[15]#		D[3]#		D[1]#		D[2]#		TEST3		
44	D[19]#		D[30]#		D[18]#		D[31]#		D[16]#		D[14]#		D[9]#		D[5]#		VSS		VSS			

Table 18.Intel Core 2 Duo Mobile Processor in SFF Package Listing by Ball Name

Signal Name	Ball Number
A[3]#	P2
A[4]#	V4
A[5]#	W1
A[6]#	T4
A[7]#	AA1
A[8]#	AB4
A[9]#	T2
A[10]#	AC5
A[11]#	AD2
A[12]#	AD4
A[13]#	AA5
A[14]#	AE5
A[15]#	AB2
A[16]#	AC1
A[17]#	AN1
A[18]#	AK4
A[19]#	AG1
A[20]#	AT4
A[21]#	AK2
A[22]#	AT2
A[23]#	AH2
A[24]#	AF4
A[25]#	AJ5
A[26]#	AH4
A[27]#	AM4
A[28]#	AP4
A[29]#	AR5
A[30]#	AJ1
A[31]#	AL1
A[32]#	AM2
A[33]#	AU5
A[34]#	AP2
A[35]#	AR1
ADS#	C7
ADSTB[0]#	M4
ADSTB[1]#	Y4

Signal Name	Ball Number
BCLK[0]	AN5
BCLK[1]	A35
BNR#	C35
BPM[0]#	J5
BPM[1]#	AY8
BPM[2]#	BA7
BPM[3]#	BA5
BPRI#	AY2
BR0#	L5
BSEL[0]	M2
BSEL[1]	A37
BSEL[2]	C37
COMP[0]	B38
COMP[1]	AE43
COMP[2]	AD44
COMP[3]	AE1
D[0]#	AF2
D[1]#	F40
D[2]#	G43
D[3]#	E43
D[4]#	J43
D[5]#	H40
D[6]#	H44
D[7]#	G39
D[8]#	E41
D[9]#	L41
D[10]#	K44
D[11]#	N41
D[12]#	T40
D[13]#	M40
D[14]#	M44
D[15]#	L43
D[16]#	P44
D[17]#	V40
D[18]#	V44
D[19]#	AB44

Signal Name	Ball Number
D[20]#	R41
D[21]#	W41
D[22]#	N43
D[23]#	U41
D[24]#	AA41
D[25]#	AB40
D[26]#	AD40
D[27]#	AC41
D[28]#	AA43
D[29]#	Y40
D[30]#	Y44
D[31]#	T44
D[32]#	AP44
D[33]#	AR43
D[34]#	AH40
D[35]#	AF40
D[36]#	AJ43
D[37]#	AG41
D[38]#	AF44
D[39]#	AH44
D[40]#	AM44
D[41]#	AN43
D[42]#	AM40
D[43]#	AK40
D[44]#	AG43
D[45]#	AP40
D[46]#	AN41
D[47]#	AL41
D[48]#	AV38
D[49]#	AT44
D[50]#	AV40
D[51]#	AU41
D[52]#	AW41
D[53]#	AR41
D[54]#	BA37
D[55]#	BB38

Table 18.Intel Core 2 Duo Mobile Processor in SFF Package Listing by Ball Name

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
D[56]#	AY36	PRDY#	AV10	TMS	AW5
D[57]#	AT40	PREQ#	AV2	TRDY#	L1
D[58]#	BC35	PROCHOT#	D38	TRST#	AV8
D[59]#	BC39	PSI#	BD10	VCC	AA33
D[60]#	BA41	PWRGOOD	E7	VCC	AB16
D[61]#	BB40	REQ[0]#	R1	VCC	AB18
D[62]#	BA35	REQ[1]#	R5	VCC	AB20
D[63]#	AU43	REQ[2]#	U1	VCC	AB22
DBR#	J7	REQ[3]#	P4	VCC	AB24
DBSY#	J1	REQ[4]#	W5	VCC	AB26
DEFER#	N5	RESET#	G5	VCC	AB28
DINV[0]#	P40	RS[0]#	K2	VCC	AB30
DINV[1]#	R43	RS[1]#	H4	VCC	AB32
DINV[2]#	AJ41	RS[2]#	K4	VCC	AC33
DINV[3]#	BC37	RSVD01	V2	VCC	AD16
DPRSTP#	G7	RSVD02	Y2	VCC	AD18
DPSLP#	B8	RSVD03	AG5	VCC	AD20
DPWR#	C41	RSVD04	AL5	VCC	AD22
DRDY#	F38	RSVD05	J9	VCC	AD24
DSTBN[0]#	K40	RSVD06	F4	VCC	AD26
DSTBN[1]#	U43	RSVD07	H8	VCC	AD28
DSTBN[2]#	AK44	SLP#	D10	VCC	AD30
DSTBN[3]#	AY40	SMI#	E5	VCC	AD32
DSTBP[0]#	J41	STPCLK#	F8	VCC	AE33
DSTBP[1]#	W43	TCK	AV4	VCC	AF16
DSTBP[2]#	AL43	TDI	AW7	VCC	AF18
DSTBP[3]#	AY38	TDO	AU1	VCC	AF20
FERR#	D4	TEST1	E37	VCC	AF22
GTLREF	AW43	TEST2	D40	VCC	AF24
HIT#	H2	TEST3	C43	VCC	AF26
HITM#	F2	TEST4	AE41	VCC	AF28
IERR#	B40	TEST5	AY10	VCC	AF30
IGNNE#	F10	TEST6	AC43	VCC	AF32
INIT#	D8	THERMTRIP#	B10	VCC	AG33
LINT0	C9	THRMDA	BB34	VCC	AH16
LINT1	C5	THRMDC	BD34	VCC	AH18
LOCK#	N1	THERMTRIP#	B10	VCC	AH20

Table 18. Intel Core 2 Duo Mobile Processor in SFF Package Listing by Ball Name

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
VCC	AH22	VCC	AP32	VCC	B22
VCC	AH24	VCC	AR33	VCC	B24
VCC	AH26	VCC	AT14	VCC	B26
VCC	AH28	VCC	AT16	VCC	B28
VCC	AH30	VCC	AT18	VCC	B30
VCC	AH32	VCC	AT20	VCC	BB14
VCC	AJ33	VCC	AT22	VCC	BB16
VCC	AK16	VCC	AT24	VCC	BB18
VCC	AK18	VCC	AT26	VCC	BB20
VCC	AK20	VCC	AT28	VCC	BB22
VCC	AK22	VCC	AT30	VCC	BB24
VCC	AK24	VCC	AT32	VCC	BB26
VCC	AK26	VCC	AT34	VCC	BB28
VCC	AK28	VCC	AU33	VCC	BB30
VCC	AK30	VCC	AV14	VCC	BB32
VCC	AK32	VCC	AV16	VCC	BD14
VCC	AL33	VCC	AV18	VCC	BD16
VCC	AM14	VCC	AV20	VCC	BD18
VCC	AM16	VCC	AV22	VCC	BD20
VCC	AM18	VCC	AV24	VCC	BD22
VCC	AM20	VCC	AV26	VCC	BD24
VCC	AM22	VCC	AV28	VCC	BD26
VCC	AM24	VCC	AV30	VCC	BD28
VCC	AM26	VCC	AV32	VCC	BD30
VCC	AM28	VCC	AY14	VCC	BD32
VCC	AM30	VCC	AY16	VCC	D16
VCC	AM32	VCC	AY18	VCC	D18
VCC	AN33	VCC	AY20	VCC	D20
VCC	AP14	VCC	AY22	VCC	D22
VCC	AP16	VCC	AY24	VCC	D24
VCC	AP18	VCC	AY26	VCC	D26
VCC	AP20	VCC	AY28	VCC	D28
VCC	AP22	VCC	AY30	VCC	D30
VCC	AP24	VCC	AY32	VCC	F16
VCC	AP26	VCC	B16	VCC	F18
VCC	AP28	VCC	B18	VCC	F20
VCC	AP30	VCC	B20	VCC	F22

Table 18. Intel Core 2 Duo Mobile Processor in SFF Package Listing by Ball Name

Signal Name	Ball Number
VCC	F24
VCC	F26
VCC	F28
VCC	F30
VCC	F32
VCC	G33
VCC	H16
VCC	H18
VCC	H20
VCC	H22
VCC	H24
VCC	H26
VCC	H28
VCC	H30
VCC	H32
VCC	J33
VCC	K16
VCC	K18
VCC	K20
VCC	K22
VCC	K24
VCC	K26
VCC	K28
VCC	K30
VCC	K32
VCC	L33
VCC	M16
VCC	M18
VCC	M20
VCC	M22
VCC	M24
VCC	M26
VCC	M28
VCC	M30
VCC	M32
VCC	N33
VCC	P16

Signal Name	Ball Number
VCC	P18
VCC	P20
VCC	P22
VCC	P24
VCC	P26
VCC	P28
VCC	P30
VCC	P32
VCC	R33
VCC	T16
VCC	T18
VCC	T20
VCC	T22
VCC	T24
VCC	T26
VCC	T28
VCC	T30
VCC	T32
VCC	U33
VCC	V16
VCC	V18
VCC	V20
VCC	V22
VCC	V24
VCC	V26
VCC	V28
VCC	V30
VCC	V32
VCC	W33
VCC	Y16
VCC	Y18
VCC	Y20
VCC	Y22
VCC	Y24
VCC	Y26
VCC	Y28
VCC	Y30

Signal Name	Ball Number
VCC	Y32
VCCA	B34
VCCA	D34
VCCP	A13
VCCP	A33
VCCP	AA7
VCCP	AA9
VCCP	AA11
VCCP	AA13
VCCP	AA35
VCCP	AA37
VCCP	AB10
VCCP	AB12
VCCP	AB14
VCCP	AB36
VCCP	AB38
VCCP	AC7
VCCP	AC9
VCCP	AC11
VCCP	AC13
VCCP	AC35
VCCP	AC37
VCCP	AD14
VCCP	AE7
VCCP	AE9
VCCP	AE11
VCCP	AE13
VCCP	AE35
VCCP	AE37
VCCP	AF10
VCCP	AF12
VCCP	AF14
VCCP	AF36
VCCP	AF38
VCCP	AG7
VCCP	AG9
VCCP	AG11

Table 18.Intel Core 2 Duo Mobile Processor in SFF Package Listing by Ball Name

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
VCCP	AG13	VCCP	B12	VCCP	M14
VCCP	AG35	VCCP	B14	VCCP	N7
VCCP	AG37	VCCP	B32	VCCP	N9
VCCP	AH14	VCCP	C13	VCCP	N11
VCCP	AJ7	VCCP	C33	VCCP	N13
VCCP	AJ9	VCCP	D12	VCCP	N35
VCCP	AJ11	VCCP	D14	VCCP	N37
VCCP	AJ13	VCCP	D32	VCCP	P10
VCCP	AJ35	VCCP	E11	VCCP	P12
VCCP	AJ37	VCCP	E13	VCCP	P14
VCCP	AK10	VCCP	E33	VCCP	P36
VCCP	AK12	VCCP	E35	VCCP	P38
VCCP	AK14	VCCP	F12	VCCP	R7
VCCP	AK36	VCCP	F14	VCCP	R9
VCCP	AK38	VCCP	F34	VCCP	R11
VCCP	AL7	VCCP	F36	VCCP	R13
VCCP	AL9	VCCP	G11	VCCP	R35
VCCP	AL11	VCCP	G13	VCCP	R37
VCCP	AL13	VCCP	G35	VCCP	T14
VCCP	AL35	VCCP	H12	VCCP	U7
VCCP	AL37	VCCP	H14	VCCP	U9
VCCP	AN7	VCCP	H36	VCCP	U11
VCCP	AN9	VCCP	J11	VCCP	U13
VCCP	AN11	VCCP	J13	VCCP	U35
VCCP	AN13	VCCP	J35	VCCP	U37
VCCP	AN35	VCCP	J37	VCCP	V10
VCCP	AN37	VCCP	K10	VCCP	V12
VCCP	AP10	VCCP	K12	VCCP	V14
VCCP	AP12	VCCP	K14	VCCP	V36
VCCP	AP36	VCCP	K36	VCCP	V38
VCCP	AP38	VCCP	K38	VCCP	W7
VCCP	AR7	VCCP	L7	VCCP	W9
VCCP	AR9	VCCP	L9	VCCP	W11
VCCP	AR11	VCCP	L11	VCCP	W13
VCCP	AR13	VCCP	L13	VCCP	W35
VCCP	AU11	VCCP	L35	VCCP	W37
VCCP	AU13	VCCP	L37	VCCP	Y14

Table 18.Intel Core 2 Duo Mobile Processor in SFF Package Listing by Ball Name

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
VCCSENSE	BD12	VSS	AB42	VSS	AG17
VID[0]	BD8	VSS	AC3	VSS	AG19
VID[1]	BC7	VSS	AC15	VSS	AG21
VID[2]	BB10	VSS	AC17	VSS	AG23
VID[3]	BB8	VSS	AC19	VSS	AG25
VID[4]	BC5	VSS	AC21	VSS	AG27
VID[5]	BB4	VSS	AC23	VSS	AG29
VID[6]	AY4	VSS	AC25	VSS	AG31
VSS	A5	VSS	AC27	VSS	AG39
VSS	A7	VSS	AC29	VSS	AH6
VSS	A9	VSS	AC31	VSS	AH8
VSS	A11	VSS	AC39	VSS	AH10
VSS	A15	VSS	AD6	VSS	AH12
VSS	A17	VSS	AD8	VSS	AH34
VSS	A19	VSS	AD10	VSS	AH36
VSS	A21	VSS	AD12	VSS	AH38
VSS	A23	VSS	AD34	VSS	AH42
VSS	A25	VSS	AD36	VSS	AJ3
VSS	A27	VSS	AD38	VSS	AJ15
VSS	A29	VSS	AD42	VSS	AJ17
VSS	A31	VSS	AE3	VSS	AJ19
VSS	A39	VSS	AE15	VSS	AJ21
VSS	A41	VSS	AE17	VSS	AJ23
VSS	AA3	VSS	AE19	VSS	AJ25
VSS	AA15	VSS	AE21	VSS	AJ27
VSS	AA17	VSS	AE23	VSS	AJ29
VSS	AA19	VSS	AE25	VSS	AJ31
VSS	AA21	VSS	AE27	VSS	AJ39
VSS	AA23	VSS	AE29	VSS	AK6
VSS	AA25	VSS	AE31	VSS	AK8
VSS	AA27	VSS	AE39	VSS	AK34
VSS	AA29	VSS	AF6	VSS	AK42
VSS	AA31	VSS	AF8	VSS	AL3
VSS	AA39	VSS	AF34	VSS	AL15
VSS	AB6	VSS	AF42	VSS	AL17
VSS	AB8	VSS	AG3	VSS	AL19
VSS	AB34	VSS	AG15	VSS	AL21

Table 18. Intel Core 2 Duo Mobile Processor in SFF Package Listing by Ball Name

Signal Name	Ball Number
VSS	AL23
VSS	AL25
VSS	AL27
VSS	AL29
VSS	AL31
VSS	AL39
VSS	AM6
VSS	AM8
VSS	AM10
VSS	AM12
VSS	AM34
VSS	AM36
VSS	AM38
VSS	AM42
VSS	AN3
VSS	AN15
VSS	AN17
VSS	AN19
VSS	AN21
VSS	AN23
VSS	AN25
VSS	AN27
VSS	AN29
VSS	AN31
VSS	AN39
VSS	AP6
VSS	AP8
VSS	AP34
VSS	AP42
VSS	AR3
VSS	AR15
VSS	AR17
VSS	AR19
VSS	AR21
VSS	AR23
VSS	AR25
VSS	AR27

Signal Name	Ball Number
VSS	AR29
VSS	AR31
VSS	AR35
VSS	AR37
VSS	AR39
VSS	AT6
VSS	AT8
VSS	AT10
VSS	AT12
VSS	AT36
VSS	AT38
VSS	AT42
VSS	AU3
VSS	AU7
VSS	AU9
VSS	AU15
VSS	AU17
VSS	AU19
VSS	AU21
VSS	AU23
VSS	AU25
VSS	AU27
VSS	AU29
VSS	AU31
VSS	AU35
VSS	AU37
VSS	AU39
VSS	AV6
VSS	AV12
VSS	AV34
VSS	AV36
VSS	AV42
VSS	AV44
VSS	AW1
VSS	AW3
VSS	AW9
VSS	AW11

Signal Name	Ball Number
VSS	AW13
VSS	AW15
VSS	AW17
VSS	AW19
VSS	AW21
VSS	AW23
VSS	AW25
VSS	AW27
VSS	AW29
VSS	AW31
VSS	AW33
VSS	AW35
VSS	AW37
VSS	AW39
VSS	AY6
VSS	AY12
VSS	AY34
VSS	AY42
VSS	AY44
VSS	B4
VSS	B6
VSS	B36
VSS	B42
VSS	BA1
VSS	BA3
VSS	BA9
VSS	BA11
VSS	BA13
VSS	BA15
VSS	BA17
VSS	BA19
VSS	BA21
VSS	BA23
VSS	BA25
VSS	BA27
VSS	BA29
VSS	BA31

Table 18.Intel Core 2 Duo Mobile Processor in SFF Package Listing by Ball Name

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
VSS	BA33	VSS	C31	VSS	H10
VSS	BA39	VSS	C39	VSS	H34
VSS	BA43	VSS	D2	VSS	H38
VSS	BB2	VSS	D6	VSS	H42
VSS	BB6	VSS	D36	VSS	J3
VSS	BB12	VSS	D42	VSS	J15
VSS	BB36	VSS	D44	VSS	J17
VSS	BB42	VSS	E1	VSS	J19
VSS	BC3	VSS	E3	VSS	J21
VSS	BC9	VSS	E9	VSS	J23
VSS	BC11	VSS	E15	VSS	J25
VSS	BC15	VSS	E17	VSS	J27
VSS	BC17	VSS	E19	VSS	J29
VSS	BC19	VSS	E21	VSS	J31
VSS	BC21	VSS	E23	VSS	J39
VSS	BC23	VSS	E25	VSS	K6
VSS	BC25	VSS	E27	VSS	K8
VSS	BC27	VSS	E29	VSS	K34
VSS	BC29	VSS	E31	VSS	K42
VSS	BC31	VSS	E39	VSS	L3
VSS	BC33	VSS	F6	VSS	L15
VSS	BC41	VSS	F42	VSS	L17
VSS	BD4	VSS	F44	VSS	L19
VSS	BD6	VSS	G1	VSS	L21
VSS	BD36	VSS	G3	VSS	L23
VSS	BD38	VSS	G9	VSS	L25
VSS	BD40	VSS	G15	VSS	L27
VSS	C3	VSS	G17	VSS	L29
VSS	C11	VSS	G19	VSS	L31
VSS	C15	VSS	G21	VSS	L39
VSS	C17	VSS	G23	VSS	M6
VSS	C19	VSS	G25	VSS	M8
VSS	C21	VSS	G27	VSS	M10
VSS	C23	VSS	G29	VSS	M12
VSS	C25	VSS	G31	VSS	M34
VSS	C27	VSS	G37	VSS	M36
VSS	C29	VSS	H6	VSS	M38

Table 18.Intel Core 2 Duo Mobile Processor in SFF Package Listing by Ball Name

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
VSS	M42	VSS	U15		
VSS	N3	VSS	U17		
VSS	N15	VSS	U19		
VSS	N17	VSS	U21		
VSS	N19	VSS	U23		
VSS	N21	VSS	U25		
VSS	N23	VSS	U27		
VSS	N25	VSS	U29		
VSS	N27	VSS	U31		
VSS	N29	VSS	U39		
VSS	N31	VSS	V6		
VSS	N39	VSS	V8		
VSS	P6	VSS	V34		
VSS	P8	VSS	V42		
VSS	P34	VSS	W3		
VSS	P42	VSS	W15		
VSS	R3	VSS	W17		
VSS	R15	VSS	W19		
VSS	R17	VSS	W21		
VSS	R19	VSS	W23		
VSS	R21	VSS	W25		
VSS	R23	VSS	W27		
VSS	R25	VSS	W29		
VSS	R27	VSS	W31		
VSS	R29	VSS	W39		
VSS	R31	VSS	Y6		
VSS	R39	VSS	Y8		
VSS	T6	VSS	Y10		
VSS	T8	VSS	Y12		
VSS	T10	VSS	Y34		
VSS	T12	VSS	Y36		
VSS	T34	VSS	Y38		
VSS	T36	VSS	Y42		
VSS	T38	VSSSENSE	BC13		
VSS	T42				
VSS	U3				
VSS	U5				

4.3 Alphabetical Signals Reference

Table 19. Signal Description (Sheet 1 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>A[35:3]#</td><td>Input/
Output</td><td>A[35:3]# (Address) define a 2^{36}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the processor FSB. A[35:3]# are source-synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps, which are sampled before RESET# is deasserted.</td></tr>
<tr><td>A20M#</td><td>Input</td><td>If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-MB boundary. Assertion of A20M# is only supported in real mode.
A20M# is an asynchronous signal. However, to ensure recognition of this signal following an input/output write instruction, it must be valid along with the TRDY# assertion of the corresponding input/output Write bus transaction.</td></tr>
<tr><td>ADS#</td><td>Input/
Output</td><td>ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.</td></tr>
<tr><td>ADSTB[1:0]#</td><td>Input/
Output</td><td>Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB[0]#</td></tr>
<tr><td>A[35:17]#</td><td>ADSTB[1]#</td></tr>
</table></td></tr>
<tr><td>BCLK[1:0]</td><td>Input</td><td>The differential pair BCLK (Bus Clock) determines the FSB frequency. All FSB agents must receive these signals to drive their outputs and latch their inputs.
All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.</td></tr>
<tr><td>BNR#</td><td>Input/
Output</td><td>BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.</td></tr>
<tr><td>BPM[2:1]#

BPM[3,0]#</td><td>Output

Input/
Output</td><td>BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all processor FSB agents.This includes debug or performance monitoring tools.</td></tr>
</table>

Table 19. Signal Description (Sheet 2 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BPRI#</td><td>Input</td><td>BPRI# (Bus Priority Request) is used to arbitrate for ownership of the FSB. It must connect the appropriate pins of both FSB agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.</td></tr>
<tr><td>BR0#</td><td>Input/
Output</td><td>BR0# is used by the processor to request the bus. The arbitration is done between the processor (Symmetric Agent) and GMCH (High Priority Agent).</td></tr>
<tr><td>BSEL[2:0]</td><td>Output</td><td>BSEL[2:0] (Bus Select) are used to select the processor input clock frequency. Table 3 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency.</td></tr>
<tr><td>COMP[3:0]</td><td>Analog</td><td>COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors.</td></tr>
<tr><td>D[63:0]#</td><td>Input/
Output</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the FSB agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer.
D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#.
Quad-Pumped Signal Groups
<table>
<tr><th>Data Group</th><th>DSTBN#/
DSTBP#</th><th>DINV#</th></tr>
<tr><td>D[15:0]#</td><td>0</td><td>0</td></tr>
<tr><td>D[31:16]#</td><td>1</td><td>1</td></tr>
<tr><td>D[47:32]#</td><td>2</td><td>2</td></tr>
<tr><td>D[63:48]#</td><td>3</td><td>3</td></tr>
</table>
Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.</td></tr>
<tr><td>DBR#</td><td>Output</td><td>DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.</td></tr>
<tr><td>DBSY#</td><td>Input/
Output</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the FSB to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both FSB agents.</td></tr>
</table>

Table 19. Signal Description (Sheet 3 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DEFER#</td><td>Input</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be ensured in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or input/ output agent. This signal must connect the appropriate pins of both FSB agents.</td></tr>
<tr><td>DINV[3:0]#</td><td>Input/ Output</td><td>DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle.
DINV[3:0]# Assignment To Data Bus
<table>
<tr><th>Bus Signal</th><th>Data Bus Signals</th></tr>
<tr><td>DINV[3]#</td><td>D[63:48]#</td></tr>
<tr><td>DINV[2]#</td><td>D[47:32]#</td></tr>
<tr><td>DINV[1]#</td><td>D[31:16]#</td></tr>
<tr><td>DINV[0]#</td><td>D[15:0]#</td></tr>
</table></td></tr>
<tr><td>DPRSTP#</td><td>Input</td><td>DPRSTP#, when asserted on the platform, causes the processor to transition from the Deep Sleep State to the Deeper Sleep state or Deep Power Down Technology (C6) state. To return to the Deep Sleep State, DPRSTP# must be deasserted. DPRSTP# is driven by the ICH9M.</td></tr>
<tr><td>DPSLP#</td><td>Input</td><td>DPSLP# when asserted on the platform causes the processor to transition from the Sleep State to the Deep Sleep state. To return to the Sleep State, DPSLP# must be deasserted. DPSLP# is driven by the ICH9M.</td></tr>
<tr><td>DPWR#</td><td>Input/ Output</td><td>DPWR# is a control signal used by the chipset to reduce power on the processor data bus input buffers. The processor drives this pin during dynamic FSB frequency switching.</td></tr>
<tr><td>DRDY#</td><td>Input/ Output</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both FSB agents.</td></tr>
<tr><td>DSTBN[3:0]#</td><td>Input/ Output</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DINV[0]#</td><td>DSTBN[0]#</td></tr>
<tr><td>D[31:16]#, DINV[1]#</td><td>DSTBN[1]#</td></tr>
<tr><td>D[47:32]#, DINV[2]#</td><td>DSTBN[2]#</td></tr>
<tr><td>D[63:48]#, DINV[3]#</td><td>DSTBN[3]#</td></tr>
</table></td></tr>
</table>

Table 19. Signal Description (Sheet 4 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DSTBP[3:0]#</td><td>Input/
Output</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DINV[0]#</td><td>DSTBP[0]#</td></tr>
<tr><td>D[31:16]#, DINV[1]#</td><td>DSTBP[1]#</td></tr>
<tr><td>D[47:32]#, DINV[2]#</td><td>DSTBP[2]#</td></tr>
<tr><td>D[63:48]#, DINV[3]#</td><td>DSTBP[3]#</td></tr>
</table></td></tr>
<tr><td>FERR#/PBE#</td><td>Output</td><td>FERR# (Floating-point Error)/PBE# (Pending Break Event) is a multiplexed signal and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel® 387 coprocessor, and is included for compatibility with systems using Microsoft MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event.
For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volumes 3A and 3B of the Intel® 64 and IA-32 Architectures Software Developer's Manuals and the Intel® Processor Identification and CPUID Instruction application note.</td></tr>
<tr><td>GTLREF</td><td>Input</td><td>GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.</td></tr>
<tr><td>HIT#</td><td>Input/
Output</td><td rowspan="2">HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall that can be continued by reasserting HIT# and HITM# together.</td></tr>
<tr><td>HITM#</td><td>Input/
Output</td></tr>
<tr><td>IERR#</td><td>Output</td><td>IERR# (Internal Error) is asserted by the processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.</td></tr>
<tr><td>IGNNE#</td><td>Input</td><td>IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a non-control floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set.
IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an input/output write instruction, it must be valid along with the TRDY# assertion of the corresponding input/output Write bus transaction.</td></tr>
</table>

Table 19. Signal Description (Sheet 5 of 8)

Name	Type	Description
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an input/output write instruction, it must be valid along with the TRDY# assertion of the corresponding input/output write bus transaction. INIT# must connect the appropriate pins of both FSB agents. If INIT# is sampled active on the active-to-inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST)
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward-compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the FSB, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the FSB throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	Output	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	Input	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	Input/ Output	As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system deasserts PROCHOT#. By default PROCHOT# is configured as an output. The processor must be enabled via the BIOS for PROCHOT# to be configured as bidirectional. This signal may require voltage translation on the motherboard.
PSI#	Output	Processor Power Status Indicator signal. This signal is asserted when the processor is both in the normal state (HFM to LFM) and in lower power states (Deep Sleep and Deeper Sleep).

Table 19. Signal Description (Sheet 6 of 8)

Name	Type	Description
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal remains low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, both FSB agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted. There is a 55 Ω (nominal) on die pull-up resistor on this signal.
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both FSB agents.
RSVD	Reserved/ No Connect	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued and the processor begins program execution from the SMM handler. If an SMI# is asserted during the deassertion of RESET#, then the processor will tristate its outputs.

Table 19. Signal Description (Sheet 7 of 8)

Name	Type	Description
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1, TEST2, TEST3, TEST4, TEST5, TEST6 TEST7	Input	Refer to the appropriate platform design guide for further TEST1, TEST2, TEST3, TEST4, TEST5, TEST6 and TEST7 termination requirements and implementation details.
THRMDA	Other	Thermal Diode Anode.
THRMDC	Other	Thermal Diode Cathode.
THERMTRIP#	Output	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125 °C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.
VCC	Input	Processor core power supply.
VSS	Input	Processor core ground node.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs.
VCCP	Input	Processor I/O Power Supply.

Table 19. Signal Description (Sheet 8 of 8)

Name	Type	Description
VCCSENSE	Output	VCCSENSE together with VSSSENSE are voltage feedback signals that control the 2.1 mΩ loadline at the processor die. It should be used to sense voltage near the silicon with little noise.
VID[6:0]	Output	VID[6:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V_{CC}). Unlike some previous generations of processors, these are CMOS signals that are driven by the processor. The voltage supply for these pins must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 2 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself.
VSSSENSE	Output	VSSSENSE together with VCCSENSE are voltage feedback signals that control the 2.1-mΩ loadline at the processor die. It should be used to sense ground near the silicon with little noise.

§

5 Thermal Specifications and Design Considerations

A complete thermal solution includes both component and system-level thermal management features. To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed so the processor remains within the minimum and maximum junction temperature (T_J) specifications at the corresponding thermal design power (TDP) value listed in the tables below

Caution: Operating the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system.

Table 20. Power Specifications for the Dual-Core Extreme Edition Processor

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	X9100	3.06 GHz & V_{CCHFM} 1.6 GHz & V_{CCLFM} 0.8 GHz & V_{CCSLFM}	44 29 20			W	1, 4, 5, 6
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power at V_{CCHFM} at V_{CCSLFM}		—	—	18.8 6.7	W	2, 5, 7
P_{SLP}	Sleep Power at V_{CCHFM} at V_{CCSLFM}		—	—	17.8 6.4	W	2, 5, 7
P_{DSLP}	Deep Sleep Power at V_{CCHFM} at V_{CCSLFM}		—	—	8.2 3.8	W	2, 5, 8
P_{DPRSLP}	Deeper Sleep Power		—	—	1.9	W	2, 8
P_{DC4}	Intel® Enhanced Deeper Sleep state Power		—	—	1.7	W	2, 8
P_{C6}	Intel® Deep Power Down Power		—	—	1.3	W	2, 8
T_J	Junction Temperature		0	—	105	°C	3, 4

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Processor TDP requirements in Intel Dynamic Acceleration Technology mode are lesser than TDP in HFM.
6. At Tj of 105 ^{o}C
7. At Tj of 50 ^{o}C
8. At Tj of 35 ^{o}C

Table 21. Power Specifications for the Dual-Core Standard Voltage Processor

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	T9900 T9800 T9600 T9550 T9400	3.06 GHz & V_{CCHFM} 2.93 GHz & V_{CCHFM} 2.80 GHz & V_{CCHFM} 2.66 GHz & V_{CCHFM} 2.53 GHz & V_{CCHFM} 1.6 GHz & V_{CCLFM} 0.8 GHz & V_{CCSLFM}	35 35 35 35 35 22 12			W	1, 4, 5, 6
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power at V_{CCHFM} at V_{CCSLFM}		—	—	13.9 5.0	W	2, 5, 7
P_{SLP}	Sleep Power at V_{CCHFM} at V_{CCSLFM}		—	—	13.1 4.8	W	2, 5, 7
P_{DSLP}	Deep Sleep Power at V_{CCHFM} at V_{CCSLFM}		—	—	5.5 2.2	W	2, 5, 8
P_{DPRSLP}	Deeper Sleep Power		—	—	1.7	W	2, 8
P_{DC4}	Intel® Enhanced Deeper Sleep state Power		—	—	1.3	W	2, 8
P_{C6}	Intel® Deep Power Down Power		—	—	0.3	W	2, 8
T_J	Junction Temperature		0	—	105	°C	3, 4

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Processor TDP requirements in Intel Dynamic Acceleration Technology mode are lesser than TDP in HFM.
6. At Tj of 105 °C
7. At Tj of 50 °C
8. At Tj of 35 °C

Table 22. Power Specifications for the Dual-Core Low Power Standard Voltage Processors (25W) in Standard Package

<table>
<tr><th>Symbol</th><th>Processor Number</th><th>Core Frequency & Voltage</th><th colspan="3">Thermal Design Power</th><th>Unit</th><th>Notes</th></tr>
<tr><td>TDP</td><td>P9700
P9600
P8800
P9500
P8700
P8600
P8400</td><td>2.8 GHz & V_{CCHFM}
2.667 GHz & V_{CCHFM}
2.667 GHz & V_{CCHFM}
2.53 GHz & V_{CCHFM}
2.53 GHz & V_{CCHFM}
2.4 GHz & V_{CCHFM}
2.267 GHz & V_{CCHFM}
1.6 GHz & V_{CCLFM}
0.8 GHz & V_{CCSLFM}</td><td colspan="3">25
25
25
25
25
25
25
20
11</td><td>W</td><td>1, 4, 5, 6</td></tr>
<tr><th>Symbol</th><th colspan="2">Parameter</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th><th>Notes</th></tr>
<tr><td>P_{AH},
P_{SGNT}</td><td colspan="2">Auto Halt, Stop Grant Power
at V_{CCHFM}
at V_{CCSLFM}</td><td>—</td><td>—</td><td>8.1
3.7</td><td>W</td><td>2, 5, 7</td></tr>
<tr><td>P_{SLP}</td><td colspan="2">Sleep Power
at V_{CCHFM}
at V_{CCSLFM}</td><td>—</td><td>—</td><td>7.3
3.5</td><td>W</td><td>2, 5, 7</td></tr>
<tr><td>P_{DSLP}</td><td colspan="2">Deep Sleep Power
at V_{CCHFM}
at V_{CCSLFM}</td><td>—</td><td>—</td><td>2.9
2.1</td><td>W</td><td>2, 5, 8</td></tr>
<tr><td>P_{DPRSLP}</td><td colspan="2">Deeper Sleep Power</td><td>—</td><td>—</td><td>1.0</td><td>W</td><td>2, 8</td></tr>
<tr><td>P_{DC4}</td><td colspan="2">Intel® Enhanced Deeper Sleep State Power</td><td>—</td><td>—</td><td>0.9</td><td>W</td><td>2, 8</td></tr>
<tr><td>P_{C6}</td><td colspan="2">Intel® Deep Power Down Power</td><td>—</td><td>—</td><td>0.3</td><td>W</td><td>2, 8</td></tr>
<tr><td>T_J</td><td colspan="2">Junction Temperature</td><td>0</td><td>—</td><td>105</td><td>°C</td><td>3, 4</td></tr>
</table>

NOTES:

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 6.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Processor TDP requirements in Intel Dynamic Acceleration Technology mode are lesser than TDP in HFM.
6. At Tj of 105 ^{o}C
7. At Tj of 50 ^{o}C
8. At Tj of 35 ^{o}C

Table 23. Power Specifications for the Dual-Core Power Optimized Performance (25 W) SFF Processors

<table>
<tr><th>Symbol</th><th>Processor Number</th><th>Core Frequency & Voltage</th><th colspan="3">Thermal Design Power</th><th>Unit</th><th>Notes</th></tr>
<tr><td>TDP</td><td>SP9600
SP9400
SP9300</td><td>2.53 GHz & HFM V_{CC}
2.4 GHz & HFM V_{CC}
2.26 GHz & HFM V_{CC}
1.6 GHz & Super LFM V_{CC}
0.8 GHz & Super LFM V_{CC}</td><td colspan="3">25
25
25
20
11</td><td>W</td><td>1, 4, 5, 6</td></tr>
<tr><th>Symbol</th><th colspan="2">Parameter</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th><th>Notes</th></tr>
<tr><td>P_{AH},
P_{SGNT}</td><td colspan="2">Auto Halt, Stop Grant Power
at V_{CCHFM}
at V_{CCSLFM}</td><td>—</td><td>—</td><td>8.3
3.3</td><td>W</td><td>2, 5, 7</td></tr>
<tr><td>P_{SLP}</td><td colspan="2">Sleep Power
at V_{CCHFM}
at V_{CCSLFM}</td><td>—</td><td>—</td><td>7.5
3.1</td><td>W</td><td>2, 5, 7</td></tr>
<tr><td>P_{DSLP}</td><td colspan="2">Deep Sleep Power
at V_{CCHFM}
at V_{CCSLFM}</td><td>—</td><td>—</td><td>2.9
1.8</td><td>W</td><td>2, 5, 8</td></tr>
<tr><td>P_{DPRSLP}</td><td colspan="2">Deeper Sleep Power</td><td>—</td><td>—</td><td>1.0</td><td>W</td><td>2, 8</td></tr>
<tr><td>P_{DC4}</td><td colspan="2">Intel® Enhanced Deeper Sleep State Power</td><td>—</td><td>—</td><td>0.9</td><td>W</td><td>2, 8</td></tr>
<tr><td>P_{C6}</td><td colspan="2">Intel® Deep Power Down Power</td><td>—</td><td>—</td><td>0.3</td><td>W</td><td>2, 8</td></tr>
<tr><td>T_J</td><td colspan="2">Junction Temperature</td><td>0</td><td>—</td><td>105</td><td>°C</td><td>3, 4</td></tr>
</table>

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Processor TDP requirements in Intel Dynamic Acceleration Technology mode are lesser than TDP in HFM.
6. At Tj of 105 °C
7. At Tj of 50 °C
8. At Tj of 35 °C

Table 24. Power Specifications fro the Dual-Core Low Voltage (LV) SFF Processors

<table>
<tr><th>Symbol</th><th>Processor Number</th><th>Core Frequency & Voltage</th><th colspan="3">Thermal Design Power</th><th>Unit</th><th>Notes</th></tr>
<tr><td>TDP</td><td>SL9600
SL9400
SL9300</td><td>2.13 GHz & HFM Vcc
1.86 GHz & HFM Vcc
1.6 GHz & HFM Vcc
1.6 GHz & Super LFM Vcc
0.8 GHz & Super LFM Vcc</td><td colspan="3">17
17
17
16.7
10</td><td>W</td><td>1, 4, 5, 6</td></tr>
<tr><th>Symbol</th><th colspan="2">Parameter</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th><th>Notes</th></tr>
<tr><td>P_{AH}, P_{SGNT}</td><td colspan="2">Auto Halt, Stop Grant Power
at V_{CCHFM}
at V_{CCSLFM}</td><td>—</td><td>—</td><td>6.3
3.0</td><td>W</td><td>2, 5, 7</td></tr>
<tr><td>P_{SLP}</td><td colspan="2">Sleep Power
at V_{CCHFM}
at V_{CCSLFM}</td><td>—</td><td>—</td><td>5.7
2.8</td><td>W</td><td>2, 5, 7</td></tr>
<tr><td>P_{DSLP}</td><td colspan="2">Deep Sleep Power
at V_{CCHFM}
at V_{CCSLFM}</td><td>—</td><td>—</td><td>2.6
1.3</td><td>W</td><td>2, 5, 8</td></tr>
<tr><td>P_{DPRSLP}</td><td colspan="2">Deeper Sleep Power</td><td>—</td><td>—</td><td>0.9</td><td>W</td><td>2, 8</td></tr>
<tr><td>P_{DC4}</td><td colspan="2">Intel® Enhanced Deeper Sleep State Power</td><td>—</td><td>—</td><td>0.8</td><td>W</td><td>2, 8</td></tr>
<tr><td>P_{C6}</td><td colspan="2">Intel® Deep Power Down Power</td><td>—</td><td>—</td><td>0.3</td><td>W</td><td>2, 8</td></tr>
<tr><td>T_J</td><td colspan="2">Junction Temperature</td><td>0</td><td>—</td><td>105</td><td>°C</td><td>3, 4</td></tr>
</table>

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Processor TDP requirements in Intel Dynamic Acceleration Technology mode are lesser than TDP in HFM.
6. At Tj of 105 °C
7. At Tj of 50 °C
8. At Tj of 35 °C

Table 25. Power Specifications for the Dual-Core Ultra-Low-Voltage (ULV) Processors

<table>
<tr><th>Symbol</th><th>Processor Number</th><th>Core Frequency & Voltage</th><th colspan="3">Thermal Design Power</th><th>Unit</th><th>Notes</th></tr>
<tr><td>TDP</td><td>SU9600
SU9400
SU9300</td><td>1.4 GHz & HFM V_{CC}
1.4 GHz & HFM V_{CC}
1.2GHz & HFM V_{CC}
1.2 GHz & Super LFM V_{CC}
0.8 GHz & Super LFM V_{CC}</td><td colspan="3">10
10
10
10
8</td><td>W</td><td>1, 4, 5, 6</td></tr>
<tr><th>Symbol</th><th colspan="2">Parameter</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th><th>Notes</th></tr>
<tr><td>P_{AH},
P_{SGNT}</td><td colspan="2">Auto Halt, Stop Grant Power
at V_{CCHFM}
at V_{CCSLFM}</td><td>—</td><td>—</td><td>2.9
1.6</td><td>W</td><td>2, 5, 7</td></tr>
<tr><td>P_{SLP}</td><td colspan="2">Sleep Power
at V_{CCHFM}
at V_{CCSLFM}</td><td>—</td><td>—</td><td>2.5
1.4</td><td>W</td><td>2, 5, 7</td></tr>
<tr><td>P_{DSLP}</td><td colspan="2">Deep Sleep Power
at V_{CCHFM}
at V_{CCSLFM}</td><td>—</td><td>—</td><td>1.3
0.9</td><td>W</td><td>2, 5, 8</td></tr>
<tr><td>P_{DPRSLP}</td><td colspan="2">Deeper Sleep Power</td><td>—</td><td>—</td><td>0.6</td><td>W</td><td>2, 8</td></tr>
<tr><td>P_{DC4}</td><td colspan="2">Intel® Enhanced Deeper Sleep state Power</td><td>—</td><td>—</td><td>0.4</td><td>W</td><td>2, 8</td></tr>
<tr><td>P_{C6}</td><td colspan="2">Intel® Deep Power Down Power</td><td>—</td><td>—</td><td>0.25</td><td>W</td><td>2, 8</td></tr>
<tr><td>T_J</td><td colspan="2">Junction Temperature</td><td>0</td><td>—</td><td>105</td><td>°C</td><td>3, 4</td></tr>
</table>

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor’s automatic mode is used to indicate that the maximum T_J has been reached.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Processor TDP requirements in Intel Dynamic Acceleration Technology mode are lesser than TDP in HFM.
6. At Tj of 105 °C
7. At Tj of 50 °C
8. At Tj of 35 °C

Table 26. Power Specifications for the Single-Core Ultra-Low-Voltage (5.5 W) SFF Processors

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	SU3500 SU3300	1.4 GHz & HFM V_{CC} 1.2 GHz & HFM V_{CC} 1.2 GHz & Super LFM V_{CC} 0.8 GHz & Super LFM V_{CC}	5.5 5.5 5.5 5			W	1, 4, 5, 6
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
$P_{AH,}$ P_{SGNT}	Auto Halt, Stop Grant Power at V_{CCHFM} at V_{CCSLFM}		—	—	2.1 1.4	W	2, 5, 7
P_{SLP}	Sleep Power at V_{CCHFM} at V_{CCSLFM}		—	—	1.8 1.2	W	2, 5, 7
P_{DSLP}	Deep Sleep Power at V_{CCHFM} at V_{CCSLFM}		—	—	0.7 0.6	W	2, 5, 8
P_{DPRSLP}	Deeper Sleep Power		—	—	0.4	W	2, 8
P_{DC4}	Intel® Enhanced Deeper Sleep state Power		—	—	0.3	W	2, 8
P_{C6}	Intel® Deep Power Down Power		—	—	0.2	W	2, 8
T_J	Junction Temperature		0	—	100	°C	3, 4

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Processor TDP requirements in Intel Dynamic Acceleration Technology mode are lesser than TDP in HFM.
6. At Tj of 100 °C
7. At Tj of 50 °C
8. At Tj of 35 °C

5.1 Monitoring Die Temperature

The processor incorporates three methods of monitoring die temperature:

- Thermal Diode
- Intel® Thermal Monitor
- Digital Thermal Sensor

5.1.1 Thermal Diode

Intel's processors utilize an SMBus thermal sensor to read back the voltage/current characteristics of a substrate PNP transistor. Since these characteristics are a function of temperature, these parameters can be used to calculate silicon temperature values. For older silicon process technologies, it is possible to simplify the voltage/current and temperature relationships by treating the substrate transistor as though it were a simple diffusion diode. In this case, the assumption is that the beta of the transistor does not impact the calculated temperature values. The resultant "diode" model essentially predicts a quasi linear relationship between the base/emitter voltage differential of the PNP transistor and the applied temperature (one of the proportionality constants in this relationship is processor specific, and is known as the diode ideality factor). Realization of this relationship is accomplished with the SMBus thermal sensor that is connected to the transistor.

The processor, however, is built on Intel's advanced 45-nm processor technology. Due to this new processor technology, it is no longer possible to model the substrate transistor as a simple diode. To accurately calculate silicon temperature use a full bi-polar junction transistor-type model. In this model, the voltage/current and temperature characteristics include an additional process dependant parameter which is known as the transistor "beta". System designers should be aware that the current thermal sensors may not be configured to account for "beta" and should work with their SMB thermal sensor vendors to ensure they have a part capable of reading the thermal diode in BJT model.

Offset between the thermal diode-based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor's Automatic mode activation of the thermal control circuit. This temperature offset must be considered when using the processor thermal diode to implement power management events. This offset is different than the diode Toffset value programmed into the processor Model-Specific Register (MSR).

Table 27 and Table 28 provide the diode interface and transistor model specifications.

Table 27. Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THERMDA	A24	Thermal diode anode
THERMDC	A25	Thermal diode cathode

Table 28. Thermal Diode Parameters Using Transistor Model

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5	—	200	μA	1
I_E	Emitter Current	5	—	200	μA	1
n_Q	Transistor Ideality	0.997	1.001	1.008		2, 3, 4
Beta		0.1	0.4	0.5		2, 3
R_T	Series Resistance	3.0	4.5	7.0	Ω	2

NOTES:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized across a temperature range of 50-105°C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, nQ, represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current:

$$I_C = I_S * (e^{qV_{BE}/n_Q kT} - 1)$$

where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the transistor base emitter junction (same nodes as VD), k = Boltzmann Constant, and T = absolute temperature (Kelvin).

5.1.2 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, the TCC would only be activated for very short periods of time when running the most power-intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks or by initiating an Enhanced Intel SpeedStep Technology transition when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

There are two automatic modes called Intel Thermal Monitor 1 (TM1) and Intel Thermal Monitor 2 (TM2). These modes are selected by writing values to the MSRs of the processor. After automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

When TM1 is enabled and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed-dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

When TM2 is enabled and a high temperature situation exists, the processor will perform an Enhanced Intel SpeedStep Technology transition to the LFM. When the processor temperature drops below the critical level, the processor will make an Enhanced Intel SpeedStep Technology transition to the last requested operating point. The processor also supports Enhanced Multi-Threaded Thermal Monitoring (EMTTM). EMTTM is a processor feature that enhances TM2 with a processor throttling algorithm known as Adaptive TM2. Adaptive TM2 transitions to intermediate operating points, rather than directly to the LFM, once the processor has reached its thermal limit and subsequently searches for the highest possible operating point. Please ensure this feature is enabled and supported in the BIOS. Also with EMTTM enabled, the operating system can request the processor to **throttling to any point between Intel Dynamic Acceleration Technology frequency and SuperLFM frequency as long as these features are enabled in the BIOS and supported by the processor.**

The Intel Thermal Monitor automatic mode and Enhanced Multi-Threaded Thermal Monitoring must be enabled through BIOS for the processor to be operating within specifications. Intel recommends TM1 and TM2 be enabled on the processors.

TM1, TM2 and EMTTM features are collectively referred to as Adaptive Thermal Monitoring features.

TM1 and TM2 can co-exist within the processor. If both TM1 and TM2 bits are enabled in the auto-throttle MSR, TM2 takes precedence over TM1. However, if Force TM1 over TM2 is enabled in MSRs via BIOS and TM2 is not sufficient to cool the processor below the maximum operating temperature, then TM1 will also activate to help cool down the processor.

If a processor load-based Enhanced Intel SpeedStep Technology transition (through MSR write) is initiated when a TM2 period is active, there are two possible results:

1. If the processor load-based Enhanced Intel SpeedStep Technology transition target frequency is **higher** than the TM2 transition-based target frequency, the processor load-based transition will be deferred until the TM2 event has been completed.
2. If the processor load-based Enhanced Intel SpeedStep Technology transition target frequency is **lower** than the TM2 transition-based target frequency, the processor will transition to the processor load-based Enhanced Intel SpeedStep Technology target frequency point.

The TCC may also be activated via on-demand mode. If bit 4 of the ACPI Intel Thermal Monitor control register is written to a 1, the TCC will be activated immediately independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled, however, if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three MSR, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

PROCHOT# will not be asserted when the processor is in the Stop Grant, Sleep, Deep Sleep, and Deeper Sleep low-power states, hence the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within maximum specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above low-power states with PROCHOT# already asserted, PROCHOT# will remain asserted until the processor exits the low-power state and the processor junction temperature drops below the thermal trip point. However, PROCHOT# will de-assert for the duration of Deep Power Down Technology state (C6) residency.

If Thermal Monitor automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125 °C. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in Chapter 3.

In all cases the Intel Thermal Monitor feature must be enabled for the processor to remain within specification.

5.1.3 Digital Thermal Sensor

The processor also contains an on-die Digital Thermal Sensor (DTS) that can be read via an MSR (no I/O interface). Each core of the processor will have a unique digital thermal sensor whose temperature is accessible via the processor MSRs. The DTS is the preferred method of reading the processor die temperature since it can be located much closer to the hottest portions of the die and can thus more accurately track the die temperature and potential activation of processor core clock modulation via the Thermal Monitor. The DTS is only valid while the processor is in the normal operating state (the Normal package level low-power state).

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor ($T_{J,max}$). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the DTS will always be at or below $T_{J,max}$. Catastrophic temperature conditions are detectable via an Out Of Specification status bit. This bit is also part of the DTS MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not ensured once the activation of the Out of Specification status bit is set.

The DTS-relative temperature readout corresponds to the Thermal Monitor (TM1/TM2) trigger point. When the DTS indicates maximum processor core temperature has been reached, the TM1 or TM2 hardware thermal control mechanism will activate. The DTS and TM1/TM2 temperature may not correspond to the thermal diode reading since the thermal diode is located in a separate portion of the die and thermal gradient between the individual core DTS. Additionally, the thermal gradient from DTS to thermal diode can vary substantially due to changes in processor power, mechanical and thermal attach, and software application. The system designer is required to use the DTS to ensure proper operation of the processor within its temperature operating specifications.

Changes to the temperature can be detected via two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts via the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

5.2 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shutdown before the THERMTRIP# is activated. If the processor's TM1 or TM2 are triggered and the temperature remains high, an Out Of Spec status and sticky bit are latched in the status MSR register and generates a thermal interrupt.

5.3 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If TM1 or TM2 is enabled, then the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#. Refer to the an interrupt upon the assertion or deassertion of PROCHOT#. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

The processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from overheating situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

Only a single PROCHOT# pin exists at a package level of the processor. When either core's thermal sensor trips, PROCHOT# signal will be driven by the processor package. If only TM1 is enabled, PROCHOT# will be asserted regardless of which core is above its TCC temperature trip point, and both cores will have their core clocks modulated. If TM2 is enabled then, regardless of which core(s) are above the TCC temperature trip point, both cores will enter the lowest programmed TM2 performance state. It is important to note that Intel recommends both TM1 and TM2 to be enabled.

When PROCHOT# is driven by an external agent, if only TM1 is enabled on both cores, then both processor cores will have their core clocks modulated. If TM2 is enabled on both cores, then both processor cores will enter the lowest programmed TM2 performance state. It should be noted that Force TM1 on TM2, enabled via BIOS, does not have any effect on external PROCHOT#. If PROCHOT# is driven by an external agent when TM1, TM2, and Force TM1 on TM2 are all enabled, then the processor will still apply only TM2.

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power-intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss.

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