60V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ Max	I_D T_A = +25°C
60V	44mΩ @ V_{GS} = 10V	5.0A
	60mΩ @ V_{GS} = 4.5V	4.3A

Features and Benefits

- 100% Unclamped Inductive Switch (UIS) Test in Production
- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 standards for High Reliability**
- **PPAP Capable (Note 4)**

Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

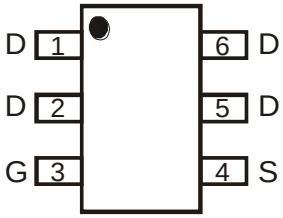
- DC-DC Converters
- Power Management Functions
- Backlighting

Mechanical Data

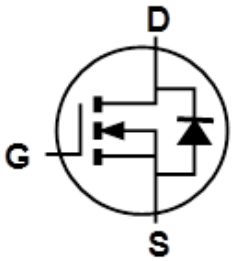
- Case: TSOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Tin Finish Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 ⓔ3
- Weight: 0.013 grams (Approximate)

TSOT26

Top View



Top View
Pin Configuration



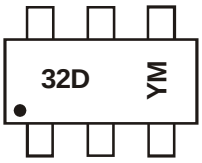
Equivalent Circuit

Ordering Information (Note 5)

Part Number	Case	Packaging
DMN6040SVTQ-7	TSOT26	3,000/Tape & Reel
DMN6040SVTQ-13	TSOT26	10,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Automotive products are AEC-Q101 qualified and are PPAP capable. Please refer to http://www.diodes.com/quality/product_compliance_definitions/.
5. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



32D = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: X = 2010)
M = Month (ex: 9 = September)

Date Code Key

Year	2010	…	2017	2018	2019	2020	2021	2022	2023	2024	2025
Code	X	…	E	F	G	H	I	J	K	L	M

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	60	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 7) V_{GS} = 10V	Steady State	T_A = +25°C T_A = +70°C	I_D	5.0 4.0	A
	t<10s	T_A = +25°C T_A = +70°C	I_D	6.3 5.0	A
Continuous Drain Current (Note 7) V_{GS} = 5V	Steady State	T_A = +25°C T_A = +70°C	I_D	4.3 3.4	A
	t<10s	T_A = +25°C T_A = +70°C	I_D	5.4 4.3	A
Maximum Body Diode Forward Current (Note 7)			I_S	2.1	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	30	A
Avalanche Current (Note 8) L = 0.1mH			I_{AR}	14.2	A
Avalanche Energy (Note 8) L = 0.1mH			E_{AR}	10	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	1.2	W
	T_A = +70°C		0.75	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	106	°C/W
	t<10s		69	°C/W
Total Power Dissipation (Note 7)	T_A = +25°C	P_D	1.8	W
	T_A = +70°C		1.1	
Thermal Resistance, Junction to Ambient (Note 7)	Steady State	$R_{\theta JA}$	68	°C/W
	t<10s		44	°C/W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	20	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 6. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
7. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
8. I_{AR} and E_{AR} rating are based on low frequency and duty cycles to keep T_J = +25°C.

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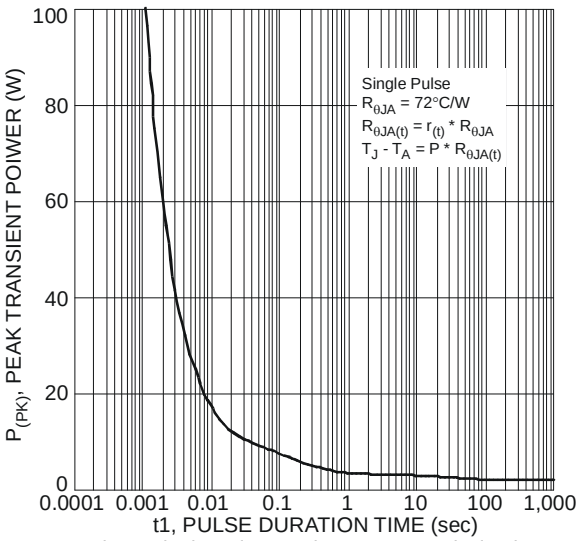

Fig. 1 Single Pulse Maximum Power Dissipation

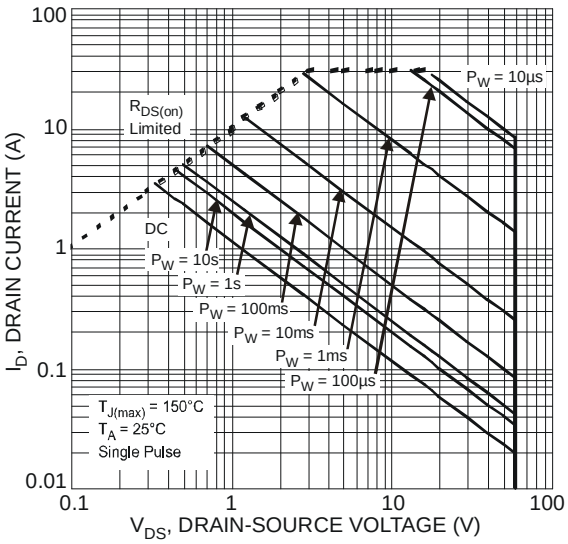

Fig. 2 SOA, Safe Operation Area

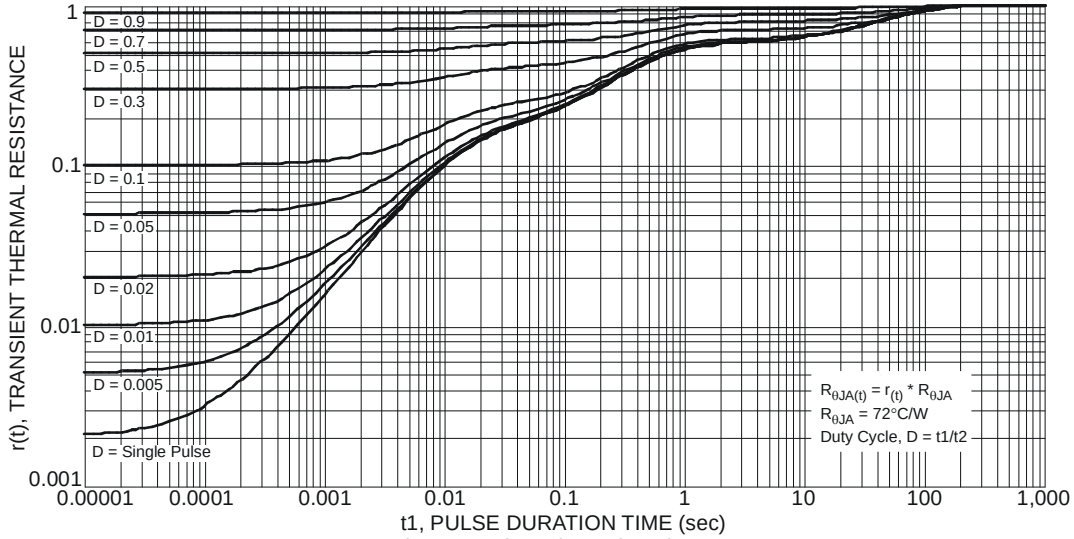

Fig. 3 Transient Thermal Resistance

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Electrical Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	100	nA	V_{DS} = 60V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	1	—	3	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	30	44	mΩ	V_{GS} = 10V, I_D = 4.3A
		—	35	60		V_{GS} = 4.5V, I_D = 4A
Forward Transfer Admittance	$\|Y_{FS}\|$	—	4.5	—	S	V_{DS} = 10V, I_D = 4.3A
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{ISS}	—	1,287	—	pF	V_{DS} = 25V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{OSS}	—	57	—		
Reverse Transfer Capacitance	C_{RSS}	—	44	—		
Gate Resistance	R_G	—	1.2	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = 10V)	Q_G	—	22.4	—	nC	V_{DS} = 30V, I_D = 4.3A
Total Gate Charge (V_{GS} = 4.5V)	Q_G	—	10.4	—		
Gate-Source Charge	Q_{GS}	—	4.9	—		
Gate-Drain Charge	Q_{GD}	—	3.0	—		
Turn-On Delay Time	$t_{D(ON)}$	—	6.6	—	ns	V_{GS} = 10V, V_{DD} = 30V, R_G = 6Ω, I_D = 4.3A
Turn-On Rise Time	t_R	—	8.1	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	20.1	—		
Turn-Off Fall Time	t_F	—	4.0	—		
Body Diode Reverse Recovery Time	t_{RR}	—	18	—	ns	I_S = 4.3A, dI/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q_{RR}	—	11.9	—	nC	I_S = 4.3A, dI/dt = 100A/μs

Notes: 9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

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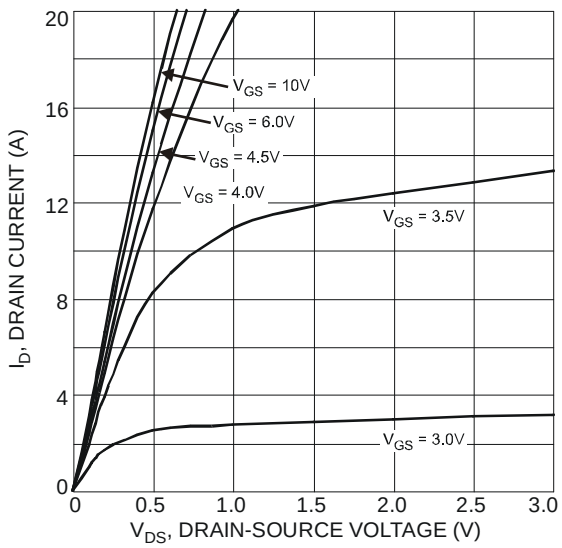

Fig. 4 Typical Output Characteristic

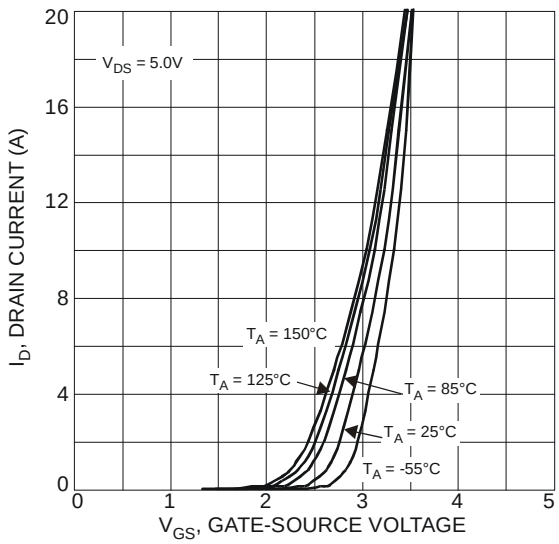

Fig. 5 Typical Transfer Characteristics

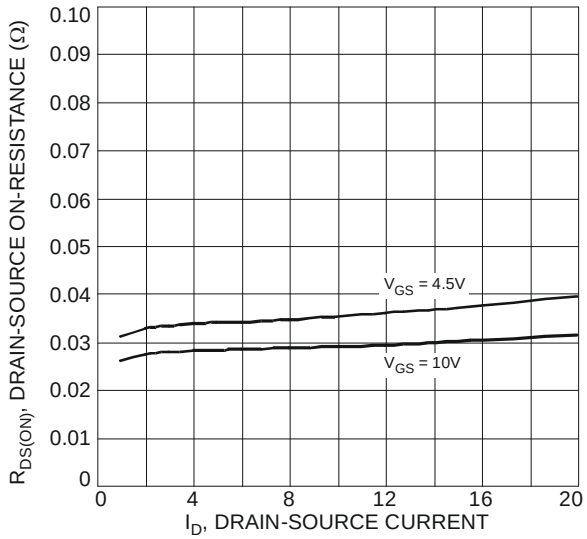

Fig. 6 Typical On-Resistance vs. Drain Current and Gate Voltage

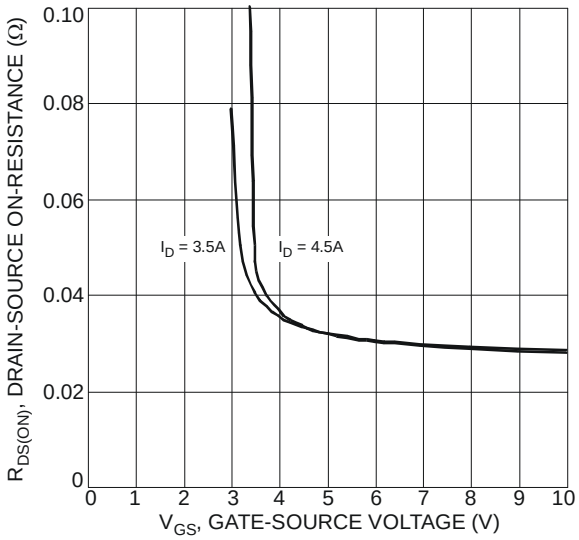

Fig. 7 Typical On-Resistance vs. Drain Current and Gate Voltage

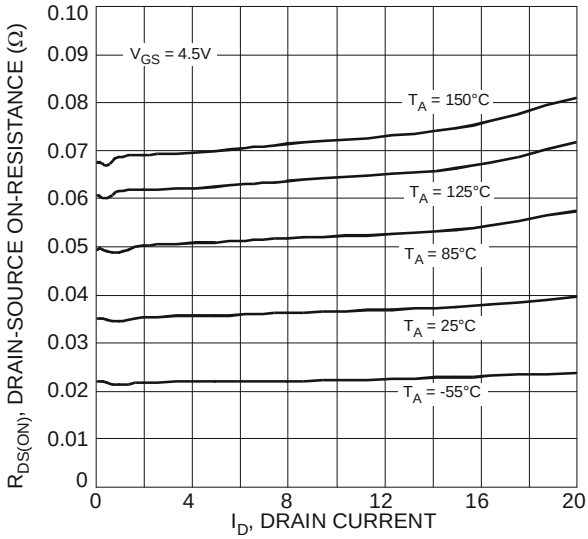

Fig. 8 Typical On-Resistance vs. Drain Current and Temperature

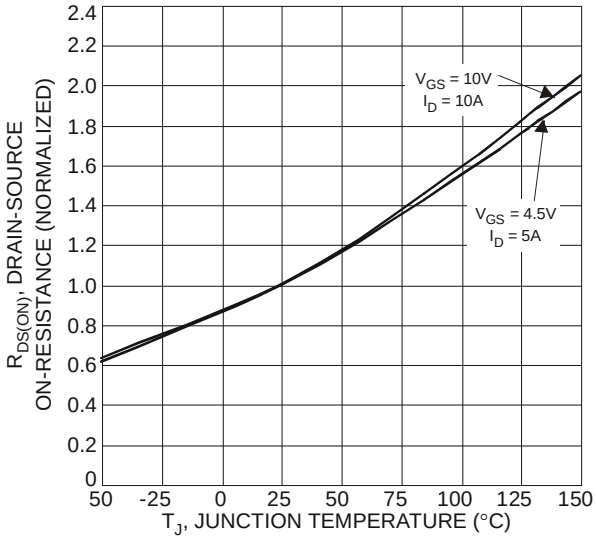

Fig. 9 On-Resistance Variation with Temperature

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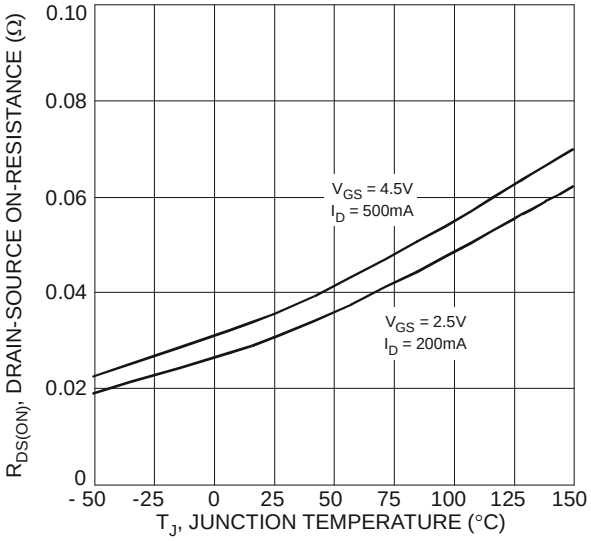

Fig. 10 On-Resistance Variation with Temperature

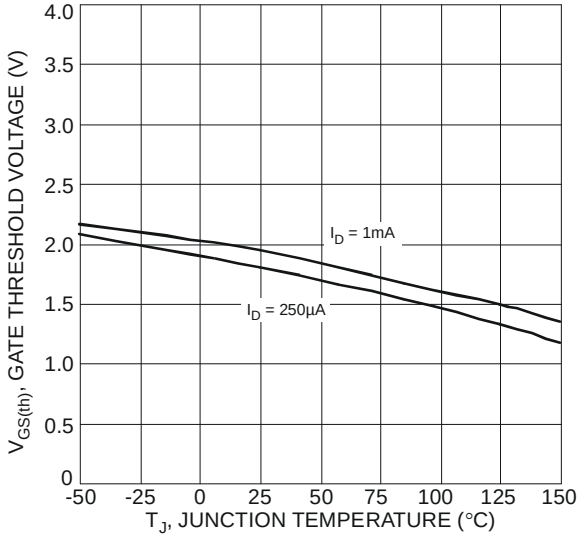

Fig. 11 Gate Threshold Variation vs. Ambient Temperature

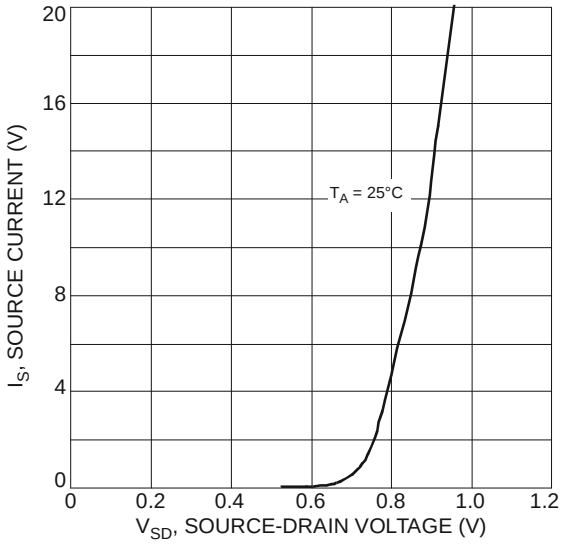

Fig. 12 Diode Forward Voltage vs. Current

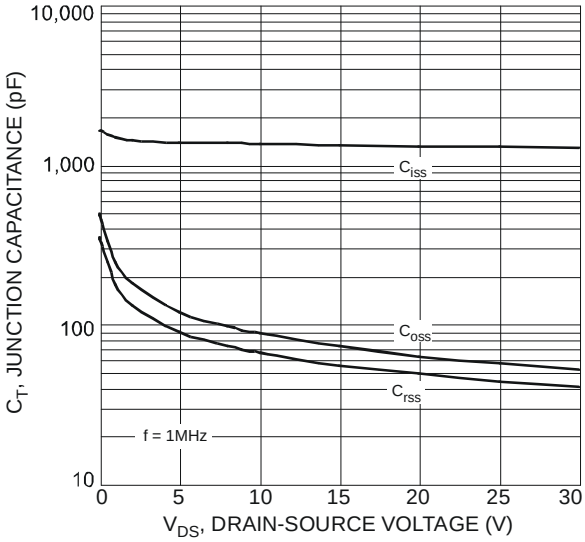

Fig. 13 Typical Junction Capacitance

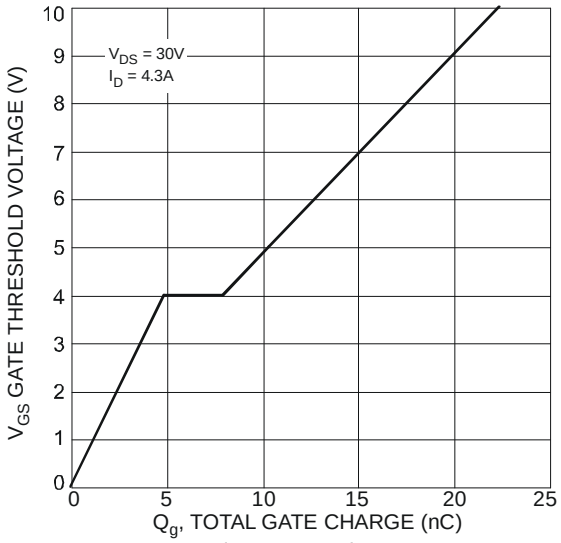

Fig. 14 Gate Charge

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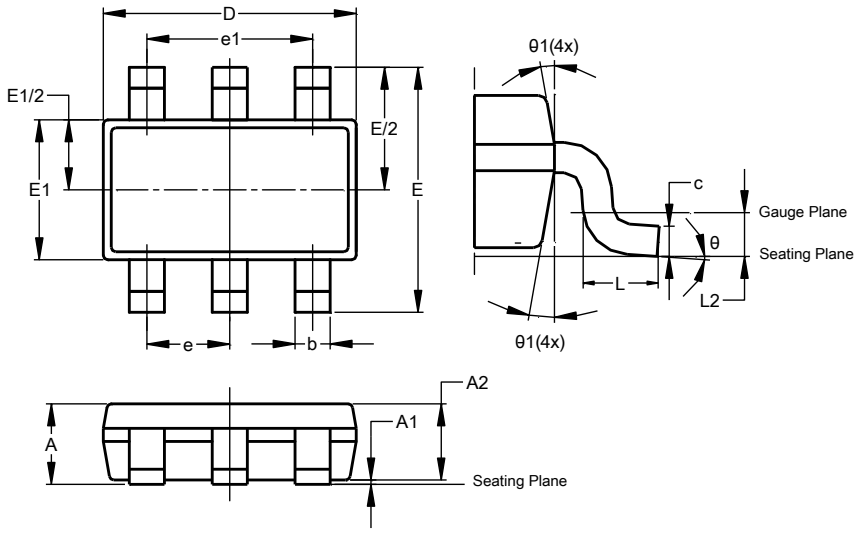
Package Outline Dimensions

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

TSOT26

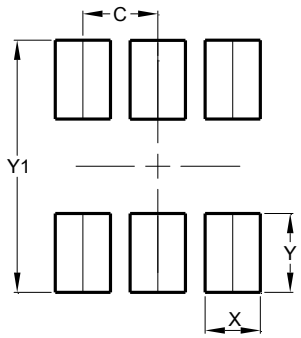


TSOT26			
Dim	**Min**	**Max**	**Typ**
A	–	1.00	–
A1	0.010	0.100	–
A2	0.840	0.900	–
D	2.800	3.000	2.900
E	2.800 BSC		
E1	1.500	1.700	1.600
b	0.300	0.450	–
c	0.120	0.200	–
e	0.950 BSC		
e1	1.900 BSC		
L	0.30	0.50	
L2	0.250 BSC		
θ	0°	8°	4°
θ1	4°	12°	–
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

TSOT26



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199

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