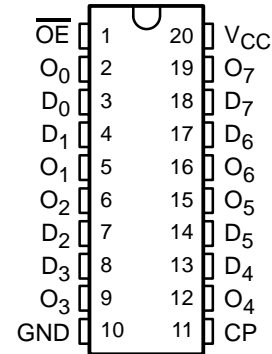


# CY74FCT2374T 8-BIT REGISTER WITH 3-STATE OUTPUTS

SCCS040A – SEPTEMBER 1994 – REVISED OCTOBER 2001

- Function and Pinout Compatible With FCT and F Logic
- 25- $\Omega$  Output Series Resistors to Reduce Transmission-Line Reflection Noise
- Reduced  $V_{OH}$  (Typically = 3.3 V) Version of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- 3-State Outputs
- 12-mA Output Sink Current  
15-mA Output Source Current
- Edge-Triggered D-Type Inputs
- 250-MHz Typical Switching Rate

SN74FCT2374T . . . Q OR SO PACKAGE  
(TOP VIEW)



## description

The CY74FCT2374T is a high-speed, low-power, octal D-type flip-flop featuring separate D-type inputs for each flip-flop. On-chip termination resistors at the outputs reduce system noise caused by reflections. The CY74FCT2374T can replace the CY74FCT374T to reduce noise in an existing design. The device has 3-state outputs for bus-oriented applications. A buffered clock (CP) and output-enable ( $\overline{OE}$ ) inputs are common to all flip-flops. The flip-flops in the CY74FCT2374T store the state of their individual data (D) inputs that meet the setup-time and hold-time requirements on the low-to-high CP transition. When  $\overline{OE}$  is low, the contents of the flip-flops are available at the outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state. The state of  $\overline{OE}$  does not affect the state of the flip-flops.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# CY74FCT2374T

## 8-BIT REGISTER WITH 3-STATE OUTPUTS

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## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	5.2	CY74FCT2374CTQCT	FCT2374C
	SOIC – SO	Tube	5.2	CY74FCT2374CTSOC	FCT2374C
		Tape and reel	5.2	CY74FCT2374CTSOCT	
	QSOP – Q	Tape and reel	6.5	CY74FCT2374ATQCT	FCT2374A
	SOIC – SO	Tube	6.5	CY74FCT2374ATSOC	FCT2374A
		Tape and reel	6.5	CY74FCT2374ATSOCT	
	SOIC – SO	Tube	10	CY74FCT2374TSOC	FCT2374
		Tape and reel	10	CY74FCT2374TSOCT	

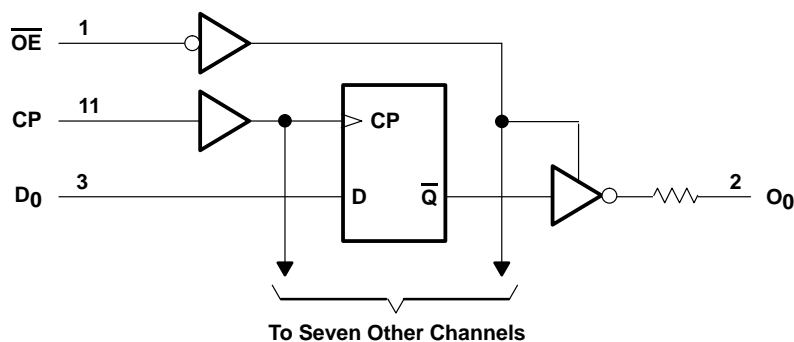
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

INPUTS			OUTPUT O
D	CP	$\overline{OE}$	
H	$\uparrow$	L	H
L	$\uparrow$	L	L
X	X	H	Z

H = High logic level, L = Low logic level,  
X = Don't care, Z = High-impedance  
state,  $\uparrow$  = Low-to-high clock transition

**logic diagram (positive logic)**



**absolute maximum rating over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range to ground potential .....	–0.5 V to 7 V
DC input voltage range .....	–0.5 V to 7 V
DC output voltage range .....	–0.5 V to 7 V
DC output current (maximum sink current/pin) .....	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package .....	68°C/W
SO package .....	58°C/W
Ambient temperature range with power applied, $T_A$ .....	–65°C to 135°C
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 2)**

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$I_{OH}$ High-level output current			–15	mA
$I_{OL}$ Low-level output current			12	mA
$T_A$ Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

# CY74FCT2374T

## 8-BIT REGISTER

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.75 V,	I <sub>IN</sub> = −18 mA		−0.7	−1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.75 V,	I <sub>OH</sub> = −15 mA	2.4	3.3		V
V <sub>OL</sub>	V <sub>CC</sub> = 4.75 V,	I <sub>OL</sub> = 12 mA		0.3	0.55	V
R <sub>OUT</sub>	V <sub>CC</sub> = 4.75 V,	I <sub>OL</sub> = 12 mA	20	25	40	Ω
V <sub>hys</sub>	All inputs			0.2		V
I <sub>I</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = V <sub>CC</sub>			5	μA
I <sub>IH</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = 2.7 V			±1	μA
I <sub>IL</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = 0.5 V			±1	μA
I <sub>OZH</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>OUT</sub> = 2.7 V			10	μA
I <sub>OZL</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>OUT</sub> = 0.5 V			−10	μA
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.25 V,	V <sub>OUT</sub> = 0 V	−60	−120	−225	mA
I <sub>off</sub>	V <sub>CC</sub> = 0 V,	V <sub>OUT</sub> = 4.5 V			±1	μA
I <sub>CC</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.2 V		0.1	0.2	mA
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open			0.5	2	mA
I <sub>CCD</sub> ¶	V <sub>CC</sub> = 5.25 V, Outputs open, One input switching at 50% duty cycle, OE = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.2 V			0.06	0.12	mA/MHz
I <sub>C</sub> <sup>#</sup>	V <sub>CC</sub> = 5.25 V, Outputs open, f <sub>0</sub> = 10 MHz, OE = GND	One bit switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.2V	0.7	1.4	mA
			V <sub>IN</sub> = 3.4 V or GND	1.2	3.4	
		Eight bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.2 V	1.6	3.2	
			V <sub>IN</sub> = 3.4 V or GND	3.9	12.2	
C <sub>i</sub>				5	10	pF
C <sub>o</sub>				9	12	pF

† Typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

§ Per TTL-driven input ( $V_{IN} = 3.4\text{ V}$ ); all other inputs at  $V_{CC}$  or GND

¶ This parameter is derived for use in total power-supply calculations.

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4\text{ V}$ )

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the  $I_{CC}$  formula.



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**8-BIT REGISTER**  
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**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		CY74FCT2374T		CY74FCT2374AT		CY74FCT2374CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, CP	7		5		4		ns
$t_{su}$	Setup time, data before CP $\uparrow$	2		2		1.5		ns
$t_h$	Hold time, data after CP $\uparrow$	1.5		1.5		1		ns

**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT2374T		CY74FCT2374AT		CY74FCT2374CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	CP	O	2	10	2	6.5	2	5.2	ns
$t_{PHL}$			2	10	2	6.5	2	5.2	
$t_{PZH}$	$\overline{OE}$	O	1.5	12.5	1.5	6.5	1.5	6.2	ns
$t_{PZL}$			1.5	12.5	1.5	6.5	1.5	6.2	
$t_{PHZ}$	$\overline{OE}$	O	1.5	8	1.5	5.5	1.5	5	ns
$t_{PLZ}$			1.5	8	1.5	5.5	1.5	5	

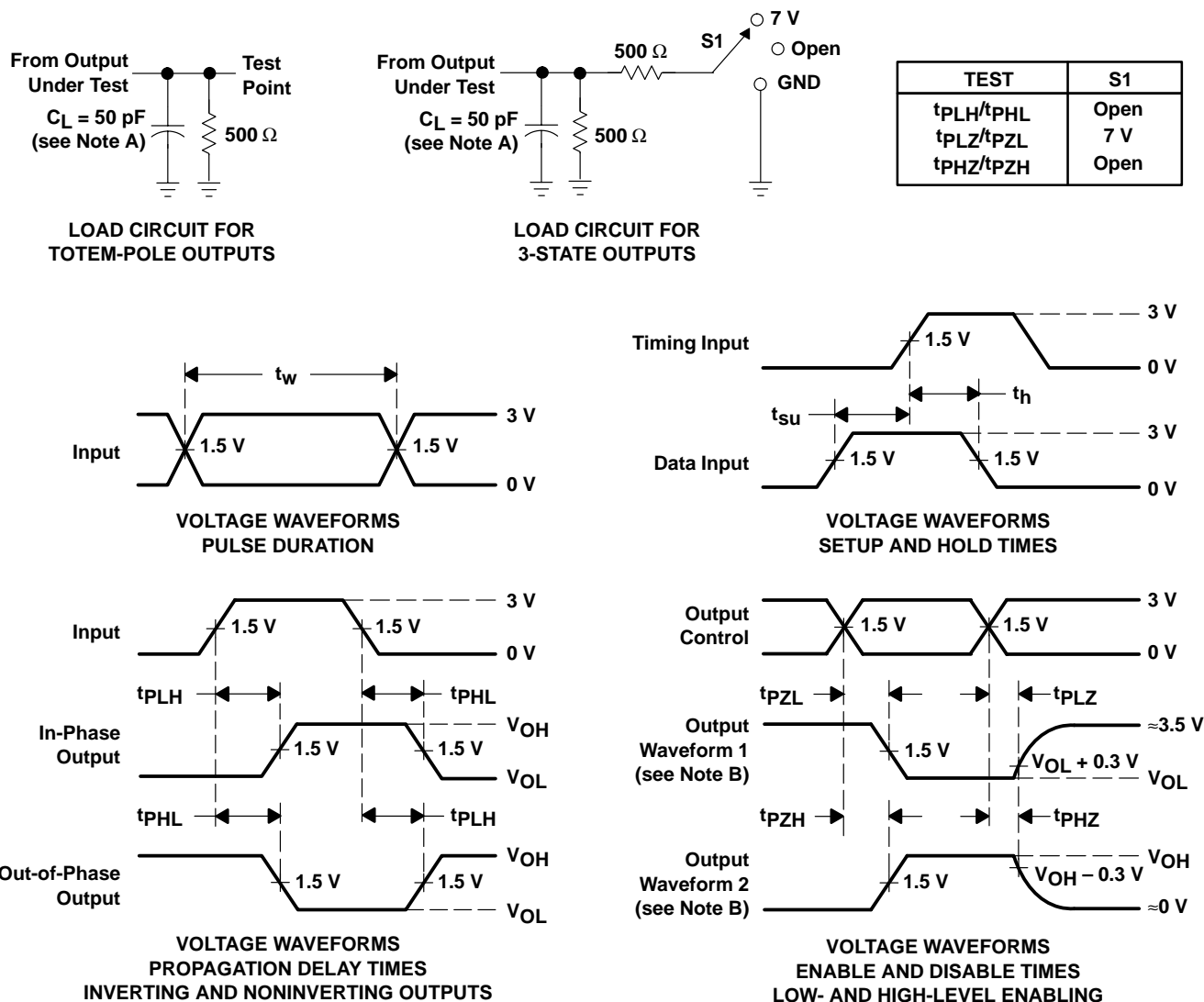
# CY74FCT2374T

## 8-BIT REGISTER

### WITH 3-STATE OUTPUTS

SCCS040A – SEPTEMBER 1994 – REVISED OCTOBER 2001

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74FCT2374ATSOCTE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
74FCT2374ATSOCTG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
74FCT2374CTSOCTE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
74FCT2374CTSOCTG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
74FCT2574ATQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
74FCT2574ATSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT2574ATSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT2574CTSOCTE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
74FCT2574CTSOCTG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2374ATQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2374ATQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2374ATQCTG4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2374ATSOCE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2374ATSOCG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2374CTQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20		TBD	Call TI	Call TI
CY74FCT2374CTQCTG4	ACTIVE	SSOP/ QSOP	DBQ	20		TBD	Call TI	Call TI
CY74FCT2374CTSOCE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2374CTSOCG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2374TSOCE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2374TSOCG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2374TSOCTE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2374TSOCTG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2574ATQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2574ATQCTG4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2574ATSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2574ATSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2574ATSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2574ATSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2574CTQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2574CTQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2574CTQCTG4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
QSOP						no Sb/Br)		
CY74FCT2574CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2574CTSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2574CTSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2574TSOCE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2574TSOCG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2574TSOCTE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2574TSOCTG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT2374ATQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT2574ATQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT2574ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT2574CTQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS

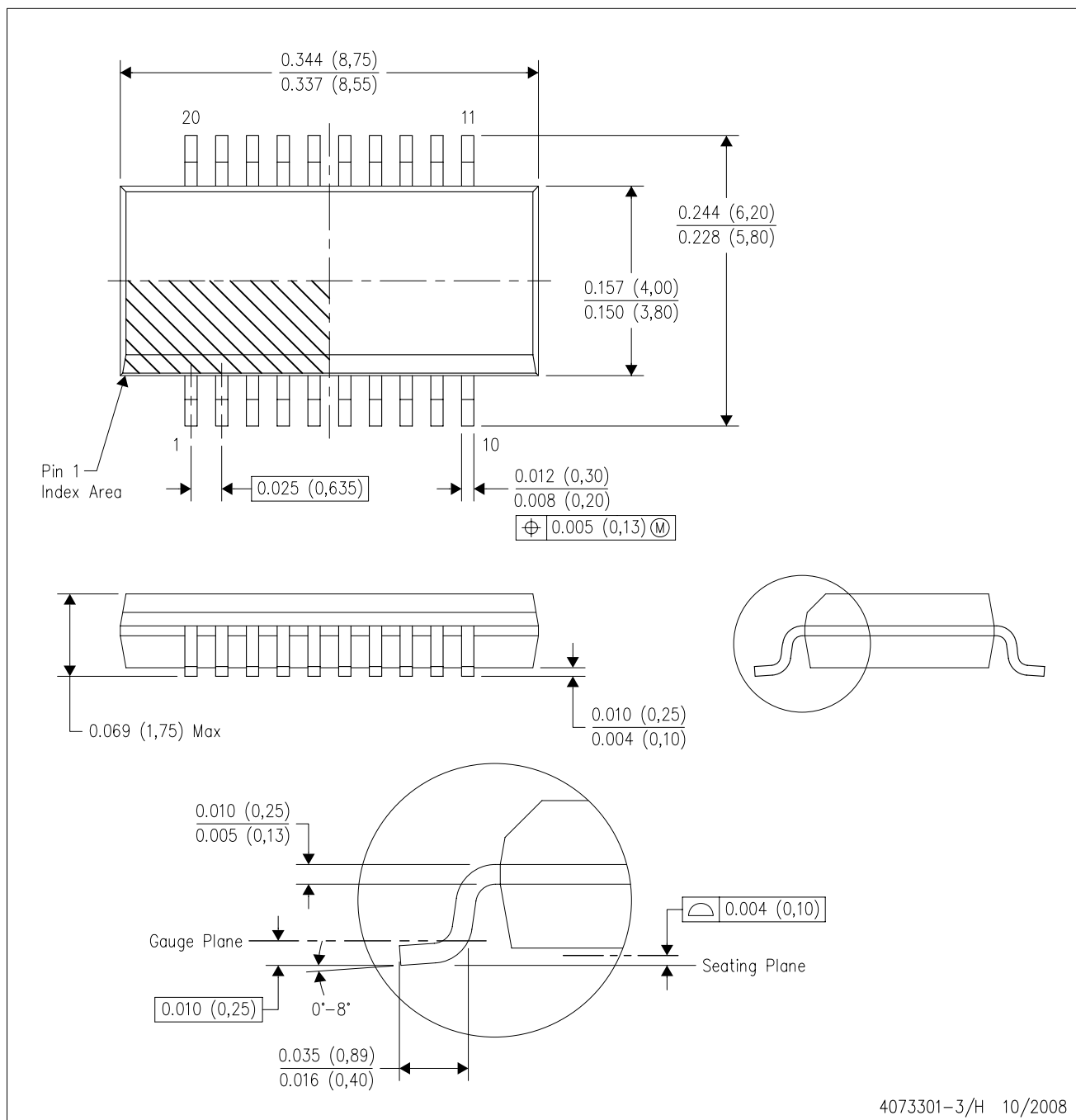


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT2374ATQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT2574ATQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT2574ATSOCT	SOIC	DW	20	2000	346.0	346.0	41.0
CY74FCT2574CTQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0

DBQ (R-PDSO-G20)

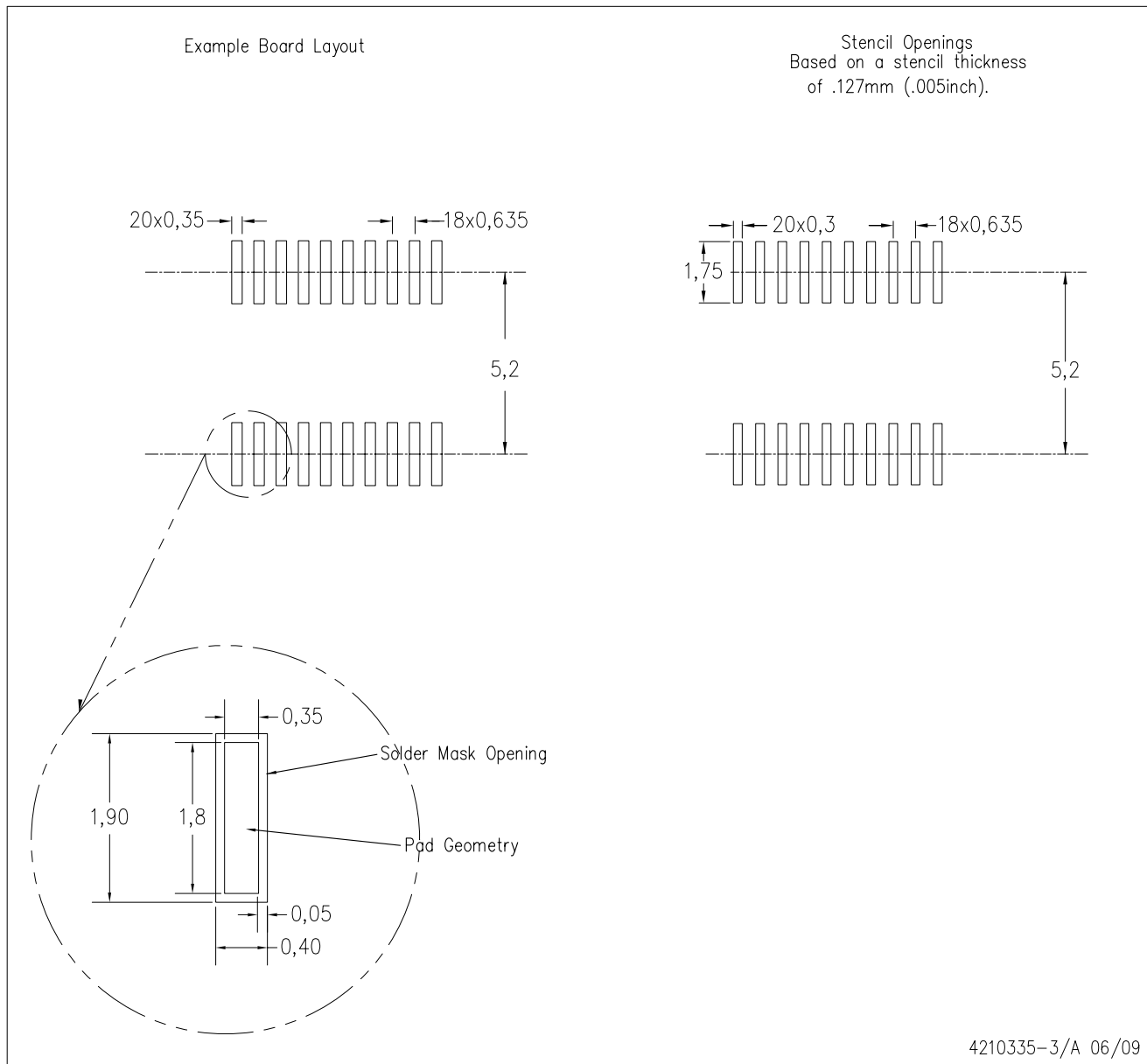
PLASTIC SMALL-OUTLINE PACKAGE



4073301-3/H 10/2008

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - Falls within JEDEC MO-137 variation AD.

## DBQ (R-PDSO-G20)



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## DW (R-PDSO-G20)

## PLASTIC SMALL-OUTLINE PACKAGE



4040000-4/F 06/2004

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.

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