HD74AC283/HD74ACT283

4-bit Binary Full Adder with Fast Carry

REJ03D0267–0200Z
(Previous ADE-205-388 (Z))
Rev.2.00
Jul.16.2004

Description

The HD74AC283/HD74ACT283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary works ($A_0 – A_3$, $B_0 – B_3$) and a Carry input (C_0). It generates the binary Sum outputs ($S_0 – S_3$) and the Carry output (C_4) from the most significant bit. The HD74AC283/HD74ACT283 will operate with either active High or active Low operands (positive or negative logic).

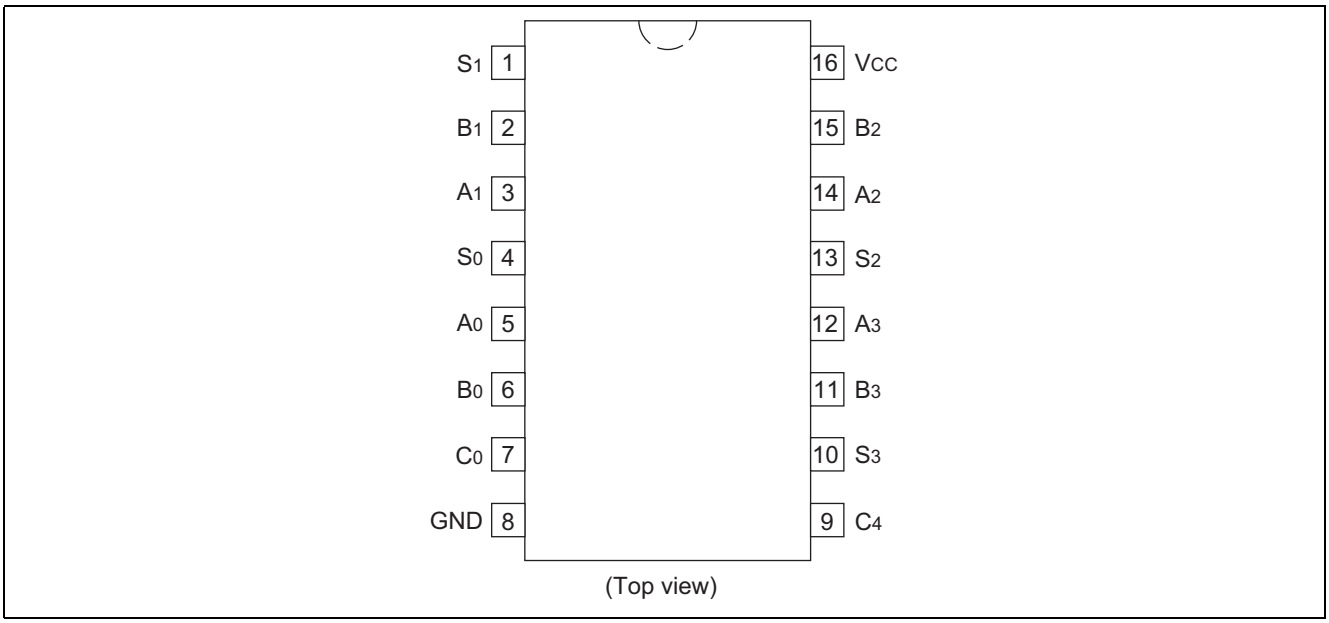
Features

- Outputs Source/Sink 24 mA
- HD74ACT283 has TTL-Cmpatible Inputs
- Ordering Information: Ex. HD74AC283

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC283AP	DIP-16 pin	DP-16E, -16FV	P	—
HD74AC283AFPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74AC283ARPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)
HD74AC283TELL	TSSOP-16 pin	TTP-16DAV	T	ELL(2,000 pcs/reel)

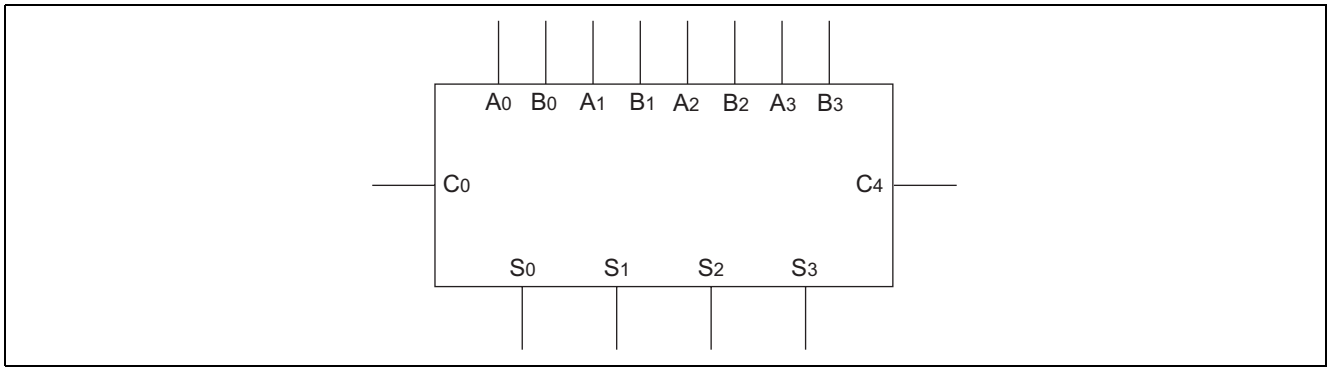
Notes: 1. Please consult the sales office for the above package availability.
2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



(Top view)

Logic Symbol



Pin Names

$A_0 – A_3$	A Operand Inputs
$B_0 – B_3$	B Operand Inputs
C_0	Carry Input
$S_0 – S_3$	Sum Outputs
C_4	Carry Output

Functional Description

The HD74AC283/HD74ACT283 adds two 4-bit binary words (A plus B) plus the incoming Carry (C_0). The binary sum appears on the Sum ($S_0 – S_3$) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C_0, A_0, B_0 can be arbitrarily assigned to pins 5, 6 and 7 for DIPS. Due to the symmetry of the binary add function, the HD74AC283/HD74ACT283 can be used either with all inputs and outputs active High (positive logic) or with all inputs and outputs active Low (negative logic). See Figure a. Note that if C_0 is not used it must be tied Low for active High logic or tied High for active Low logic.

Due to pin limitations, the intermediate carries of the HD74AC283/HD74ACT283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure b shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) Low makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle Figure c shows a way of dividing the HD74AC283/HD74ACT283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2. Note that as long as A_2 and B_2 are the same, whether High or Low, they do not influence S_2. Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third stage. Figure d shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0, S_1 and S_2 present a binary number equal to the number of inputs $I_1 – I_5$ that are true. Figure e shows one method of implementing a 5-input majority gate. When three or more of the inputs $I_1 – I_5$ are true, the output M_5 is true.

Fig. a Active HIGH varsus Active LOW Interpretation

	C_0	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	S_0	S_1	S_2	S_3	C_4
Logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16

Active LOW: 1 + 5 + 6 = 12 + 0

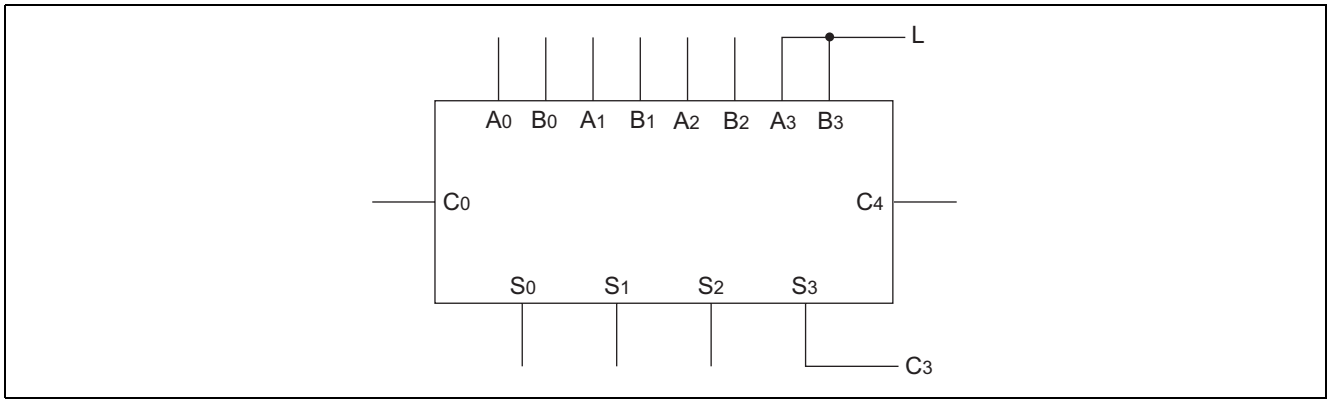


Fig. b 3-bit Adder

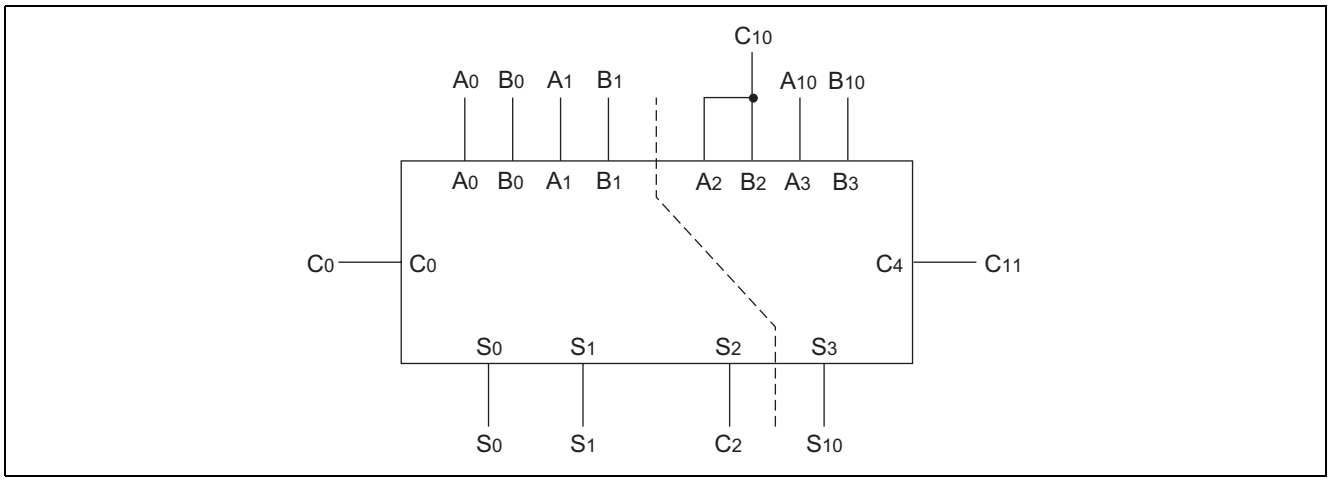


Fig. c 2-bit and 1-bit adders

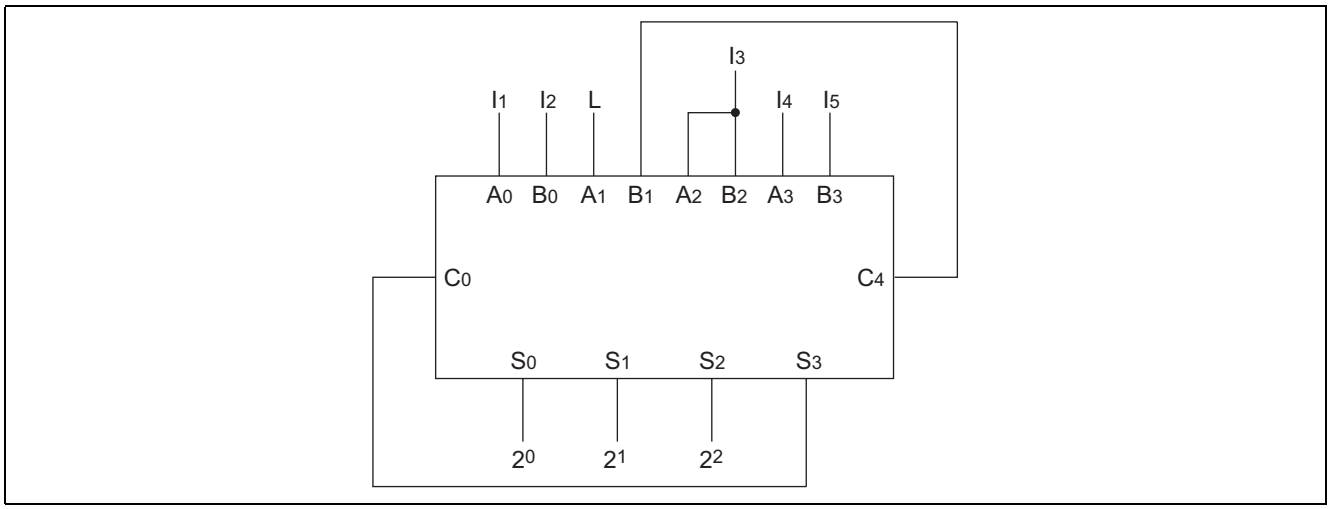


Fig. d 5-Input Encoder

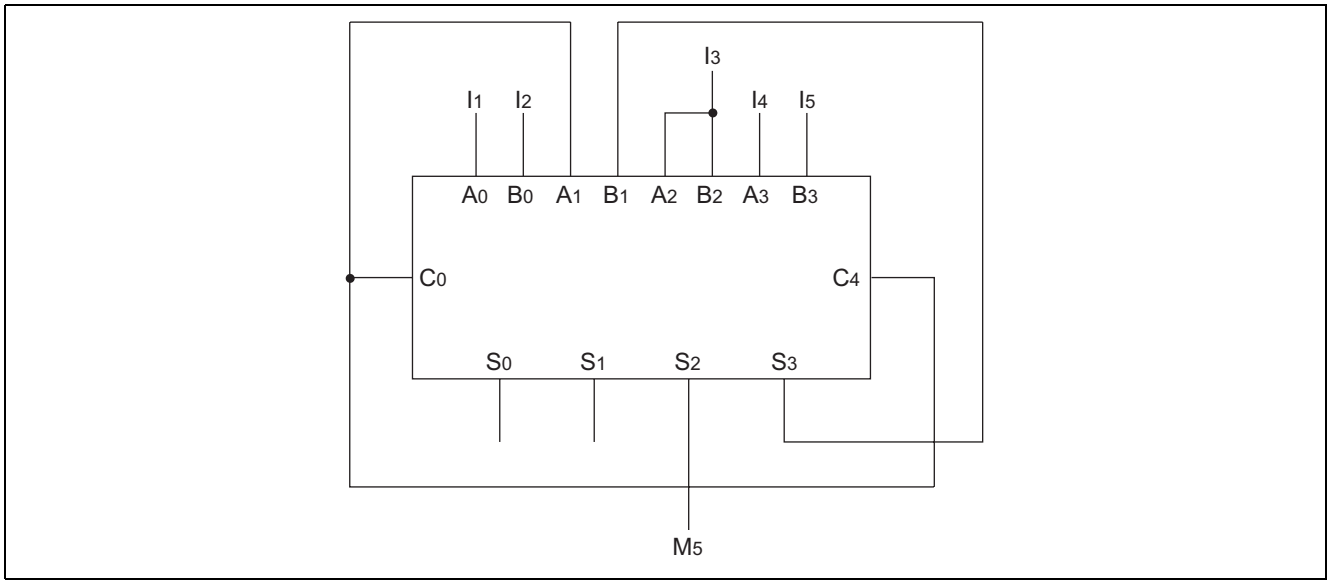
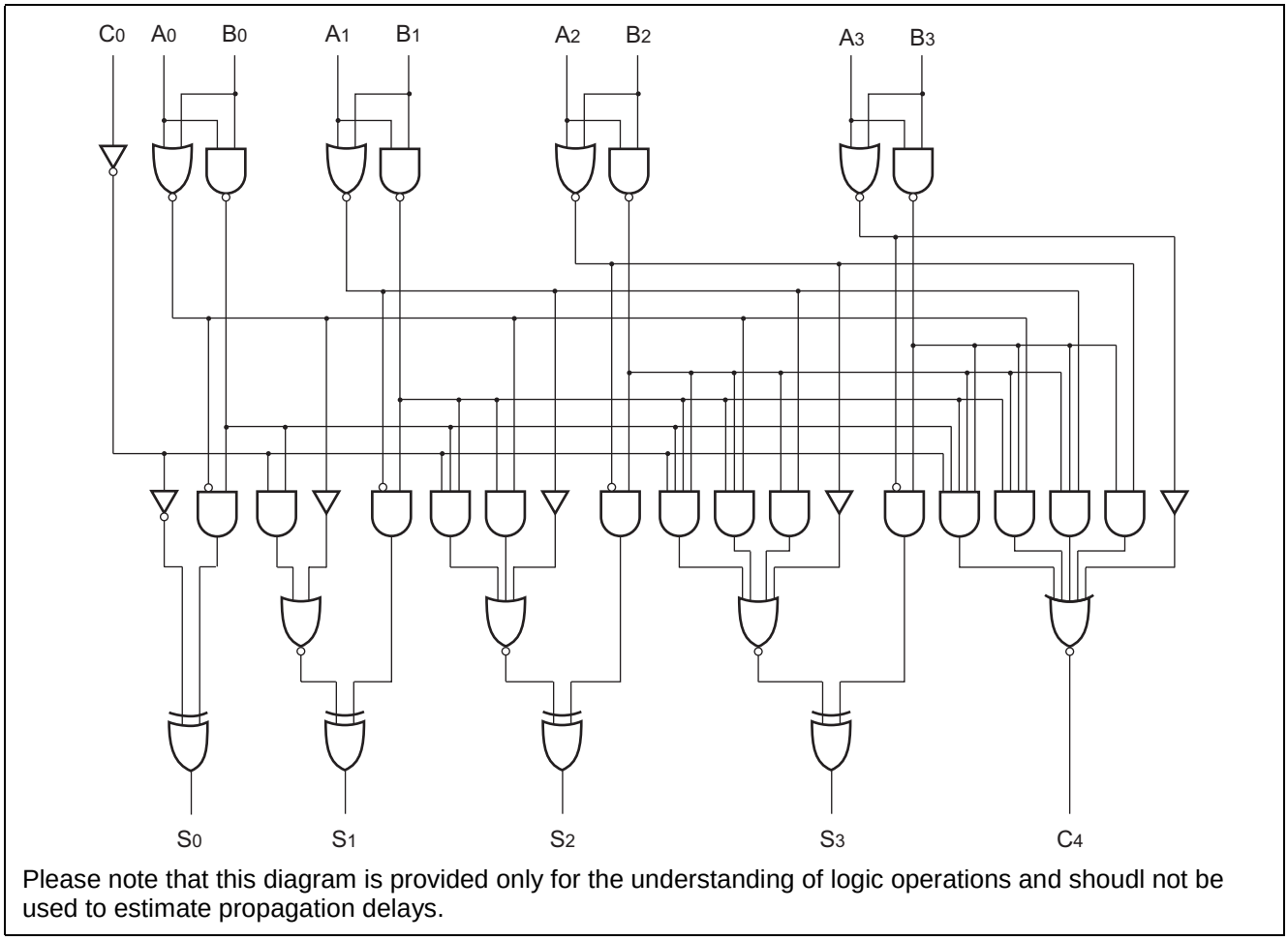


Fig. e 5-Input Majority Gate

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and shoudl not be used to estimate propagation delays.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	–0.5 to 7	V	
DC input diode current	I_{IK}	–20	mA	V_I = –0.5V
		20	mA	V_I = Vcc+0.5V
DC input voltage	V_I	–0.5 to Vcc+0.5	V	
DC output diode current	I_{OK}	–50	mA	V_O = –0.5V
		50	mA	V_O = Vcc+0.5V
DC output voltage	V_O	–0.5 to Vcc+0.5	V	
DC output source or sink current	I_O	±50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	±50	mA	
Storage temperature	Tstg	–65 to +150	°C	

Recommended Operating Conditions: HD74AC283

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	tr, tf	8	ns/V	V_{CC} = 3.0V
				V_{CC} = 4.5 V
				V_{CC} = 5.5 V

DC Characteristics: HD74AC283

Item	Sym-bol	Vcc (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input Voltage	V_{IH}	3.0	2.1	1.5	—	2.1	—	V	V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	3.15	2.25	—	3.15	—			
		5.5	3.85	2.75	—	3.85	—			
	V_{IL}	3.0	—	1.50	0.9	—	0.9		V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	—	2.25	1.35	—	1.35			
		5.5	—	2.75	1.65	—	1.65			
Output voltage	V_{OH}	3.0	2.9	2.99	—	2.9	—	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = –50 µA	
		4.5	4.4	4.49	—	4.4	—			
		5.5	5.4	5.49	—	5.4	—			
		3.0	2.58	—	—	2.48	—		V_{IN} = V_{IL} or V_{IH}	I_{OH} = –12 mA
		4.5	3.94	—	—	3.80	—			I_{OH} = –24 mA
		5.5	4.94	—	—	4.80	—			I_{OH} = –24 mA
	V_{OL}	3.0	—	0.002	0.1	—	0.1		V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 µA	
		4.5	—	0.001	0.1	—	0.1			
		5.5	—	0.001	0.1	—	0.1			
		3.0	—	—	0.32	—	0.37		V_{IN} = V_{IL} or V_{IH}	I_{OL} = 12 mA
		4.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
		5.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
Input leakage current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	V_{OLD} = 1.1 V	
	I_{OHD}	5.5	—	—	—	–75	—	mA	V_{OHD} = 3.85 V	
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	µA	V_{IN} = V_{CC} or ground	

*Maximum test duration 2.0 ms, one output loaded at a time.

Recommended Operating Conditions: HD74ACT283

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 0.8 to 2.0 V	tr, tf	8	ns/V	V_{CC} = 4.5V V_{CC} = 5.5V

DC Characteristics: HD74ACT283

Item	Sym-bol	V_{CC} (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input voltage	V_{IH}	4.5	2.0	1.5	—	2.0	—	V	V_{OUT} = 0.1 V or Vcc–0.1 V	
		5.5	2.0	1.5	—	2.0	—			
	V_{IL}	4.5	—	1.5	0.8	—	0.8		V_{OUT} = 0.1 V or Vcc–0.1 V	
		5.5	—	1.5	0.8	—	0.8			
Output voltage	V_{OH}	4.5	4.4	4.49	—	4.4	—	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = –50 µA	
		5.5	5.4	5.49	—	5.4	—			
		4.5	3.94	—	—	3.80	—		V_{IN} = V_{IL}	I_{OH} = –24 mA
		5.5	4.94	—	—	4.80	—			I_{OH} = –24 mA
	V_{OL}	4.5	—	0.001	0.1	—	0.1		V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 µA	
		5.5	—	0.001	0.1	—	0.1			
		4.5	—	—	0.32	—	0.37		V_{IN} = V_{IL}	I_{OL} = 24 mA
		5.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
Input current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
I_{CC}/input current	I_{CCT}	5.5	—	0.6	—	—	1.5	mA	V_{IN} = V_{CC}–2.1 V	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	V_{OLD} = 1.1 V	
	I_{OHD}	5.5	—	—	—	–75	—	mA	V_{OHD} = 3.85 V	
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	µA	V_{IN} = V_{CC} or ground	

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics: HD74AC283

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF			Ta = –40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay C_0 to S_n	t_{PLH}	3.3	1.0	11.5	15.0	1.0	16.5	ns
		5.0	1.0	9.5	11.5	1.0	12.5	
Propagation delay C_0 to S_n	t_{PHL}	3.3	1.0	10.5	14.0	1.0	15.5	ns
		5.0	1.0	8.5	10.5	1.0	11.5	
Propagation delay A_n or B_n to S_n	t_{PLH}	3.3	1.0	14.0	17.0	1.0	18.5	ns
		5.0	1.0	11.5	13.5	1.0	14.5	
Propagation delay A_n or B_n to S_n	t_{PHL}	3.3	1.0	13.5	16.5	1.0	18.0	ns
		5.0	1.0	11.0	13.0	1.0	14.0	
Propagation delay C_0 to C_4	t_{PLH}	3.3	1.0	9.5	12.5	1.0	15.5	ns
		5.0	1.0	7.5	9.5	1.0	10.5	
Propagation delay C_0 to C_4	t_{PHL}	3.3	1.0	10.0	13.0	1.0	14.0	ns
		5.0	1.0	8.0	10.0	1.0	11.0	
Propagation delay A_n or B_n to C_4	t_{PLH}	3.3	1.0	11.5	14.5	1.0	16.0	ns
		5.0	1.0	9.5	11.5	1.0	12.5	
Propagation delay A_n or B_n to C_4	t_{PHL}	3.3	1.0	12.0	15.0	1.0	16.5	ns
		5.0	1.0	10.0	12.0	1.0	13.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT283

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF			Ta = –40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay C_0 to S_n	t_{PLH}	5.0	1.0	11.5	13.5	1.0	14.5	ns
Propagation delay C_0 to S_n	t_{PHL}	5.0	1.0	10.0	12.0	1.0	13.0	ns
Propagation delay A_n or B_n to S_n	t_{PLH}	5.0	1.0	13.0	15.0	1.0	16.5	ns
Propagation delay A_n or B_n to S_n	t_{PHL}	5.0	1.0	12.0	14.0	1.0	15.5	ns
Propagation delay C_0 to C_4	t_{PLH}	5.0	1.0	9.0	11.0	1.0	12.0	ns
Propagation delay C_0 to C_4	t_{PHL}	5.0	1.0	10.0	12.0	1.0	13.0	ns
Propagation delay A_n or B_n to C_4	t_{PLH}	5.0	1.0	11.0	13.0	1.0	14.0	ns
Propagation delay A_n or B_n to C_4	t_{PHL}	5.0	1.0	11.5	13.5	1.0	14.5	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

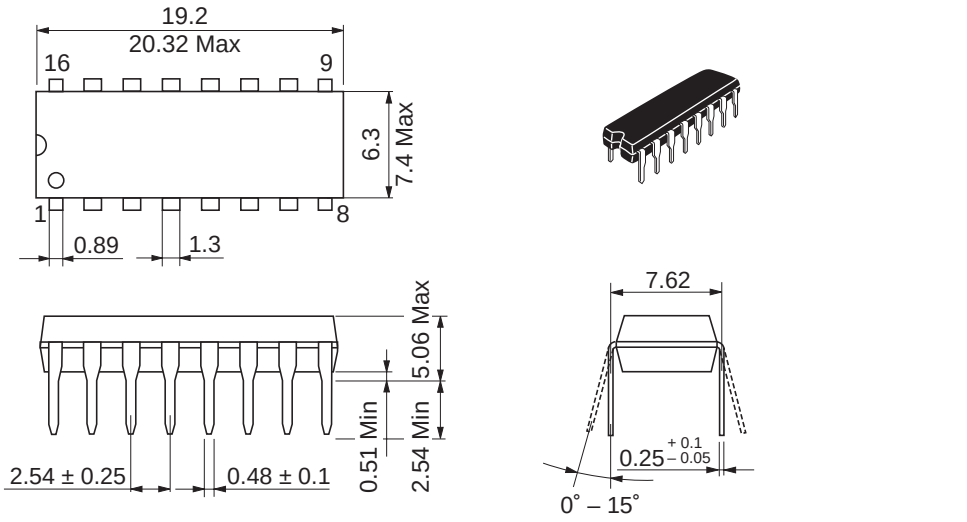
Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	60.0	pF	V_{CC} = 5.0 V

Package Dimensions

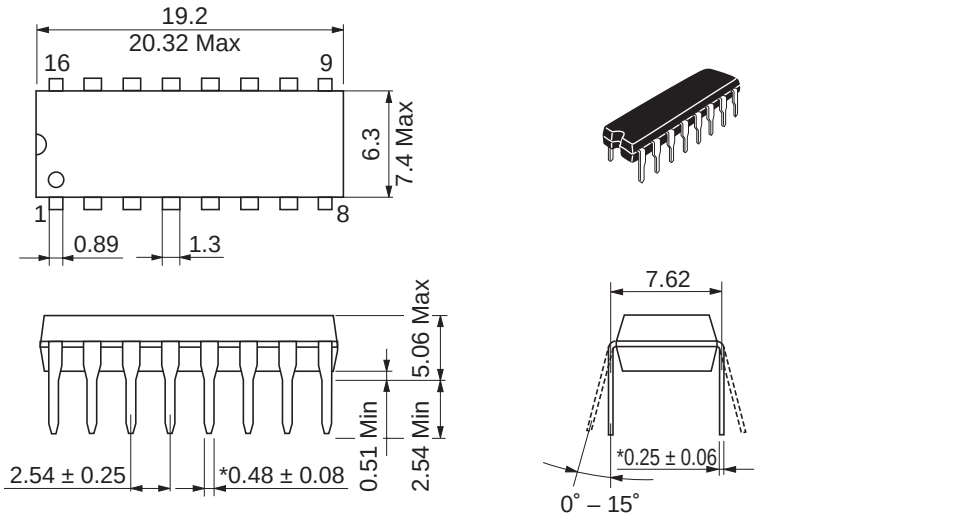
As of January, 2003

Unit: mm



Package Code	DP-16E
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	1.05 g

Unit: mm

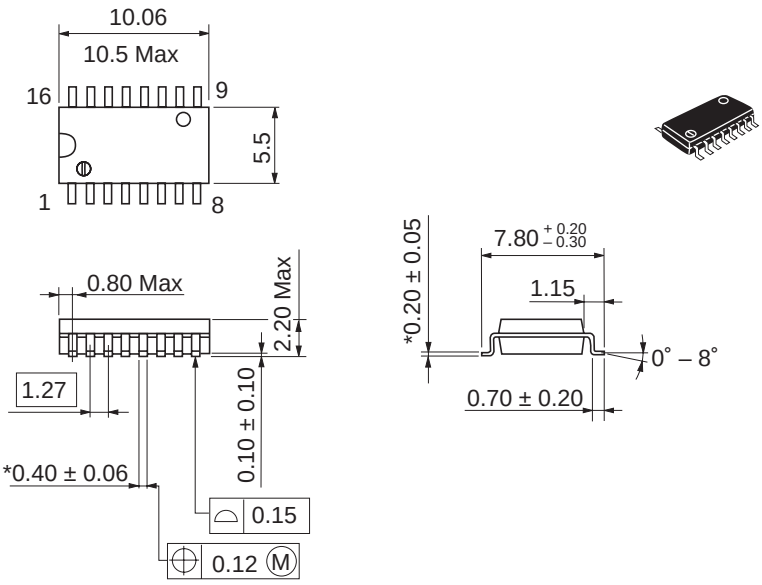


Package Code	DP-16FV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	1.05 g

*NI/Pd/AU Plating

As of January, 2003

Unit: mm

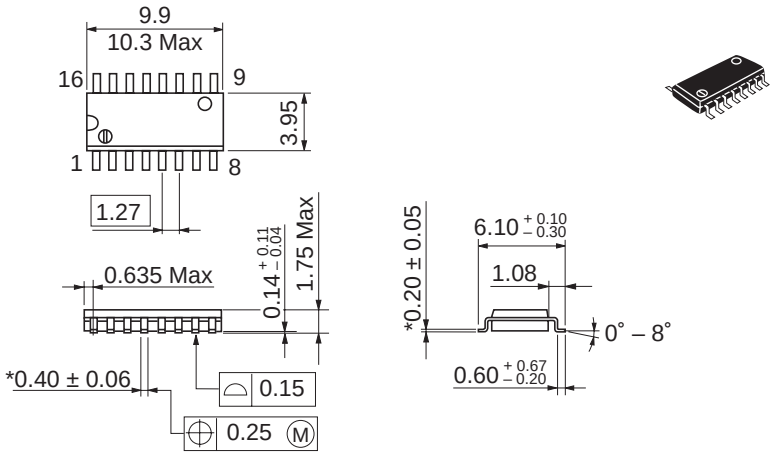


Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

*Ni/Pd/Au plating

As of January, 2003

Unit: mm



Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

*Ni/Pd/Au plating

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