

NHD-2.7-12864UCY3

Graphic OLED Display Module

NHD-	Newhaven Display
2.7-	2.7" diagonal size
12864-	128 x 64 pixel resolution
UC-	Model
Y-	Emitting Color: Yellow
3-	+3V power supply

Newhaven Display International, Inc.

2511 Technology Drive, Suite 101

Elgin IL, 60124

Ph: 847-844-8795

Fax: 847-844-8796

www.newhavendisplay.com

nhtech@newhavendisplay.com

nhsales@newhavendisplay.com

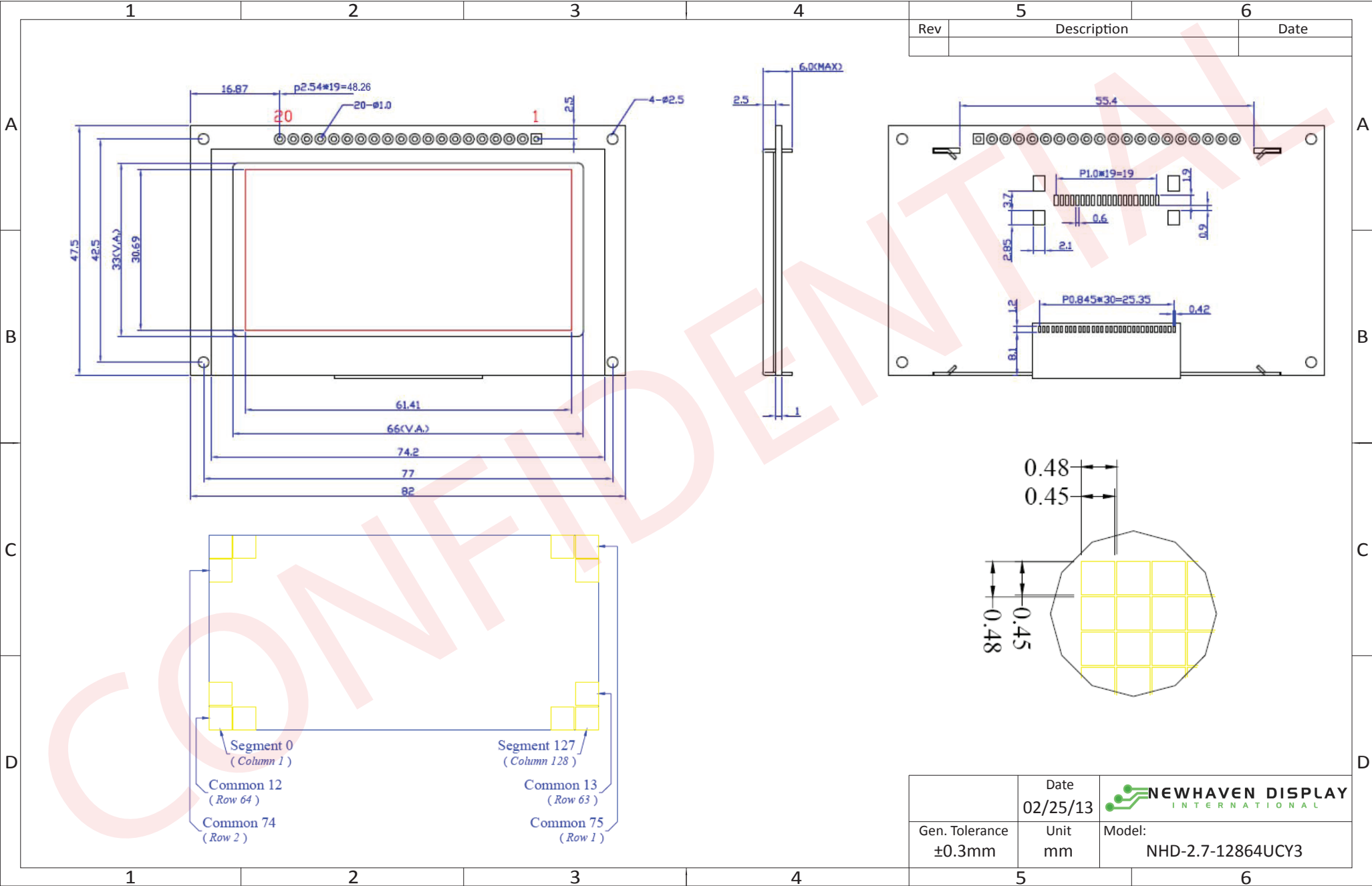
Document Revision History

Revision	Date	Description	Changed by
0	5/1/2011	Initial Product Release	-
1	7/01/2011	Updated Pin Measurement on Mechanical Drawing	MC
2	2/25/2013	Electrical characteristics and mechanical drawing updated	JN

Functions and Features

- 128 x 64 pixel resolution
- Built-in SSD1325 controller
- Parallel or serial MPU interface
- Single, low voltage power supply
- RoHS compliant

Mechanical Drawing



The drawing contained herein is the exclusive property of Newhaven Display International, Inc. and shall not be copied, reproduced, and/or disclosed in any format without permission.

Interface Description

Parallel Interface:

Pin No.	Symbol	External Connection	Function Description
1	VSS	Power Supply	Ground
2	VDD	Power Supply	Supply Voltage for OLED and logic.
3	NC	-	No Connect
4	D/C	MPU	Register select signal. D/C=0: Command, D/C=1: Data
5	R/W or /WR	MPU	6800-interface: Read/Write select signal, R/W=1: Read R/W: =0: Write 8080-interface: Active LOW Write signal.
6	E or /RD	MPU	6800-interface: Operation enable signal. Falling edge triggered. 8080-interface: Active LOW Read signal.
7-14	DB0 – DB7	MPU	8-bit Bi-directional data bus lines.
15	NC	-	No Connect
16	/RES	MPU	Active LOW Reset signal.
17	/CS	MPU	Active LOW Chip Select signal.
18	NC	-	No Connect
19	BS2	MPU	MPU Interface Select signal.
20	BS1	MPU	MPU Interface Select signal.

Serial Interface:

Pin No.	Symbol	External Connection	Function Description
1	VSS	Power Supply	Ground
2	VDD	Power Supply	Supply Voltage for OLED and logic.
3	NC	-	No Connect
4	D/C	MPU	Register select signal. D/C=0: Command, D/C=1: Data
5-6	VSS	Power Supply	Ground
7	SCLK	MPU	Serial Clock signal.
8	SDIN	MPU	Serial Data Input signal.
9	NC	-	No Connect
10-14	VSS	Power Supply	Ground
15	NC	-	No Connect
16	/RES	MPU	Active LOW Reset signal.
17	/CS	MPU	Active LOW Chip Select signal.
18	NC	-	No Connect
19	BS2	MPU	MPU Interface Select signal.
20	BS1	MPU	MPU Interface Select signal.

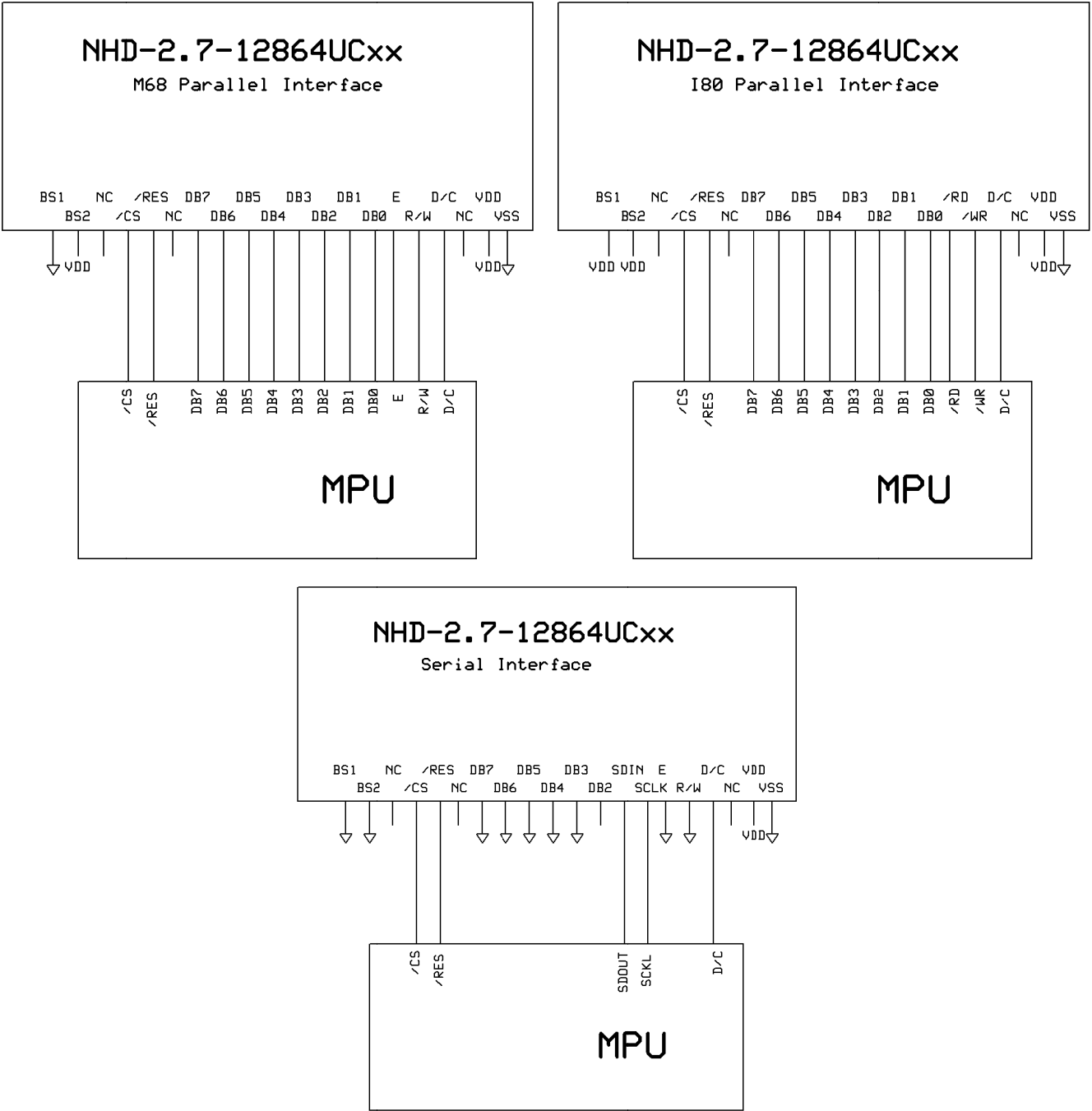
MPU Interface Pin Selections

Pin Name	6800 Parallel 8-bit interface	8080 Parallel 8-bit interface	Serial Interface
BS2	1	1	0
BS1	0	1	0

MPU Interface Pin Assignment Summery

Bus Interface	Data/Command Interface								Control Signals				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W	/CS	D/C	/RES
8-bit 6800	D[7:0]								E	R/W	/CS	D/C	/RES
8-bit 8080	D[7:0]								/RD	/WR	/CS	D/C	/RES
SPI	Tie LOW				NC		SDIN	SCLK	Tie LOW		/CS	D/C	/RES

Wiring Diagrams



Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	Top	Absolute Max	-40	-	+85	°C
Storage Temperature Range	Tst	Absolute Max	-40	-	+90	°C
Supply Voltage	VDD		-	3.3	3.5	V
Supply Current (logic)	IDD	Ta=25°C, VDD=3.3V	-	4	4	mA
Supply Current (display)	ICC	50% ON, VDD=3.3V	-	175	185	mA
		100% ON, VDD=3.3V	-	295	310	mA
Sleep Mode Current	IDD+ICC _{SLEEP}		-	2	10	µA
“H” Level input	Vih		0.8*VDD	-	VDD	V
“L” Level input	Vil		VSS	-	0.2*VDD	V
“H” Level output	Voh		0.9*VDD	-	VDD	V
“L” Level output	Vol		VSS	-	0.1*VDD	V

Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing Angle – Top	AV		-	80	-	°
Viewing Angle – Bottom	AV		-	80	-	°
Viewing Angle – Left	AH		-	80	-	°
Viewing Angle – Right	AH		-	80	-	°
Contrast Ratio	Cr		2000:1	-	-	-
Response Time (rise)	Tr	-	-	10	-	µs
Response Time (fall)	Tf	-	-	10	-	µs
Brightness		50% checkerboard	70	100	-	cd/m ²
Lifetime		Ta=25°C, 50% checkerboard	40,000	-	-	Hrs

Note: Lifetime at typical temperature is based on accelerated high-temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until **Half-Brightness**. The Display OFF command can be used to extend the lifetime of the display.

Luminance of active pixels will degrade faster than inactive pixels. Residual (burn-in) images may occur. To avoid this, every pixel should be illuminated uniformly.

Built-in SSD1325 controller

Instruction Table

Instruction	Code										Description	RESET value
	D/C	HEX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Set Column Address	0	15	0	0	0	1	0	1	0	1	Set column start and end address A[5:0]: Column start address. Range: 0-63d B[5:0]: Column end address. Range: 0-63d	0 63d
	0	A[5:0]	*	*	A5	A4	A3	A2	A1	A0		
	0	B[5:0]	*	*	B5	B4	B3	B2	B1	B0		
Set Row Address	0	75	0	1	1	1	0	1	0	1	Set row start and end address A[6:0]: Row start address. Range: 0-79d B[6:0]: Row end address. Range: 0-79d	0 79d
	0	A[6:0]	*	A6	A5	A4	A3	A2	A1	A0		
	0	B[6:0]	*	B6	B5	B4	B3	B2	B1	B0		
Set Contrast Control	0	81	1	0	0	0	0	0	0	1	Double byte command to select 1 out of 128 contrast steps. Contrast increases as the value increases.	0x40
	0	A[6:0]	*	A6	A5	A4	A3	A2	A1	A0		
Set Current Range	0	84~86	1	0	0	0	0	1	X1	X0	0x84 = Quarter Current Range 0x85 = Half Current Range 0x86 = Full Current Range	0x84
Set Remap	0	A0	1	0	1	0	0	0	0	0	A[0] = 0; Disable Column Address remap A[0] = 1; Enable Column Address remap A[1] = 0; Disable Nibble remap A[1] = 1; Enable Nibble remap A[2] = 0; Horizontal Address Increment A[2] = 1; Vertical Address Increment A[4] = 0; Disable COM remap A[4] = 1; Enable COM A[6] = 0; Disable COM split Odd/Even A[6] = 1; Enable COM split Odd/Even	0
	0	A[6:0]	*	A6	*	A4	*	A2	A1	A0		0
												0
												0
												0
												0
Set Display Start Line	0	A1	1	0	1	0	0	0	0	1	Set display RAM display start line register from 0-79.	0
	0	A[6:0]	*	A6	A5	A4	A3	A2	A1	A0		
Set Display Offset	0	A2	1	0	1	0	0	0	1	0	Set vertical shift by COM from 0~79.	0
	0	A[6:0]	*	A6	A5	A4	A3	A2	A1	A0		
Display Mode	0	A4/A7	1	0	1	0	0	X2	X1	X0	0xA4 = Normal display 0xA5 = Entire display ON, all pixels Grayscale level 15 0xA6 = Entire display OFF 0xA7 = Inverse display	0xA4
Set Multiplex Ratio	0	A8	1	0	1	0	1	0	0	0	Set MUX ratio to N+1 MUX N=A[6:0]; from 16MUX to 80MUX (0 to 14 are invalid)	80
	0	A[6:0]	*	A6	A5	A4	A3	A2	A1	A0		
Master configuration	0	AD	1	0	1	0	1	1	0	1	A[0] = 0; Disable DC-DC converter A[0] = 1; Enable DC-DC converter A[1] = 0; Disable internal VCOMH A[1] = 1; Enable internal VCOMH	1
	0	A[1:0]	*	*	*	*	*	*	A1	A0		1
Set Display ON/OFF	0	AE~AF	1	0	1	0	X3	1	1	1	0xAE = Display OFF (sleep mode) 0xAF = Display ON	A Eh

Set VCOMH Voltage	0 0	BE A[5:0]	1 *	0 *	1 A5	1 A4	1 A3	1 A2	1 A1	0 A0	Sets the VCOMH voltage level 000000-011111. A[5:0] = 1xxxxx = 1.0*VREF	010001
Set Precharge Voltage	0 0	BC A[7:0]	1 A7	0 A6	1 A5	1 A4	1 A3	1 A2	0 A1	0 A0	Sets the precharge voltage level 00000000-00011111 A[7:0] = 1xxxxxxx connects to VCOMH A[7:0] = 001xxxxx equals 1.0*VREF	00011000
Set Phase Length	0 0 0	B1 A[3:0] A[7:4]	1 * A7	0 * A6	1 * A5	1 * A4	0 A3 *	0 A2 *	0 A1 *	1 A0 *	A[3:0] = P1. Phase 1 period of 1-15 DCLK clocks A[7:4] = P2. Phase 2 period of 1-15 DCLK clocks	3 5
Set Row Period	0 0	B2 A[7:0]	1 A7	0 A6	1 A5	1 A4	0 A3	0 A2	1 A1	0 A0	Sets number of DCLKs (K) per row. Range 2-158DCLKs. K = P1 + P2 + GS15 pulse width (RESET values: 3 + 5 + 29)	37DCLKs (0x25)
Set Display Clock Divide Ratio / Oscillator Frequency	0 0 0	B3 A[3:0] A[7:4]	1 * A7	0 * A6	1 * A5	1 * A4	0 A3 *	0 A2 *	1 A1 *	1 A0 *	A[3:0] = Define the divide ratio of the display clocks. Range 1-16 Divide ratio = A[3:0] + 1 A[7:4] = Set the Oscillator Frequency. Frequency increases with the value of A[7:4]. Range 0000b~1111b.	2 0
Set Grayscale Table	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	B8 A[2:0] B[2:0] B[6:4] C[2:0] C[6:4] D[2:0] D[6:4] E[2:0] E[6:4] F[2:0] F[6:4] G[2:0] G[6:4] H[2:0] H[6:4]	1 * * * * * * * * * * * * * * * * * *	0 * * B6 * C6 * D6 * E6 * F6 * G6 * H6	0 * * B5 * C5 * D5 * E5 * F5 * G5 * H5	0 * * B4 * C4 * D4 * E4 * F4 * G4 * H4	1 * * * * * * * * * * * * * * * * * *	0 A2 B2 * C2 * D2 * E2 * F2 * G2 * H2	0 A1 B1 * C1 * D1 * E1 * F1 * G1 * H1	0 A0 B0 * C0 * D0 * E0 * F0 * G0 * H0	Sets the gray scale level. Range 1-15 A[2:0] = L1 B[2:0] = L2 B[6:4] = L3 C[2:0] = L4 C[6:4] = L5 D[2:0] = L6 D[6:4] = L7 E[2:0] = L8 E[6:4] = L9 F[2:0] = L10 F[6:4] = L11 G[2:0] = L12 G[6:4] = L13 H[2:0] = L14 H[6:4] = L15	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Set Biasing Current for DC-DC converter	0 0	CF A[7:6]	1 A7	1 A6	0 *	0 *	1 *	1 *	1 *	1 *	0xF0 = HIGH 0x70 = LOW	0xF0
NOP	0	E3	1	1	1	0	0	0	1	1	Command for No Operation	

For detailed instruction information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1325.pdf

MPU Interface

For detailed timing information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1325.pdf

6800-MPU Parallel Interface

The parallel interface consists of 8 bi-directional data pins, R/W, D/C, E, and /CS.

A LOW on R/W indicates write operation, and HIGH on R/W indicates read operation.

A LOW on D/C indicates “Command” read or write, and HIGH on D/C indicates “Data” read or write.

The E input serves as data latch signal, while /CS is LOW. Data is latched at the falling edge of E signal.

Function	E	R/W	/CS	D/C
Write Command	↓	0	0	0
Read Status	↓	1	0	0
Write Data	↓	0	0	1
Read Data	↓	1	0	1

8080-MPU Parallel Interface

The parallel interface consists of 8 bi-directional data pins, /RD, /WR, D/C, and /CS.

A LOW on D/C indicates “Command” read or write, and HIGH on D/C indicates “Data” read or write.

A rising edge of /RS input serves as a data read latch signal while /CS is LOW.

A rising edge of /WR input serves as a data/command write latch signal while /CS is LOW.

Function	/RD	/WR	/CS	D/C
Write Command	1	↑	0	0
Read Status	↑	1	0	0
Write Data	1	↑	0	1
Read Data	↑	1	0	1

Alternatively, /RD and /WR can be kept stable while /CS serves as the data/command latch signal.

Function	/RD	/WR	/CS	D/C
Write Command	1	0	↑	0
Read Status	0	1	↑	0
Write Data	1	0	↑	1
Read Data	0	1	↑	1

Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, and /CS.

D0 acts as SCLK and D1 acts as SDIN. D2 should be left open. D3~D7, E, and R/W should be connected to GND.

Function	/RD	/WR	/CS	D/C	D0
Write Command	0	0	0	0	↑
Write Data	0	0	0	1	↑

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6,...D0.

D/C is sampled on every eighth clock and the data byte in the shift register is written to the GDRAM or command register in the same clock.

Note: Read is not available in serial mode.

For detailed protocol information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1325.pdf

Example Initialization Sequence:

```
Set_Display_On_Off_12864(0x00);      // Display Off (0x00/0x01)
Set_Display_Clock_12864(0x91);       // Set Clock as 135 Frames/Sec
Set_Multiplex_Ratio_12864(0x3F);     // 1/64 Duty (0x0F~0x5F)
Set_Display_Offset_12864(0x4C);      // Shift Mapping RAM Counter (0x00~0x5F)
Set_Start_Line_12864(0x00);          // Set Mapping RAM Display Start Line (0x00~0x5F)
Set_Master_Config_12864(0x00);       // Disable Embedded DC/DC Converter (0x00/0x01)
Set_Remap_Format_12864(0x50);        // Set Column Address 0 Mapped to SEG0
                                     //  Disable Nibble Remap
                                     //  Horizontal Address Increment
                                     //  Scan from COM[N-1] to COM0
                                     //  Enable COM Split Odd Even
Set_Current_Range_12864(0x02);       // Set Full Current Range
Set_Gray_Scale_Table_12864();        // Set Pulse Width for Gray Scale Table
Set_Contrast_Current_12864(brightness); // Set Scale Factor of Segment Output Current Control
Set_Frame_Frequency_12864(0x51);     // Set Frame Frequency
Set_Phase_Length_12864(0x55);        // Set Phase 1 as 5 Clocks & Phase 2 as 5 Clocks
Set_Precharge_Voltage_12864(0x10);   // Set Pre-Charge Voltage Level
Set_Precharge_Compensation_12864(0x20,0x02); // Set Pre-Charge Compensation
Set_VCOMH_12864(0x1C);               // Set High Voltage Level of COM Pin
Set_VSL_12864(0x0D);                 // Set Low Voltage Level of SEG Pin
Set_Display_Mode_12864(0x00);        // Normal Display Mode (0x00/0x01/0x02/0x03)
Fill_RAM_12864(0x00);                // Clear Screen
Set_Display_On_Off_12864(0x01);      // Display On (0x00/0x01)
```

Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Test the endurance of the display at high storage temperature.	+90°C , 240hrs	2
Low Temperature storage	Test the endurance of the display at low storage temperature.	-40°C , 240hrs	1,2
High Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature.	+85°C 240hrs	2
Low Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at low temperature.	-40°C , 240hrs	1,2
High Temperature / Humidity Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature with high humidity.	+60°C , 90% RH , 240hrs	1,2
Thermal Shock resistance	Test the endurance of the display by applying electric stress (voltage & current) during a cycle of low and high temperatures.	-40°C,30min -> 25°C,5min -> 85°C,30min = 1 cycle 100 cycles	
Vibration test	Test the endurance of the display by applying vibration to simulate transportation and use.	10-22Hz , 15mm amplitude. 22-500Hz, 1.5G 30min in each of 3 directions X,Y,Z	3
Atmospheric Pressure test	Test the endurance of the display by applying atmospheric pressure to simulate transportation by air.	115mbar, 40hrs	3
Static electricity test	Test the endurance of the display by applying electric static discharge.	VS=800V, RS=1.5kΩ, CS=100pF One time	

Note 1: No condensation to be observed.

Note 2: Conducted after 2 hours of storage at 25°C, 0%RH.

Note 3: Test performed on product itself, not inside a container.

Evaluation Criteria:

- 1: Display is fully functional during operational tests and after all tests, at room temperature.
- 2: No observable defects.
- 3: Luminance >50% of initial value.
- 4: Current consumption within 50% of initial value

Precautions for using OLEDs/LCDs/LCMs

See Precautions at www.newhavendisplay.com/specs/precautions.pdf

Warranty Information and Terms & Conditions

http://www.newhavendisplay.com/index.php?main_page=terms

Newhaven Display International, Inc. reserves the right to alter this product or specification at any time without notification.