8-Bit, 100 MSPS 3V A/D Converter

AD9283S

1.0 Scope

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aerospace

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD9283

2.0 PART NUMBER. The complete part number(s) of this specification follow:

Part Number	Description
AD9283-703RC	8-Bit, 100 MSPS 3V ADC

3.0 Case Outline

Letter	Descriptive designator	Case Outline
RC	CQCC1-N20	20 – Terminal leadless chip carrier (LCC)

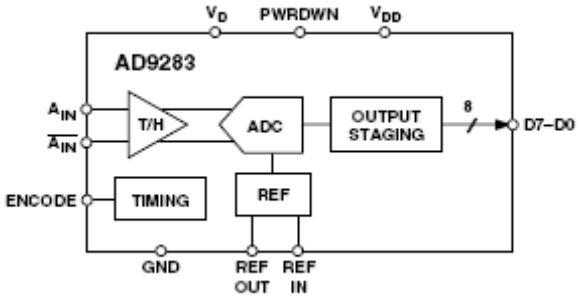

Figure 1 – Functional Block Diagram

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Package: RC			
Pin Number	**Name**	**Type**	**Description**
1	PWRDWN	DI	Power-Down Function Select; Logic HIGH for Power-Down Mode (Digital Outputs go to high impedance state)
2	VREF OUT	AO	Internal Reference Output (1.25 V typ); Bypass with 0.1 µF to Ground
3	VREF IN	AI	Reference Input for ADC (1.25 V typ)
4	GND	P	Ground
5	V_D	P	Analog 3 V Power Supply
6	A_{IN} BAR	AI	Analog Input for ADC (Can be left open if operating in single-ended mode, but recommend connection to a 0.1 µF capacitor and a 25 Ω resistor in series to Ground for better input matching)
7	A_{IN}	AI	Analog Input for ADC
8	V_D	P	Analog 3 V Power Supply
9	GND	P	Ground
10	ENCODE	DI	Encode Clock for ADC (ADC Samples on Rising Edge of ENCODE)
11	D7	DO	Data Output MSB. ADC DB7
12	D6	DO	Data Output. ADC DB6
13	D5	DO	Data Output. ADC DB5
14	D4	DO	Data Output. ADC DB4
15	V_{DD}	P	Digital output power supply. Nominally 2.5 V to 3.6 V
16	GND	P	Ground
17	D3	DO	Data Output. ADC DB3
18	D2	DO	Data Output. ADC DB2
19	D1	DO	Data Output. ADC DB1
20	D0	DO	Data Output LSB. ADC DB0

Type: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.

Figure 2 – Terminal Connections and Pin Function Descriptions

4.0 ABSOLUTE MAXIMUM RATINGS. (T_A = 25°C, unless otherwise noted)

V_D, V_{DD} 4V
Analog Input ..... -0.5V to V_D + 0.5V
Digital Inputs ..... -0.5V to V_{DD} + 0.5V
VREF IN ..... -0.5V to V_D + 0.5V
Digital Output Current 20mA
Operating Temperature Range ..... -55 °C to +125 °C
Storage Temperature Range ..... -65 °C to +150 °C
Maximum Junction Temperature ..... +150 °C

NOTES

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

5.0 THERMAL CHARACTERISTICS:

Package Type	Junction-to-Case (Θ_{JC})	Junction-to-Ambient (Θ_{JA})	Units
RC (LCC Package)	35	110	°C/W Max

6.0 Table I. Electrical Table:

Table I						
Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Subgroup	Limit Min	Limit Max	Units
DC ACCURACY						
Differential Nonlinearity	DNL		1	-1	+1.25	LSB
			2, 3	-1	+1.50	
Integral Nonlinearity	INL		1	-1.25	+1.25	LSB
			2, 3	-3.5	+3.5	
No Missing Codes			1, 2, 3	Guaranteed		
Gain Error 2/	A_E		1	-6	+6	%FS
			2, 3	-8	+8	
ANALOG INPUT						
Input Offset Voltage	Vos		1	-40	+40	mV
			2, 3	-45	+45	
Reference Voltage	V_{REF}	With 100uA load	1	1.2	1.3	V
			2, 3	1.17	1.33	
Input Resistance	R_{IN}		1	7	13	kΩ
			2, 3	5	16	
SWITCHING PERFORMANCE						
Maximum Conversion Rate	ENC _freq		9,10,11	100		MSPS
Output Propagation Delay 3/	t_{PD}		9		7.0	ns
DIGITAL INPUTS, ENC, PWRDWN						
Logic “1” Voltage	V_{IH}		1, 2, 3	2.0		V
Logic “0” Voltage	V_{IL}		1, 2, 3		0.8	V
Logic “1” Current	I_{IH}		1, 2, 3	-1.0	1.0	µA
Logic “0” Current	I_{IL}		1, 2, 3	-1.0	1.0	µA
DIGITAL OUTPUTS						
Logic “1” Voltage	V_{OH}		1, 2, 3	2.95		V
Logic “0” Voltage	V_{OL}		1, 2, 3		0.05	V
POWER SUPPLY						
Power Dissipation 4/	Pd		1, 2, 3		120	mW
Power-Down Dissipation	Pd_pwrdwn		1, 2, 3		7	mW
Power Supply Rejection Ratio	PSRR	VD= 2.85 to 3.15V	1	-18	18	mV/V

Table I, continued						
Parameter See notes at end of table	Symbol	Conditions 1/	Subgroup	Limit Min	Limit Max	Units
DYNAMIC PERFORMANCE 5/						
Signal-to-Noise Ratio (Without Harmonics)	SNR	f_{IN} = 41MHz	4	43.5		dB
Signal-to-Noise Ratio (With Harmonics)	SINAD	f_{IN} = 41MHz	4	42.5		dB
2nd Harmonic Distortion	2nd HD	f_{IN} = 41MHz	4	49		dBc
3rd Harmonic Distortion	3rd HD	f_{IN} = 41MHz	4	47		dBc

TABLE I NOTES:

1/ T_A = +25 °C, T_A Max = +125 °C, T_A Min = -55 °C. V_{DD} = 3.0V, V_D = 3.0V; single-ended input; external reference, unless otherwise noted.
2/ Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.25V external reference).
3/ t_{PD} is measured from the 1.5V level of the ENCODE input to the 50%/50% levels of the digital outputs swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of ± 40 µA.
4/ Power dissipation measured with encode at rated speed and a dc analog input.
5/ SNR/harmonics based on an analog input voltage of -0.7 dBFS referenced to a 1.024 V full-scale input range.

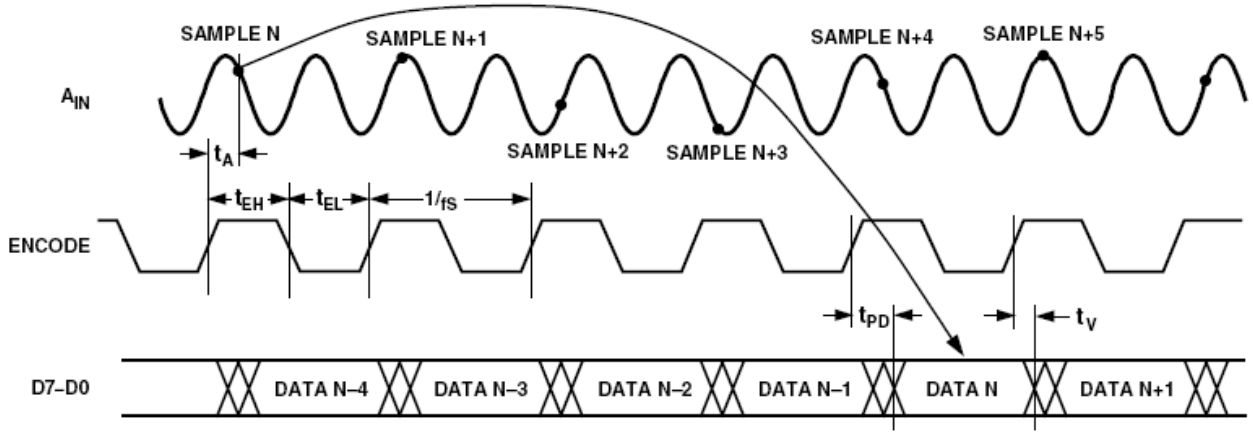

Figure 3 – Timing Diagram

7.0 Table II. Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4, 9, 10, 11 1/ 2/
Group A Test Requirements	1, 2, 3, 4, 9, 10, 11
Group C end-point electrical parameters	1 2/
Group D end-point electrical parameters	1

Notes:

1/ PDA apply to Subgroup 1 only. Delta's excluded from PDA.
2/ See Table III for Delta parameters. See Table I for test conditions.

8.0 Table III. Life Test / Burn-in Delta limits:

Table III		
Test Symbol	**Delta Limit**	**Units**
Pd	±5	mW
Vos	±5	mV
A_E	±1	%FS

9.0 Life Test / Burn-In Circuit:

9.1 HTRB is not applicable for this drawing.

9.2 Burn-in is per MIL-STD-883 Method 1015 test condition D.

9.3 Steady state life test is per MIL-STD-883 Method 1005, test condition D.

10.0 MIL-STD-38535 QMLV exceptions:

10.1 Full WLA per MIL-STD-883 TM 5007 is not available for this product. SEM inspection only is available per MIL-STD-883, TM2018.

10.2 This product is manufactured in a MIL-PRF-38535 QMLQ certified wafer fab facility.

Rev	Description of Change	Date
A	Initiate	5/12/2008
B	Correct Section 1.0 Scope description. Update deltas for product release. Minor format improvements and clarifications for product release.	11/4/2008
C	Remove post Group C specification limits in Table III such that only Delta limits are listed. Remove QMLV exception for testing in QMLQ facility. Add Figure 1 block diagram and update pin connections with descriptions. Formatting improvements.	3/24/2010